

DESCRIPTION

Title of Invention

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD
5 THEREOF, AND STRUCTURE USED IN MANUFACTURE OF
SEMICONDUCTOR DEVICE

Technical Field

[0001] The present disclosure relates to a semiconductor device, a
manufacturing method for a semiconductor device, and a structure used
10 for the manufacture of a semiconductor device.

Background Art

[0002] Conventionally, wire bonding has been widely applied to the
connection of a semiconductor chip and a substrate. Wire bonding is a
method of connecting a semiconductor chip and a substrate using a fine
15 metal wire such as a gold wire. In order to respond to the request for
improved functionality, improved integration, increased speed, and the
like with regard to semiconductor devices (hereinafter, referred to as
"semiconductor package" in some cases), a method called flip-chip
connection is becoming widespread. Flip-chip connection is a method
20 of forming electroconductive protrusions called bumps on a
semiconductor chip or a substrate and thereby directly connecting the
semiconductor chip and the substrate.

[0003] As described above, semiconductor packages are required to
undergo thickness reduction and size reduction in addition to improved
25 functionality. As semiconductor packages that are required to undergo
further size reduction, thickness reduction, and improved functionality,

chip stack type packages, POP (package on package), TSV (through silicon via), and the like are also beginning to be popularly spread. These semiconductor packages can be reduced in size because the chips are disposed in a three-dimensional shape instead of a planar shape. For example, Patent Literature 1 discloses a semiconductor device of an aspect in which a first semiconductor element (for example, a controller) is embedded in an adhesive film for adhering a second semiconductor element.

Citation List

Patent Literature

[0004] Patent Literature 1: Japanese Unexamined Patent Publication No. 2015-120836

Summary of Invention

Technical Problem

[0005] According to an investigation of the inventors of the present invention, when a first chip on a substrate is embedded in an adhesive film as in the case of the semiconductor device described in Patent Literature 1, there is a problem that voids are likely to be generated. Furthermore, when a relatively soft adhesive film having excellent fluidity is used in order to suppress void generation, the position of the second chip to be adhered by means of the adhesive film may be shifted or distorted, and it tends to be difficult to further stack a plurality of chips thereon. In addition to this, it is necessary to use an adhesive film having a thickness sufficient so that the first chip can be embedded, and the semiconductor package tends to become thick.

[0006] The inventors of the present invention have examined a

configuration in which a space is formed by disposing a spacer around the position at which a first chip is disposed, instead of embedding the first chip in an adhesive film, the first chip is disposed within this space, and the space is filled with a sealing material. As a result, it has been found that at the time of filling the space with a sealing material, when there is a difference between the height of the top face of the spacer and the height of the top face of the first chip, filling with the sealing material tends to be difficult.

[0007] The present disclosure provides a manufacturing method for a semiconductor device having a configuration in which a first chip is mounted on a substrate and a second chip is disposed above the first chip, by which a semiconductor device can be suppressed from becoming excessively thick, and an operation of sealing the first chip and the second chip with a sealing material can be easily performed. Furthermore, the present disclosure provides a semiconductor device that is not excessively thick and has excellent filling property by a sealing material, and a structure that is used for the manufacture of this semiconductor device.

Solution to Problem

[0008] A manufacturing method for a semiconductor device according to the present disclosure comprises: (A) a step of preparing a structure including a substrate, a first chip disposed on the substrate, and a plurality of spacers disposed around the first chip on the substrate; (B) a step of preparing an adhesive-piece-attached chip including a second chip having a size larger than that of the first chip, and an adhesive piece provided on one face of the second chip; (C) a step of disposing

the second chip above the first chip such that the adhesive piece of the adhesive-piece-attached chip comes into contact with the top faces of the spacers; and (D) a step of sealing the first chip, the spacers, and the second chip, wherein before the step (D) is carried out, the height of the top faces of the spacers coincides with the height of the top face of the first chip. Incidentally, the term "coincide" as used herein means that the difference between the height of the top faces of the spacers and the height of the top face of the first chip is less than 10 μm .

[0009] When it is said that the height of the top faces of the spacers coincides with the height of the top face of the first chip before the above-described step (D) is carried out, it is implied that the adhesive piece of the adhesive-piece-attached chip disposed in step (C) is also in contact with the top face of the first chip. If the top face of the first chip and the adhesive piece are not in contact, and there is a gap between the two, it is difficult to fill this gap with a sealing material, and voids are likely to occur. On the other hand, when the distance between the top face of the first chip and the adhesive piece is made sufficiently wide, the filling property of the sealing material is enhanced; however, the semiconductor device tends to become thicker. In contrast, according to the manufacturing method of the present disclosure, both excellent filling property of the sealing material and thickness reduction of the semiconductor device can be achieved.

[0010] With regard to the manufacturing method of the present disclosure, it is desirable that the height of the top faces of the spacers coincides with the height of the top face of the first chip before step (D) is carried out. For example, the height of the top faces of the spacers

may coincide with the height of the top face of the first chip in the structure prepared in step (A), or it is also acceptable that in the structure prepared in step (A), the top faces of the spacers are higher than the top face of the first chip, and in the subsequent step (C), the height of the top faces of the spacers and the height of the top face of the first chip are made to coincide with each other by squashing the spacers with the adhesive-piece-attached chip.

[0011] An aspect of the above-described spacer is a dummy chip comprising a chip and an adhesive piece provided on one face of this chip. As described above, in step (C), in a case where the height of the spacers is adjusted by squashing the spacers with the adhesive-piece-attached chip, it is preferable that the adhesive piece included in the dummy chip is softer than the adhesive piece included in the adhesive-piece-attached chip. Furthermore, it is preferable that the adhesive piece included in the dummy chip is thicker than the adhesive piece included in the adhesive-piece-attached chip.

[0012] From the viewpoint of increasing the speed of a semiconductor device, it is preferable that the first chip is mounted on the substrate by flip-chip connection. In a case where the first chip is mounted on the substrate by flip-chip connection, variation is likely to occur in the height of the connection part as compared to a case where the first chip is adhered to the substrate using an adhesive film, and as a result, variation is likely to occur in the height position of the top face of the first chip. For this reason, in a case where the first chip is mounted by flip-chip connection, it is preferable that a structure in which the top faces of the spacers are higher than the top face of the first chip is

prepared in step (A), so that the height of the spacers can be adjusted by squashing the spacers with the adhesive-piece-attached chip in step (C).

[0013] The semiconductor device according to the present disclosure comprises a substrate; a first chip disposed on the substrate; a plurality of spacers disposed around the first chip on the substrate; a second chip disposed above the first chip and having a size larger than that of the first chip; an adhesive piece adhering the spacers and the second chip; and a sealing material sealing the first chip, the spacers, and the second chip, wherein the adhesive piece is in contact with the top face of the first chip. The first chip is, for example, a controller chip.

[0014] The above-described semiconductor device can be manufactured by the manufacturing method according to the present disclosure. In the semiconductor device according to the present disclosure, since the adhesive piece is in contact with the top face of the first chip, the semiconductor device is not excessively thick, and the filling property of the sealing material is excellent.

[0015] The present disclosure provides a structure used for the manufacture of the above-described semiconductor device. A structure according to a first aspect comprises a substrate; a first chip disposed on the substrate; and a plurality of spacers disposed around the first chip on the substrate, and the height of the top faces of the spacers coincides with the height of the top face of the first chip. A structure according to a second aspect comprises a substrate; a first chip disposed on the substrate; and a plurality of spacers disposed around the first chip on the substrate, and the top faces of the spacers are higher than the top face of the first chip, and the spacers include a material capable of making the

height of the top faces of the spacers coincide with the height of the top face of the first chip, by being squashed.

[0016] The structure according to the present disclosure may be an aspect further comprising a second chip. The structure of this aspect comprises a substrate; a first chip disposed on the substrate; a plurality of spacers disposed around the first chip on the substrate; a second chip disposed above the first chip and having a size larger than that of the first chip; and an adhesive piece adhering the spacers and the second chip, and the adhesive piece is in contact with the top face of the first chip.

Advantageous Effects of Invention

[0017] According to the present disclosure, there is provided a manufacturing method for a semiconductor device having a configuration in which a first chip is mounted on a substrate and a second chip is disposed above the first chip, the manufacturing method being capable of suppressing the semiconductor device from becoming excessively thick and capable of easily performing an operation of sealing the first chip and the second chip with a sealing material. Furthermore, according to the present disclosure, a semiconductor device that is not excessively thick and has excellent filling property of the sealing material, and a structure that is used for the manufacture of this semiconductor device are provided.

Brief Description of Drawings

[0018] FIG. 1 is a cross-sectional view schematically illustrating a first embodiment of a semiconductor device according to the present disclosure.

FIG. 2(a) and FIG. 2(b) are plan views schematically illustrating an example of the positional relationship between a first chip and a plurality of dummy chips.

FIG. 3(a) to FIG. 3(e) are cross-sectional views schematically illustrating an example of the process for manufacturing a dummy chip.

FIG. 4 is a cross-sectional view schematically illustrating the first embodiment of a structure used for the manufacture of the semiconductor device according to the present disclosure.

FIG. 5 is a cross-sectional view schematically illustrating an example of an adhesive-piece-attached chip.

FIG. 6 is a cross-sectional view schematically illustrating a state in which the adhesive-piece-attached chip illustrated in FIG. 5 is pressure-bonded to the structure illustrated in FIG. 4.

FIG. 7 is a cross-sectional view schematically illustrating another embodiment of the structure used for the manufacture of the semiconductor device according to the present disclosure.

FIG. 8 is a cross-sectional view schematically illustrating a state in which the adhesive-piece-attached chip illustrated in FIG. 5 is pressure-bonded to the structure illustrated in FIG. 7.

Description of Embodiments

[0019] Hereinafter, embodiments of the present disclosure will be described with appropriate reference to the drawings. In the following description, identical or equivalent parts will be assigned with the same reference numeral, and any overlapping description will not be repeated. Furthermore, it should be noted that the positional relationship such as up, down, right, and left is based on the positional relationship shown in

the drawings, unless particularly stated otherwise. In addition, the dimensional ratios of the drawings are not limited to the ratios shown therein. Incidentally, the description of "(meth)acryl" in the present specification means "acryl" as well as "methacryl" corresponding thereto.

[0020] <First embodiment>

(Semiconductor device)

FIG. 1 is a cross-sectional view schematically illustrating a semiconductor device according to the present embodiment. A semiconductor device 100 illustrated in this drawing comprises a substrate 10; a chip S1 (first chip) disposed on the surface of the substrate 10; two dummy chips D (spacers) disposed on the surface of the substrate 10 and around the chip S1; a chip S2 (second chip) disposed above the chip S1; chips S3 and S4 stacked on the chip S2; wires w electrically connecting an electrode (not illustrated) on the surface of the substrate 10 with the chips S2, S3, and S4, respectively; and a sealing material 50 sealing the chips S1, S2, S3, and S4, the dummy chips D, and the wires w. Between the top face of the chip S1, the top faces of the dummy chips D, and the chip S2, a cured product Sc of an adhesive piece is disposed. In the semiconductor device 100, the height of the top face of the chip S1 coincides with the height of the top faces of the dummy chips D. That is, the cured product Sc is in contact with the top face of the chip S1 and the top faces of the dummy chips D.

[0021] The substrate 10 may be an organic substrate or may be a metal substrate such as a lead frame. With regard to the substrate 10, from

the viewpoint of suppressing warpage of the semiconductor device 100, the thickness of the substrate 10 is, for example, 90 to 300 μm and may be 90 to 210 μm .

[0022] The chip S1 is, for example, a controller chip and is mounted on the substrate 10 by flip-chip connection. The shape of the chip S1 as seen in a plan view is, for example, a rectangular shape (a square shape or an oblong shape). The length of one side of the chip S1 is, for example, 5 mm or less and may be 2 to 5 mm or 1 to 5 mm. The thickness of the chip S1 is, for example, 10 to 150 μm and may be 20 to 100 μm .

[0023] The chip S2 is, for example, a memory chip and is adhered above the chip S1 and the dummy chips D, with the cured product Sc of the adhesive piece interposed therebetween. The chip S2 as seen in a plan view has a size larger than that of the chip S1. The shape of the chip S2 as seen in a plan view is, for example, a rectangular shape (a square shape or an oblong shape). The length of one side of the chip S2 is, for example, 20 mm or less and may be 4 to 20 mm or 4 to 12 mm. The thickness of the chip S2 is, for example, 10 to 170 μm and may be 20 to 120 μm . Incidentally, the chips S3 and S4 are also, for example, memory chips and are adhered above the chip S2, with the cured product Sc of the adhesive piece interposed therebetween. The length of one side of the chips S3 and S4 may be similar to that of the chip S2, and the thickness of the chips S3 and S4 may also be similar to that of the chip S2.

[0024] The dummy chips D accomplish the role of spacers that form a space around the chip S1. The dummy chips D are composed of a chip

D1 and an adhesive piece Da provided on one face of the chip D1. As illustrated in FIG. 2(a), two dummy chips D (shape: oblong shape) may be disposed at positions separated apart from the two sides of the chip S1, or as illustrated in FIG. 2(b), one dummy chip D (shape: square shape, four units in total) may be disposed at each of the positions corresponding to the corners of the chip S1. The length of one side of the chip D1 as seen in a plan view is, for example, 20 mm or less and may be 1 to 20 mm or 1 to 12 mm. The thickness of the chip D1 is, for example, 30 to 150 μm and may be 80 to 120 μm .

[0025] As described above, the height of the top faces of the dummy chips D coincides with the height of the top face of the chip S1. The position of the top face of the flip-chip connected chip S1 can be made to coincide with the position of the top faces of the dummy chips D by, for example, adjusting the thickness of the adhesive piece Da.

[0026] An example of a method for producing a dummy chip D, which is an aspect of an adhesive-piece-attached chip, will be described with reference to FIG. 3(a) to FIG. 3(e). First, a dicing-die bonding integrated film 8 (hereinafter, referred to as "film 8" in some cases) is prepared, and this is disposed in a predetermined device (not illustrated). The film 8 comprises a base material film 1, a tacky adhesive layer 2, and an adhesive layer 3A in this order. The base material film 1 is, for example, a polyethylene terephthalate film (PET film). The tacky adhesive layer 2 has a property that tacky adhesiveness is deteriorated by being irradiated with ultraviolet radiation. The adhesive layer 3A is formed from a heat-curable resin composition.

[0027] As illustrated in FIG. 3(a) and FIG. 3(b), the film 8 is attached to one face of a wafer W such that the adhesive layer 3A comes into contact with the face of the wafer W. The wafer W may be a single crystal silicon or may be a polycrystalline silicon, one of various ceramics, or a compound semiconductor such as gallium arsenide. Incidentally, in a case where the dummy chips D are produced, the wafer W does not have to be a semiconductor and may be, for example, a glass substrate.

[0028] The wafer W and the adhesive layer 3A are cut using a dicing blade (see FIG. 3(c)). As the wafer W is singulated by dicing, a chip D1 is formed. As the adhesive layer 3A is singulated by dicing, an adhesive piece Da is formed. Subsequently, as illustrated in FIG. 3(d), the tacky adhesive force between the tacky adhesive layer 2 and the adhesive layer 3A is lowered by irradiating the tacky adhesive layer 2 with ultraviolet radiation. After irradiation with ultraviolet radiation, as illustrated in FIG. 3(e), dummy chips D are separated apart from each other by expanding the base material film 1. A dummy chip D is detached from the tacky adhesive layer 2 by pushing up the dummy chip D with a needle 42, and at the same time, the dummy chip D is picked up by suctioning the dummy chip D with a suction collet 44.

[0029] (Manufacturing method for semiconductor device)

A manufacturing method for the semiconductor device 100 will be described with reference to FIG. 4 to FIG. 6. The manufacturing method for the semiconductor device 100 includes the following steps (A) to (D).

(A) A step of preparing a structure 30A comprising a substrate

10; a chip S1 disposed on the substrate 10; and a plurality of dummy chips D disposed on the substrate 10 and around the chip S1 (see FIG. 4).

(B) A step of preparing an adhesive-piece-attached chip S2a comprising a chip S2 and an adhesive piece Sa provided on one face of the chip S2 (see FIG. 5).

(C) A step of disposing the chip S2 above the chip S1 such that the adhesive piece Sa comes into contact with the top faces of the dummy chips D and the top face of the chip S1 (see FIG. 6).

(D) A step of sealing the chips S1, S2, S3, and S4, the dummy chips D, and the like.

[0030] [Step (A)]

Step (A) is a step of preparing the structure 30A illustrated in FIG. 4. The structure 30A comprises a substrate 10, a chip S1 disposed on the surface of the substrate, and a plurality of dummy chips D, and the height of the top face of the chip S1 coincides with the height of the top faces of the dummy chips D. For example, first, the chip S1 is mounted at a predetermined position on the substrate 10 by flip-chip connection, and subsequently, the dummy chips D may be pressure-bonded at predetermined positions. It is preferable that this pressure-bonding treatment is carried out, for example, under the conditions of 80°C to 180°C and 0.01 to 0.50 MPa for 0.5 to 3.0 seconds. The height of the top faces of the dummy chips D can be adjusted by adjusting the pressing pressure to be applied to the dummy chips D. The adhesive piece Da of the dummy chips D may be completely cured at the time point of the step (A), or it is also

acceptable that the adhesive piece Da is not completely cured at this time point but is completely cured at the time point of the step (C).

[0031] [Step (B)]

Step (B) is a step of preparing the adhesive-piece-attached chip S2a illustrated in FIG. 5. The adhesive-piece-attached chip S2a comprises a chip S2 and an adhesive piece Sa provided on one surface of the chip S2. The adhesive-piece-attached chip S2a can be obtained by, for example, using a dicing-die bonding integrated film and carrying out a dicing step (see FIG. 3(a) to FIG. 3(e)).

[0032] [Step (C)]

Step (C) is a step of disposing the adhesive-piece-attached chip S2a above the chip S1 such that the adhesive piece Sa comes into contact with the top faces of the dummy chips D and the top face of the chip S1. Specifically, the chip S2 is pressure-bonded to the top faces of the dummy chips D and the top face of the chip S1, with the adhesive piece Sa interposed therebetween. It is preferable that this pressure-bonding treatment is carried out, for example, under the conditions of 80°C to 180°C and 0.01 to 0.50 MPa for 0.5 to 3.0 seconds. Next, the adhesive piece Sa is cured by heating. It is preferable that this curing treatment is carried out, for example, under the conditions of 60°C to 175°C and 0.01 to 1.0 MPa for 5 minutes or longer. Thereby, the adhesive piece Sa becomes a cured product Sc.

[0033] In the structure 30A according to the present embodiment, as described above, the height of the top face of the chip S1 coincides with the height of the top faces of the dummy chips D. Therefore, the adhesive piece Sa is in contact with both the top faces of the dummy

chips D and the top face of the chip S1. FIG. 6 is a cross-sectional view schematically illustrating the structure obtainable through step (C). Since a structure 40 illustrated in this diagram has no gap between the cured product Sc and the chip S1, the structure 40 can attain excellent filling property of the sealing material in step (D).

[0034] After step (C) and before step (D), a chip S3 is disposed on the chip S2, with an adhesive piece interposed therebetween, and a chip S4 is disposed on the chip S3, with an adhesive piece interposed therebetween. The adhesive piece may be a heat-curable resin composition similar to the above-mentioned adhesive piece Sa and becomes a cured product Sc as a result of heating and curing (see FIG. 1). Subsequently, the chips S2, S3, and S4 and the substrate 10 are respectively electrically connected with wires w. Incidentally, the number of chips to be stacked above the chip S1 is not limited to three as in the present embodiment and may be appropriately set.

[0035] [Step (D)]

Step (D) is a step of sealing the chips S1, S2, S3, and S4, the dummy chips D, and the wires w by means of a sealing material 50. Through this step, the semiconductor device 100 illustrated in FIG. 1 is completed.

[0036] (Heat-curable resin composition)

The heat-curable resin composition constituting the adhesive piece Da and the adhesive piece Sa will be described. The heat-curable resin composition according to the present embodiment is a resin composition that can go through a semi-cured (stage B) state and then enter a completely cured product (stage C) state by a subsequent

curing treatment. The heat-curable resin composition includes an epoxy resin, a curing agent, and an elastomer and further includes, as necessary, an inorganic filler, a curing accelerator, and the like.

[0037] [Epoxy resin]

5 The epoxy resin is not particularly limited so long as it is a resin that cures to acquire adhesive action. A bifunctional epoxy resin such as a bisphenol A type epoxy resin, a bisphenol F type epoxy resin, or a bisphenol S type epoxy resin; a novolac type epoxy resin such as a phenol novolac type epoxy resin or a cresol novolac type epoxy resin; or
10 the like can be used. Furthermore, a generally known resin, such as a polyfunctional epoxy resin, a glycidyl amine type epoxy resin, a heterocyclic ring-containing epoxy resin, or an alicyclic epoxy resin, can be applied. These may be used singly, or two or more kinds thereof may be used in combination.

15 [0038] [Curing agent]

 Examples of the curing agent include a phenol resin, an ester compound, an aromatic amine, an aliphatic amine, and an acid anhydride. Among these, from the viewpoints of reactivity and stability over time, a phenol resin is preferred. Examples of a
20 commercially available product of the phenol resin include PHENOLITE KA and TD series manufactured by DIC Corporation; MILEX XLC-series and XL series (for example, MILEX XLC-LL) manufactured by Mitsui Chemicals, Inc.; HE series (for example, HE100C-30) manufactured by AIR WATER INC.; and MEHC-7800
25 series (for example, MEHC-7800-4S) manufactured by Meiwa Plastic Industries, Ltd. These may be used singly, or two or more kinds

thereof may be used in combination.

[0039] Regarding the blending amounts of the epoxy resin and the phenol resin, from the viewpoint of curability, the equivalent ratio between the epoxy equivalent and the hydroxy group equivalent is preferably 0.30/0.70 to 0.70/0.30, more preferably 0.35/0.65 to 0.65/0.35, even more preferably 0.40/0.60 to 0.60/0.40, and particularly preferably 0.45/0.55 to 0.55/0.45. When the blending ratio is in the above-described range, both curability and fluidity is easily achieved at a sufficiently high level.

[0040] [Elastomer]

Examples of the elastomer include an acrylic resin, a polyester resin, a polyamide resin, a polyimide resin, a silicone resin, polybutadiene, acrylonitrile, epoxy-modified polybutadiene, maleic anhydride-modified polybutadiene, phenol-modified polybutadiene, and carboxy-modified acrylonitrile.

[0041] From the viewpoints of solubility in a solvent and fluidity, an acrylic resin is preferred as the elastomer, and an acrylic resin such as an epoxy group-containing (meth)acrylic copolymer obtained by polymerizing a functional monomer having an epoxy group or a glycidyl group as a crosslinkable functional group, such as glycidyl acrylate or glycidyl methacrylate, is more preferred. Among the acrylic resins, an epoxy group-containing (meth)acrylic acid ester copolymer and an epoxy group-containing acrylic rubber are preferred, and an epoxy group-containing acrylic rubber is more preferred. The epoxy group-containing acrylic rubber is a rubber having an epoxy group, which has an acrylic acid ester as a main component and is

formed mainly from a copolymer of butyl acrylate, acrylonitrile, and the like, a copolymer of ethyl acrylate, acrylonitrile, and the like, or the like. Incidentally, the acrylic resin may have not only an epoxy group but also a crosslinkable functional group such as an alcoholic or phenolic hydroxy group or a carboxyl group.

[0042] Examples of a commercially available product of an acrylic resin include SG-70L, SG-708-6, WS-023 EK30, SG-280 EK23, and a solvent-modified product of SG-P3 (trade name, acrylic rubber, weight average molecular weight: 800000, Tg: 12°C, solvent is cyclohexanone), all manufactured by Nagase ChemteX Corporation.

[0043] The glass transition temperature (Tg) of the acrylic resin is preferably -50°C to 50°C, and more preferably -30°C to 30°C. The weight average molecular weight (Mw) of the acrylic resin is preferably 100000 to 3000000, and more preferably 500000 to 2000000. When an acrylic resin having a Mw in this range is blended into the heat-curable resin composition, the heat-curable resin composition is easily formed into a film form, and the strength, flexibility, and tackiness in the film form is easily controlled as appropriate. In addition to this, both reflow properties and embeddability tend to be enhanced. Here, the Mw means a value measured by gel permeation chromatography (GPC) and converted using a calibration curve produced on the basis of polystyrene standards. Incidentally, when an acrylic resin having a narrow molecular weight distribution is used, there is a tendency that a highly elastic adhesive piece having excellent embeddability can be formed.

[0044] The amount of the acrylic resin to be included in the

heat-curable resin composition is preferably 20 to 200 parts by mass, and more preferably 30 to 100 parts by mass, with respect to 100 parts by mass of the sum of the epoxy resin and the epoxy resin curing agent. When the amount is in this range, control of fluidity during molding, handleability at high temperatures, and embeddability can be made further satisfactory.

[0045] [Inorganic filler]

Examples of the inorganic filler include aluminum hydroxide, magnesium hydroxide, calcium carbonate, magnesium carbonate, calcium silicate, magnesium silicate, calcium oxide, magnesium oxide, aluminum oxide, aluminum nitride, aluminum borate whiskers, boron nitride, crystalline silica, and amorphous silica. These may be used singly, or two or more kinds thereof may be used in combination.

[0046] From the viewpoint of enhancing adhesiveness, the average particle size of the inorganic filler is preferably 0.005 μm to 1.0 μm , and more preferably 0.05 to 0.5 μm . It is preferable that the surface of the inorganic filler is chemically modified, from the viewpoints of compatibility with solvents and resin components, and adhesive strength. A suitable material for chemically modifying the surface may be a silane coupling agent. Examples of the type of the functional group for the silane coupling agent include a vinyl group, an acryloyl group, an epoxy group, a mercapto group, an amino group, a diamino group, an alkoxy group, and an ethoxy group.

[0047] From the viewpoint of controlling the fluidity and fracture characteristics of the heat-curable resin composition, and the tensile modulus and adhesive force after curing, the content of the inorganic

filler with respect to 100 parts by mass of the resin components in the heat-curable resin composition is preferably 20 to 200 parts by mass, and more preferably 30 to 100 parts by mass.

[0048] [Curing accelerator]

5 Examples of the curing accelerator include imidazoles and derivatives thereof, organic phosphorus-based compounds, secondary amines, tertiary amines, and quaternary ammonium salts. From the viewpoint of appropriate reactivity, an imidazole-based compound is preferred. Examples of the imidazoles include 2-methylimidazole,
10 1-benzyl-2-methylimidazole, 1-cyanoethyl-2-phenylimidazole, and 1-cyanoethyl-2-methylimidazole. These may be used singly, or two or more kinds thereof may be used in combination.

[0049] The content of the curing accelerator in the heat-curable resin composition is preferably 0.04 to 3 parts by mass, and more preferably
15 0.04 to 0.2 parts by mass, with respect to 100 parts by mass of the sum of the epoxy resin and the epoxy resin curing agent. When the amount of addition of the curing accelerator is in this range, both curability and reliability can be achieved.

[0050] <Second embodiment>

20 According to the above-described first embodiment, an embodiment of preparing a structure 30A in which the height of the top faces of dummy chips D coincides with the height of the top face of the chip S1, in step (A) has been illustrated; however, it is also acceptable to prepare a structure in which the top faces of the dummy chips D are
25 higher than the top face of the chip S1, in step (A). A structure 30B illustrated in FIG. 7 comprises a substrate 10; a chip S1 disposed on the

substrate 10; and a plurality of dummy chips D disposed on the substrate 10 and around the chip S1, and the top faces of the dummy chips D are higher than the top face of the chip S1.

[0051] Prior to the step (D) (step of sealing with a sealing material 50)

5 of the first embodiment, it is desirable that the height of the top faces of the dummy chips D coincide with the height of the top face of the chip S1, and it is desirable that the height of the dummy chips D and the height of the top face of the chip S1 are made to coincide with each other by squashing the adhesive piece Da of the dummy chips D with
10 the adhesive-piece-attached chip S2a in step (C) (see FIG. 8). In a case where the chip S1 is mounted on the substrate 10 by flip-chip connection, a variation of about 5 μm is likely to occur in the height of the flip chip connection part, and as a result, a variation of about 5 μm is likely to occur in the height position of the top face of the chip S1.

15 There is an advantage that when this variation is predicted, and the position of the top faces of the dummy chips D is set to be slightly higher by about 8 to 12 μm than the set position of the top face of the chip S1 after connection, it is not necessary to make the height of the top faces of the dummy chips D exactly coincide with the height of the
20 top face of the chip S1 in step (A).

[0052] According to the present embodiment, the adhesive piece Da of the dummy chip D is formed of a material that is squashed with the adhesive-piece-attached chip S2a. Specifically, it is preferable that the adhesive piece Da of the dummy chip D is softer than the adhesive
25 piece Sa of the adhesive-piece-attached chip S2a. As a technique of making the adhesive piece Da softer than the adhesive piece Sa, for

example, a technique of adjusting the content of the heat-curable resin in the adhesive piece Da to be larger than that in the adhesive piece Sa, or a technique of adjusting the content of the elastomer or the inorganic filler in the adhesive piece Da to be lower than that in the adhesive piece Sa, may be mentioned.

[0053] It is preferable that the adhesive piece Da of the dummy chip D is thicker than the adhesive piece Sa of the adhesive-piece-attached chip Sa2. According to the present embodiment, for example, the thickness of the adhesive piece Da is 1.1 to 8 times the thickness of the adhesive piece Sa, and the thickness thereof may be 1.2 to 6 times.

[0054] Hereinbefore, embodiments of the present disclosure have been described in detail; however, the present invention is not intended to be limited to the above-described embodiments. For example, in the above-described embodiments, a case where the chip S1 is mounted by flip-chip connection has been illustrated; however, it is also acceptable to perform electrical connection by wire bonding after the chip S1 is fixed to the substrate 10 using an adhesive.

[0055] Hereinafter, the present disclosure will be described in detail by way of Examples; however, the present invention is not intended to be limited to these.

[0056] <Production of adhesive sheet>

Varnishes A and B of adhesive compositions were prepared by the following procedure using the components shown in Table 1. First, [Epoxy resin], [Curing agent], and [Filler] that will be described below were blended, subsequently cyclohexanone was added thereto, and the mixture was stirred. Subsequently, [Elastomer], [Curing accelerator],

and [Coupling agent] were added thereto, the resulting mixture was stirred until the various components became uniform, and thereby a varnish of an adhesive composition was obtained.

[0057] [Elastomer]

5 Acrylic rubber: trade name manufactured by Nagase ChemteX Corporation, trade name "HTR-860P-3", weight average molecular weight 800000, glass transition point: 12°C

[0058] [Epoxy resin]

 Cresol novolac type epoxy resin: manufactured by Tohto Kasei
10 Co., Ltd., trade name "YDCN-700-10", epoxy equivalent: 210

 Bisphenol F type epoxy resin: DIC Corporation, trade name "EXA-830CRP", epoxy equivalent: 159

[0059] [Curing agent]

 Phenol resin: manufactured by Mitsui Chemicals, Inc., trade
15 name "MILEX XLC-LL", softening point: 75°C, hydroxy group equivalent: 175

[0060] [Filler]

 Silica filler: manufactured by NIPPON AEROSIL CO., LTD., trade name "R972", average particle size 0.500 µm

20 Silica filler: manufactured by Admatechs Co., Ltd., trade name "SC2050-HLG", specific surface area 110 m/g

[0061] [Curing accelerator]

 1-Cyanoethyl-2-phenylimidazole CUREZOL: manufactured by SHIKOKU CHEMICALS CORPORATION, trade name "2PZ-CN"

25 [0062] [Coupling agent]

 γ-Mercaptopropyltrimethoxysilane: manufactured by Nippon

Unicar Company Limited, trade name "NUC A-189"

γ -Ureidopropyltriethoxysilane: manufactured by Nippon Unicar Company Limited, trade name "NUC A-1160"

[0063] [Table 1]

		Varnish A (parts by mass)	Varnish B (parts by mass)
Elastomer	HTR-860P-3	66	29
Epoxy resin	YDCN-700-10	13	16
	EXA-830CRP	-	14
Curing agent	XLC-LL	11	23
Filler	R972	8	-
	SC2050-HLG	-	17
Curing accelerator	2PZ-CN	0.1	0.1
Coupling agent	NUC A-189	0.4	0.1
	NUC A-1160	1.2	0.2

[0064] The varnish A was applied on a base material film (release-treated polyethylene terephthalate film, thickness: 38 μ m). The varnish was heated and dried for 5 minutes at 140°C on the base material film, and an adhesive sheet A1 (thickness 20 μ m) and an adhesive sheet A2 (thickness 40 μ m) were produced. An adhesive sheet B (thickness 40 μ m) was produced in the same manner as described above, except that the varnish B was used instead of the varnish A.

[0065] <Measurement of melt viscosity of adhesive sheet>

The melt viscosity of an adhesive sheet was measured by the following procedure using a rotary viscoelasticity analyzer (manufactured by TA Instruments Japan Inc., ARES-RDA). First, the base material film was detached from the adhesive sheet, subsequently a plurality of adhesive layers were stuck together thereto at 70°C, and a

lamine film having a thickness of 160 μm or more was obtained. A sample for measurement was obtained by punching this lamine film into a circular shape having a diameter of 8 mm and then interposing this between two sheets of jigs (diameter: 8 mm). Measurement was performed under the following conditions, and the value at 80°C was designated as the melt viscosity of the adhesive sheet. The melt viscosity of the adhesive sheets A1 and A2 was 24000 Pa·s, and the melt viscosity of the tacky adhesive sheet B was 2000 Pa·s.

- Frequency: 1 Hz

- Measurement initiation temperature: 35°C

- Measurement completion temperature: 150°C

- Rate of temperature increase: 5°C/min

[0066] (Example 1)

The adhesive sheet A1 (thickness: 20 μm) was stuck to a semiconductor wafer (thickness: 90 μm). The semiconductor wafer was singulated into semiconductor chips having a size of 5.0 mm $\times$ 5.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). One resulting semiconductor chip was thermocompression-bonded on an organic substrate that had been dried at 150°C for 1 hour, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second, and a semiconductor chip-attached substrate was obtained.

[0067] Next, the adhesive sheet B (thickness: 40 μm) was stuck to a semiconductor wafer (thickness: 80 μm). The semiconductor wafer was singulated into chips having a size of 1.5 mm $\times$ 6.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). The

above-described chips were thermocompression-bonded as dummy chips on the organic substrate on both sides of the above-described semiconductor chip with a 2-mm space, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second.

[0068] Next, HR-900T-20-N50 (manufactured by Hitachi Chemical Co., Ltd., thickness of adhesive layer: 20 μm) was stuck to a semiconductor wafer (thickness: 50 μm) with a wafer mounter (DFM-2800 manufactured by DISCO Corporation) under the conditions of 70°C and (10 mm/second). Subsequently, the semiconductor wafer was singulated into chips having a size of 6.0 mm × 12.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). One resulting chip was thermocompression-bonded on the semiconductor chip and the two dummy chips with a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 100°C to 120°C, 0.05 to 0.20 MPa, and 0.5 to 2.0 seconds. Subsequently, the adhesive was cured under the conditions of heating the adhesive at 150°C for 1 hour in a pressurized atmosphere at 7 kg. As a result, a structure comprising a substrate, two dummy chips, and two semiconductor chips was obtained.

[0069] (Comparative Example 1)

The adhesive sheet A1 (thickness: 20 μm) was stuck to a semiconductor wafer (thickness: 90 μm). The semiconductor wafer was singulated into semiconductor chips having a size of 5.0 mm × 5.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). One resulting semiconductor chip was thermocompression-bonded on

an organic substrate that had been dried at 150°C for 1 hour, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second, and a semiconductor chip-attached substrate was obtained.

5 [0070] Next, the adhesive sheet A2 (thickness: 40 μm) was stuck to a semiconductor wafer (thickness: 90 μm). The semiconductor wafer was singulated into chips having a size of 1.5 mm × 6.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). The above-described chips were thermocompression-bonded as dummy
10 chips on the organic substrate on both sides of the above-described semiconductor chip with a 2-mm space, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second.

[0071] Next, HR-900T-20-N50 (manufactured by Hitachi Chemical
15 Co., Ltd., thickness of adhesive layer: 20 μm) was stuck to a semiconductor wafer (thickness: 50 μm) with a wafer mounter (DFM-2800 manufactured by DISCO Corporation) under the conditions of 70°C and (10 mm/second). Subsequently, the semiconductor wafer was singulated into chips having a size of 6.0 mm × 12.0 mm using a
20 dicer (DFD-6361 manufactured by DISCO Corporation). One resulting chip was thermocompression-bonded on the semiconductor chip and the two dummy chips using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.10 MPa, and 1.0 second. Subsequently, the
25 adhesive was cured under the conditions of heating the adhesive at 150°C for 1 hour in a pressurized atmosphere at 7 kg. As a result, a

structure comprising a substrate, two dummy chips, and two semiconductor chips was obtained.

[0072] (Comparative Example 2)

The adhesive sheet A1 (thickness: 20 μm) was stuck to a semiconductor wafer (thickness: 90 μm). The semiconductor wafer was singulated into semiconductor chips having a size of 5.0 mm $\times$ 5.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). One resulting semiconductor chip was thermocompression-bonded on an organic substrate that had been dried at 150°C for 1 hour, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second, and a semiconductor chip-attached substrate was obtained.

[0073] Next, the adhesive sheet A1 (thickness: 20 μm) was stuck to a semiconductor wafer (thickness: 110 μm). The semiconductor wafer was singulated into chips having a size of 1.5 mm $\times$ 6.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). The above-described chips were thermocompression-bonded as dummy chips on the organic substrate on both sides of the above-described semiconductor chip with a 2-mm space, using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.1 MPa, and 1 second.

[0074] Next, HR-900T-20-N50 (manufactured by Hitachi Chemical Co., Ltd., thickness of adhesive layer: 20 μm) was stuck to a semiconductor wafer (thickness: 50 μm) with a wafer mounter (DFM-2800 manufactured by DISCO Corporation) under the conditions of 70°C and (10 mm/second). The semiconductor wafer was

singulated into chips having a size of 6.0 mm × 12.0 mm using a dicer (DFD-6361 manufactured by DISCO Corporation). One resulting chip was thermocompression-bonded on the semiconductor chip and the two dummy chips using a flexible die bonder (DB-830HSD manufactured by Hitachi High-Tech Instruments Co., Ltd.) under the conditions of 120°C, 0.10 MPa, and 1.0 second. Subsequently, the adhesive was cured under the conditions of heating the adhesive at 150°C for 1 hour in a pressurized atmosphere at 7 kg. As a result, a structure comprising a substrate, two dummy chips, and two semiconductor chips was obtained.

[0075] (Production and evaluation of semiconductor package)

A sealing material (trade name CEL-9750ZHF) manufactured by Hitachi Chemical Co., Ltd. was molded on each of the above-described structures according to Examples and Comparative Examples under the conditions of 175°C, 6.75 MPa, and 120 seconds, a curing treatment for 5 hours at 175°C was carried out, and thus semiconductor packages were obtained. The presence or absence of detachment and voids inside the semiconductor packages were observed using an ultrasonic diagnostic imaging system (manufactured by Insight k.k., Insight-300 Scanning Acoustic Microscope: SAM). Furthermore, cross-sections of the semiconductor packages thus obtained were observed, and the heights of the semiconductor chips and the dummy chips were checked.

[0076] A satisfactory case where there were no detachment and voids inside the semiconductor package was rated as "A"; and a case where there were detachment and voids was rated as "B". Furthermore, a

case where the difference between the height of the top face of the semiconductor chip and the height of the top faces of the dummy chips was less than 10 μm was rated as "A"; and a case where the difference was 10 μm or more was rated as "B". The results are presented in Table 2.

[0077] [Table 2]

	Example 1	Comparative Example 1	Comparative Example 2
Presence or absence of detachment and voids inside semiconductor package	A	B	B
Difference between height of top face of semiconductor chip and height of top faces of dummy chips	A	B	B

Industrial Applicability

[0078] According to the present disclosure, there is provided a manufacturing method for a semiconductor device having a configuration in which a first chip is mounted on a substrate and a second chip is disposed above the first chip, the manufacturing method being capable of suppressing a semiconductor device from becoming excessively thick and capable of easily performing an operation of sealing the first chip and the second chip with a sealing material. Furthermore, according to the present disclosure, a semiconductor device that is not excessively thick and has excellent filling property of the sealing material, and a structure that is used for the manufacture of this semiconductor device, are provided.

Reference Signs List

[0079] 10: substrate, 30A, 30B, 40: structure, 50: sealing material, 100: semiconductor device, D: dummy chip (spacer), D1: chip, Da: adhesive piece, S1: first chip, S2: second chip, S2a: adhesive-piece-attached chip, Sa: adhesive piece, Sc: cured product (adhesive piece).

CLAIMS

1. A manufacturing method for a semiconductor device, the manufacturing method comprising:

(A) a step of preparing a structure including a substrate, a first
5 chip disposed on the substrate, and a plurality of spacers disposed around the first chip on the substrate;

(B) a step of preparing an adhesive-piece-attached chip including a second chip having a size larger than that of the first chip, and an adhesive piece provided on one face of the second chip;

10 (C) a step of disposing the second chip above the first chip such that the adhesive piece comes into contact with top faces of the spacers; and

(D) a step of sealing the first chip, the spacers, and the second chip,

15 wherein before the step (D) is carried out, a height of the top faces of the spacers coincides with the height of a top face of the first chip.

2. The manufacturing method according to claim 1, wherein in the structure prepared in the step (A), the height of the spacers coincides
20 with the height of the top face of the first chip.

3. The manufacturing method according to claim 1 or 2, wherein the spacer is a dummy chip including a chip and an adhesive piece provided on one face of the chip.

4. The manufacturing method according to claim 1, wherein in the
25 structure prepared in the step (A), the top faces of the spacers are higher than the top face of the first chip, and

in the step (C), the height of the spacers and the height of the top face of the first chip are made to coincide with each other by squashing the spacers with the adhesive-piece-attached chip.

5. The manufacturing method according to claim 4, wherein the spacer is a dummy chip including a chip and an adhesive piece provided on one face of the chip, and

the adhesive piece included in the dummy chip is softer than the adhesive piece included in the adhesive-piece-attached chip.

6. The manufacturing method according to claim 5, wherein the adhesive piece included in the dummy chip is thicker than the adhesive piece included in the adhesive-piece-attached chip.

7. The manufacturing method according to any one of claims 1 to 6, wherein the first chip is mounted on the substrate by flip-chip connection.

8. A semiconductor device manufactured by the manufacturing method for a semiconductor device according to any one of claims 1 to 7.

9. A semiconductor device comprising:

a substrate;

a first chip disposed on the substrate;

a plurality of spacers disposed around the first chip on the substrate;

a second chip disposed above the first chip and having a size larger than that of the first chip;

an adhesive piece adhering the spacers and the second chip; and

a sealing material sealing the first chip, the spacers, and the

second chip,

wherein the adhesive piece is in contact with a top face of the first chip.

10. The semiconductor device according to claim 9, wherein the first chip is a controller chip.

11. A structure used for a manufacture of a semiconductor device, the structure comprising:

a substrate;

a first chip disposed on the substrate; and

a plurality of spacers disposed around the first chip on the substrate,

wherein a height of top faces of the spacers coincides with a height of a top face of the first chip.

12. A structure used for a manufacture of a semiconductor device, the structure comprising:

a substrate;

a first chip disposed on the substrate; and

a plurality of spacers disposed around the first chip on the substrate,

wherein top faces of the spacers are higher than a top face of the first chip, and

the spacers include a material capable of making a height of the top faces of the spacers coincide with a height of a top face of the first chip, by being squashed.

13. A structure used for a manufacture of a semiconductor device, the structure comprising:

a substrate;

a first chip disposed on the substrate;

a plurality of spacers disposed around the first chip on the substrate;

5 a second chip disposed above the first chip and having a size larger than that of the first chip; and

an adhesive piece adhering the spacers and the second chip,

wherein the adhesive piece is in contact with a top face of the first chip.

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