

SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF, MEMORY CHIP AND ELECTRONIC DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to Chinese Patent Application No. 202210709274.2, filed on June 21, 2022 and entitled "SEMICONDUCTOR STRUCTURE AND MANUFACTURING METHOD THEREOF, MEMORY CHIP AND ELECTRONIC DEVICE", the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] Embodiments of the disclosure belong to the field of semiconductors and particularly relate to a semiconductor structure and a manufacturing method thereof, a memory chip and an electronic device.

BACKGROUND

[0003] A semiconductor structure includes a plurality of memory cells, and the memory cells need to be connected to a peripheral circuit to execute a storage function. The higher the integration level of the semiconductor structure is, the greater the number of the memory cells capable of being accommodated in the semiconductor structure is, and the more excellent the performance of the semiconductor structure is. However, many spaces in the current semiconductor structure are wasted. Further, due to the limitation from physical properties, the volume of the memory cell has reached the scaling limit, and due to the limitation from process factors, it is also difficult to increase the number of stacked layers of the memory cell.

[0004] Therefore, it is an urgent need of a semiconductor structure with a new

architecture to improve the integration level of the semiconductor structure.

SUMMARY

[0005] Embodiments of the disclosure provide a semiconductor structure and a manufacturing method thereof, a memory chip and an electronic device, which at least contributes to improving the integration level of the semiconductor structure.

[0006] According to some embodiments of the disclosure, on the one hand, the embodiments of the disclosure provide a semiconductor structure. The semiconductor structure includes: a substrate, on which a stacked structure is provided, where the stacked structure includes a plurality of memory cell groups arranged in a first direction, each of the memory cell groups including multiple layers of memory cells arranged in a second direction, and the stacked structure further includes a plurality of horizontal signal lines arranged in the second direction, and each of the horizontal signal lines is in contact with one layer of the memory cells; and a plurality of leading wire posts arranged in the first direction, where the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are contacted with the horizontal signal lines.

[0007] According to some embodiments of the disclosure, on the other hand, the embodiments of the disclosure provide a semiconductor structure. The semiconductor structure includes: a substrate, on which a stacked structure is provided, where the stacked structure includes a plurality of memory cell groups arranged in a first direction, each of the memory cell groups including multiple layers of memory cells arranged in a second direction, and the stacked structure further includes a plurality of horizontal signal lines arranged in the second direction, where each of the horizontal signal lines is in contact with one layer of the memory cells; and a plurality of leading wire posts arranged in the first direction and extending along the second direction, where orthographic projections of the plurality of leading wire posts on the surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are contacted with the horizontal

signal lines.

[0008] According to some embodiments of the disclosure, on the other hand, the embodiments of the disclosure provide a method for manufacturing a semiconductor structure. The method includes the following operations. A substrate is provided. A stacked structure is formed on the substrate. The stacked structure includes a plurality of memory cell groups arranged in a first direction, each of the memory cell groups including multiple layers of memory cells arranged in a second direction, and the stacked structure further includes a plurality of horizontal signal lines arranged in the second direction, where each of the horizontal signal lines is in contact with one layer of the memory cells. A plurality of leading wire posts arranged in the first direction is formed. The plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are contacted with the horizontal signal lines.

[0009] According to some embodiments of the disclosure, on the other hand, the embodiments of the disclosure provide a method for manufacturing a semiconductor structure. The method includes the following operations. A substrate is provided. A stacked structure is formed on the substrate. The stacked structure includes a plurality of memory cell groups arranged in a first direction, each of the memory cell groups including multiple layers of memory cells arranged in a second direction, and the stacked structure further includes a plurality of horizontal signal lines arranged in the second direction, where each of the horizontal signal lines is in contact with one layer of the memory cells. A plurality of leading wire posts arranged in the first direction and extending along the second direction is formed, where orthographic projections of the plurality of leading wire posts on the surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are contacted with the horizontal signal lines.

[0010] According to some embodiments of the disclosure, the embodiments of the disclosure further provide a memory chip. The memory chip includes the aforementioned semiconductor structures.

[0011] According to some embodiments of the disclosure, the embodiments of the disclosure further provide an electronic device. The electronic device includes the aforementioned memory chip.

[0012] Technical solutions provided by the embodiments of the disclosure at least have the following advantages.

[0013] In some embodiments of the disclosure, the stacked structure includes a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines is contacted with one layer of memory cells in the stacked structure, the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are contacted with the horizontal signal lines. That is, in the third direction, the leading wire posts are directly connected to the horizontal signal lines, so that it contributes to reducing the number of staircases or it is no longer to arrange a staircase area independently, thereby improving the integration level of the semiconductor structure.

[0014] In some other embodiments of the disclosure, the plurality of leading wire posts extend along the second direction, and orthographic projections of the plurality of leading wire posts on the surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped. That is, the leading wire posts are directly connected to the horizontal signal lines in an alternative manner, so that it contributes to reducing the number of staircases or it is no longer to arrange a staircase area independently, thereby improving the integration level of the semiconductor structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments consistent with the disclosure and, together with the description, serve to explain the principles of the disclosure. It is apparent that the accompanying drawings described below are merely some embodiments of the disclosure, and other drawings can be obtained by those of ordinary skill in the art

according to these accompanying drawings without creative efforts.

- [0016] FIG. 1 illustrates a top view of a semiconductor structure.
- [0017] FIG. 2 illustrates a partial enlarged drawing of FIG. 1.
- [0018] FIG. 3 illustrates a section view of FIG. 2 in the direction A-A1.
- [0019] FIG. 4-FIG. 5 respectively illustrate stereograms of two semiconductor structures provided by an embodiment of the disclosure.
- [0020] FIG. 6-FIG. 10 respectively illustrate different partial side views of a semiconductor structure provided by an embodiment of the disclosure.
- [0021] FIG. 11-FIG. 13 and FIG. 24 respectively illustrate different partial section views of a semiconductor structure provided by an embodiment of the disclosure.
- [0022] FIG. 14-FIG. 23 and FIG. 25-FIG. 28 respectively illustrate different top views of a semiconductor structure provided by an embodiment of the disclosure.
- [0023] FIG. 29-FIG. 30 respectively illustrate stereograms of two semiconductor structures provided by another embodiment of the disclosure.
- [0024] FIG. 31, FIG. 32, FIG. 34 and FIG. 36 respectively illustrate different section views of a semiconductor structure provided by another embodiment of the disclosure.
- [0025] FIG. 33 illustrates a partial enlarged drawing of FIG. 32.
- [0026] FIG. 35 illustrates a partial enlarged drawing of FIG. 34.
- [0027] FIG. 37 illustrates a partial enlarged drawing of FIG. 36.
- [0028] FIG. 38-FIG. 44 respectively illustrate different top views of a semiconductor structure provided by another embodiment of the disclosure.
- [0029] FIG. 45-FIG. 56 illustrate schematic structural diagrams corresponding to operations of a method for manufacturing a semiconductor structure provided by another embodiment of the disclosure.

[0030] FIG. 57-FIG. 60 illustrate schematic structural diagrams corresponding to operations of a method for manufacturing a semiconductor structure provided by another embodiment of the disclosure.

DETAILED DESCRIPTION

[0031] FIG. 1 is a top view of a semiconductor structure. FIG. 2 is an enlarged drawing of a staircase in a dotted circle in FIG. 1. FIG. 3 is a section view of FIG. 2 in the direction A-A1. Referring to FIG. 1 to FIG. 3, the semiconductor structure includes a memory cell area 100 and a staircase area 200. There are multiple layers of memory cells in the memory cell area 100. There are multiple staircases in the staircase area 200, and the staircases and the memory cells are arranged in one-to-one correspondence. A connecting layer (not shown in the drawing) can be arranged in the staircase, a leading wire post 300 can be arranged on the staircase, and the leading wire post 300 are electrically contacted with the memory cell through the connecting layer in the staircase, so as to lead out the memory cell, so that it is convenient to connect the memory cell to a peripheral circuit. However, with increase of stacked layers of the memory cells, the area occupied by the staircase area 200 will be larger and larger. For example, if there are totally 64 layers of memory cells, correspondingly, 64 staircases are needed, and the lower the staircase is, the larger the area is. If the area of the topmost staircase is $0.25\mu\text{m}^2$, the area of the bottommost staircase is $64 \times 0.25 = 16\mu\text{m}^2$. Referring to FIG. 3, the connecting layer below each staircase only provides support and electric connection, so that the bottom space is wasted. Therefore, the integration level of the semiconductor structure needs to be further improved.

[0032] The embodiments of the disclosure provide a semiconductor structure. In such semiconductor structure, the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along the third direction, and the leading wire posts and the horizontal signal lines are connected; alternatively, the plurality of leading wire posts extend along the second direction, and orthographic projections of the plurality of leading wire posts on the surface of the substrate are at least partially overlapped with orthographic projections of the horizontal signal lines on the surface of the substrate.

That is, the leading wire posts and the horizontal signal lines are directly connected in a parallel manner or an alternative manner. Therefore, it is unnecessary to connect the leading wire posts to the horizontal signal lines through a connection layer in the staircase area, so that the space utilization ratio in the semiconductor structure is improved, thereby improving the integration level of the semiconductor structure.

[0033] The embodiments of the disclosure will be described below in detail in combination with the drawings. However, those of ordinary skill in the art may understand that many technical details are provided to better understand the disclosure in the embodiments of the disclosure. However, the technical solutions claimed by the disclosure may also be implemented even though there are no these technical details and various changes and modifications based on the following embodiments.

[0034] As shown in FIG. 4-FIG. 28, an embodiment of the disclosure provide a semiconductor structure. The semiconductor structure includes: a substrate (not shown in the drawings), on which a stacked structure is provided, the stacked structure includes a plurality of memory cell groups TC0 arranged in the first direction X, and each of the memory cell groups TC0 includes multiple layers of memory cells TC arranged in a second direction Z, and the stacked structure further includes a plurality of horizontal signal lines 3 arranged in the second direction Z, and each of the horizontal signal lines 3 is contacted with one layer of the memory cells TC; and a plurality of leading wire posts 5 arranged in a first direction X, the plurality of leading wire posts 5 and the plurality of horizontal signal lines 3 are arranged along a third direction Y, and the leading wire posts 5 are contacted with the horizontal signal lines 3.

[0035] That is, the edge of the orthographic projection of the leading wire post 5 on the surface of the substrate is in contact with the edge of the orthographic projection of the horizontal signal line 3 on the surface of the substrate. In other words, at least part of side walls of the leading wire post 5 is directly contacted with a side wall of the horizontal signal line 3, and it is unnecessary to connect indirectly through the connection layer of the staircase area, so that the numbers of the connection layers and the staircases may be decreased, thereby facilitating to improve the integration level of the semiconductor structure.

[0036] The semiconductor structure will be described below in detail in combination with the drawings.

[0037] It is to be noted first that FIG. 6-FIG. 10 are partial top views. For a more intuitive purpose, FIG. 6-FIG. 9 do not illustrate a structure for isolating and supporting the leading wire post 5 in the semiconductor structure. FIG. 10 illustrates the structure for isolating and supporting the leading wire post 5.

[0038] In some embodiments, referring to FIG. 6-FIG. 10, each horizontal signal line 3 is at least contacted with one leading wire post 5. That is, each horizontal signal line 3 may be directly contacted with the leading wire post 5, so as to be led out by the leading wire post 5. Therefore, it may be unnecessary to arrange the staircase area independently, so that the space utilization ratio of the semiconductor structure can be improved to a great extent, and it contributes to simplifying the production process.

[0039] Exemplarily, referring to FIG. 6-FIG. 8, the plurality of horizontal signal lines 3 are contacted with the plurality of leading wire posts 5 in one-to-one correspondence. That is, each horizontal signal line 3 is contacted with one leading wire post 5, so as to reduce the connection positions between the horizontal signal lines 3 and the leading wire posts 5, and make the production process simpler. In some other embodiments, referring to FIG. 9, one horizontal signal line 3 may also be contacted with the plurality of leading wire posts 5, so that the contact regions between the horizontal signal line 3 and the leading wire posts 5 may be increased, and the contact resistance is reduced.

[0040] In some embodiments, referring to FIG. 4-FIG. 13, the leading wire posts 5 extend along the second direction Z. That is, the plurality of leading wire posts 5 are parallel one another, and the extension directions of the leading wire posts 5 are the same as the stacking direction of the memory cells TC, which contributes to simplifying the process and improving the uniformity of the semiconductor structure. Exemplarily, the stacking direction of the memory cells TC is the second direction Z which is perpendicular to the surface of the substrate.

[0041] Referring to FIG. 4-FIG. 11, it is to be noted that with respect to the leading wire post 5 contacted with the horizontal signal line 3 of the non-top layer, the leading

wire post 5 may be arranged adjacent to multiple layers of horizontal signal lines 3. It may be known based on a leading function of the leading wire posts 5 that, each leading wire post 5 is only connected to one horizontal signal line 3, rather than two horizontal signal lines 3 at the same time. Otherwise, signal disturbance occurs. In order to facilitate understanding, the horizontal signal line 3 connected to the leading wire post 5 is called as the horizontal signal line 3 of the corresponding layer. The leading wire post 5 is arranged to be insulated from horizontal signal lines 3, except the horizontal signal line 3 of the corresponding layer. In addition, the leading wire post 5 is divided into a contact portion 51 and an extension portion 52 arranged in a stacked manner. The contact portion 51 and the horizontal signal line 3 of the corresponding layer are arranged in the same layer and are connect to each other. The extension portion 52 is arranged adjacent to the horizontal signal line 3 above the corresponding layer, but insulated from the horizontal signal line.

[0042] Correspondingly, referring to FIG. 5-FIG. 13, the stacked structure may further include a dielectric layer 6. The dielectric layer 6 is at least located on a side wall of the leading wire post 5 facing the horizontal signal line 3 above the corresponding layer, and the lower surface of the dielectric layer 6 is higher than the horizontal signal line 3 connected to the leading wire post 5. That is, the dielectric layer 6 is used for isolating the leading wire post 5 from the horizontal signal lines 3 out of the corresponding layer, so as to avoid incorrect electrical connections. Specifically, the dielectric layer 6 may encircle the side walls of the extension portion 52 of the leading wire post 5. A material of the dielectric layer 6 may be a material with a low dielectric constant, such as silicon nitride or silicon oxide.

[0043] In some embodiments, referring to FIG. 4-FIG. 10, the leading wire posts 5 connected to different horizontal signal lines 3 are different in length in the second direction Z, and the bottoms of the leading wire posts 5 are contacted with the horizontal signal lines 3. Exemplarily, the leading wire post 5 connected to the horizontal signal line 3 of the top layer is the shortest in the second direction Z, and the leading wire post 5 connected to the horizontal signal line 3 of the bottom layer is the shortest in the second direction Z, which contributes to saving the material, so as to further reduce the production cost, and further contributes to simplifying the production process. In some

other embodiments, the leading wire posts 5 may be same in length, but the leading wire posts 5 are only connected to the horizontal signal lines 3 of the corresponding layer and are arranged to be insulated from the horizontal signal lines 3 above and below the corresponding layer.

[0044] In order to increase the contact region between the leading wire post 5 and the horizontal signal line 3 to decrease the contact resistance, the bottom surface of the leading wire post 5 may be aligned with the bottom surface of the horizontal signal line 3 of the corresponding layer; alternatively, the bottom surface of the leading wire post 5 may be slightly lower than the bottom surface of the horizontal signal line 3 of the corresponding layer. In some other embodiments, the bottom surface of the leading wire post 5 may be higher than the bottom surface of the horizontal signal line 3 of the corresponding layer, but lower than the top surface of the horizontal signal line 3 of the corresponding layer.

[0045] In some embodiments, referring to FIG. 6-FIG. 7, the adjacent leading wire posts 5 are arranged at an equal spacing in the first direction X. That is, the spacing between the adjacent leading wire posts 5 is the same, so that the uniformity of the semiconductor structure is improved.

[0046] Referring to FIG. 6, the leading wire posts 5 may be arranged in the order of the length magnitude in the second direction Z. In some other embodiments, referring to FIG. 7, the lengths of the leading wire posts 5 may not be increased or decreased progressively but alternative in length, so that a large parasitic capacitance is prevented from being generated between the longer leading wire posts 5.

[0047] In some other embodiments, referring to FIG. 8, a spacing between the adjacent leading wire posts 5 is in proportion to an area of a directly facing region. It is to be noted that the area of the directly facing region between the adjacent leading wire posts 5 is in proportion to the magnitude of the parasitic capacitance. Therefore, in a case that the area of the directly facing region between the adjacent leading wire posts 5 is large, the spacing between the leading wire posts may be correspondingly increased to reduce the parasitic capacitance.

[0048] In some embodiments, referring to FIG. 10-FIG. 12, the stacked structure further includes multiple etching barrier layers 13 arranged in the second direction Z, and each etching barrier layer 13 is contacted with a bottom surface of at least one leading wire post 5. Specifically, a method for forming the leading wire post 5 includes: forming a through hole 8 (referring to FIG. 53) in one side of the horizontal signal line 3 by adopting an etching process, and depositing a conductive material in the through hole 8 to form the leading wire post 5. Therefore, the position of the through hole 8 decides the position of the leading wire post 5. The etching barrier layer 13 may stop etching to realize a self-aligning function, so as to avoid the problem of over-etching or insufficient etching of the through hole 8. That is to say, the etching barrier layers 13 and isolation layers 14 are alternatively arranged in the second direction Z, the etching barrier layer 13 directly faces a gap between the two adjacent horizontal signal lines 3, the isolation layer 14 and the horizontal signal line 3 are arranged in the same layer, and the etch selectivity ratio of the isolation layer 14 to the etching barrier layer 13 is large. Exemplarily, a material of the isolation layer 14 may be silicon oxide, and a material of the etching barrier layer 13 may be silicon nitride. In addition, the etching barrier layer 13 may also provide an isolating function.

[0049] In some other embodiments, referring to FIG. 13, only the isolation layer 14 may be arranged on one side of the horizontal signal line 3, and no etching barrier layer 13 is arranged. Correspondingly, in the process of forming the through hole 8, the depth of the through hole 8 is controlled by means of an etching time. Therefore, only one etching agent may be used, thereby simplifying the manufacturing process.

[0050] Referring to FIG. 4-FIG. 5 and FIG. 11-FIG. 28, the memory cell TC includes a channel region 22 and source/drain doped regions 21 arranged in the third direction Y, and the source/drain doped regions 21 are located on two sides of the channel region 22. That is, the memory cell TC at least includes a transistor T. In some other embodiments, the memory cell TC may further include a capacitor C. The transistor T and the capacitor C are arranged in the third direction Y. Exemplarily, in a Dynamic Random Access Memory (DRAM), the memory cell TC includes a transistor T and a capacitor C. In some other embodiments, the memory cell TC may only include the transistor T. For example, in a Static Random-Access Memory (SRAM), the memory cell TC is composed of six

transistors T. For another example, a Capacitorless Double Gate Quantum Well Single Transistor (1T DRAM), the memory cell TC is composed of one dual gate transistor T.

[0051] Referring to FIG. 4-FIG. 5, the stacked structure further includes perpendicular signal lines 4 extending along the second direction Z and contacted with multiple layers of memory cells TC of the same memory cell group TC0. One of the horizontal signal line 3 and the perpendicular signal line 4 is a bit line (BL), and the other of the horizontal signal line 3 and the perpendicular signal line 4 is a word line (WL). The BL is contacted with the source/drain doped region 21, and the WL is contacted with the channel region 22. The source/drain doped region 21 contacted with the BL is called as the first source/drain doped region 211, and the source/drain doped region 21 arranged spaced from the BL is called as the second source/drain doped region 212.

[0052] Position relationships between the horizontal signal lines 3 and the leading wire posts 5 will be described below in detail in two situations: the horizontal signal lines are BLs and the horizontal signal lines are WLs.

[0053] In a case that the horizontal signal lines 3 are BLs, the horizontal signal lines 3 and the leading wire posts 5 mainly have the following several position relationships.

[0054] In example 1, referring to FIG. 14-FIG. 18, the leading wire post 5 and the memory cell TC are respectively located on two opposite sides of the horizontal signal line 3 arranged in the third direction Y, that is, the leading wire post 5 is located on the side of the horizontal signal line 3 away from the memory cell TC. Therefore, it may be more flexible to set arrangement positions and dimensions of the leading wire posts 5.

[0055] Specifically, referring to FIG. 14, in some embodiments, the leading wire post 5 directly faces the memory cell group TC0 in the third direction Y, which contributes to improving the uniformity of position arrangement. In some other embodiments, referring to FIG. 15, the leading wire posts 5 and the memory cell groups TC0 are arranged alternatively in the first direction X, that is, the leading wire post 5 directly faces the space between adjacent memory cell groups TC0. In some other embodiments, referring to FIG. 16, the leading wire post 5 is arranged simultaneously opposite the memory cell group TC0 and the space between the adjacent memory cell groups TC0. In some other

embodiments, referring to FIG. 17, a part of leading wire posts 5 directly faces the space between adjacent memory cells TC0, and part of leading wire posts 5 directly faces the memory cell group TC0.

[0056] Continuously referring to FIG. 14-FIG. 17, in order to reduce the parasitic capacitance between the adjacent leading wire posts 5, the gap between the adjacent leading wire posts 5 may be arranged opposite at least one memory cell group TC0. In addition, referring to FIG. 14-FIG. 16, in order to increase the uniformity of the semiconductor structure, the spacings between the adjacent leading wire posts 5 may be the same. In addition, referring to FIG. 17, the spacings between the adjacent leading wire posts 5 may be adjusted according to different areas of the directly facing regions, so as to balance the parasitic capacitance among different leading wire posts 5.

[0057] In some embodiments, referring to FIG. 14-FIG. 17, the width of the leading wire post 5 in the first direction X is equal to the width of the memory cell group TC0, so that it contributes to unifying characteristic sizes of different structures, so as to simplify the production process. In some other embodiments, referring to FIG. 18, the width of the leading wire post 5 in the first direction X is greater than the width of the memory cell group TC0, so that it contributes to increasing the contact region between the leading wire post 5 and the horizontal signal line 3 of the corresponding layer, so as to reduce the contact resistance.

[0058] In addition, the width of the leading wire post 5 in the first direction X may be greater than or equal to the spacing between adjacent memory cell groups TC0. Such arrangement contributes to increasing the contact region between the leading wire post 5 and the horizontal signal line 3 of the corresponding layer, so as to reduce the contact resistance.

[0059] In addition, referring to FIG. 18, the width of the leading wire post 5 in the first direction X is greater than the width of the leading wire post 5 in the third direction Y. It is to be noted that the horizontal signal line 3 has a long length in the first direction X, and thus the leading wire post 5 has an enough accommodation space in the first direction X. In order to improve the utilization ratio of a semiconductor space while increasing the cross sectional areas of the leading wire posts 5, the leading wire posts 5

may be arranged in the first direction X and the third direction Y with certain width differences.

[0060] In example 2, referring to FIG. 19-FIG. 20, the leading wire post 5 and the memory cell TC are located on the same side of the horizontal signal line 3. That is, the leading wire post 5 is located between adjacent memory cell groups TC0. Therefore, it contributes to making full use of the space position in the stacked structure, thereby improving the space utilization ratio.

[0061] Continuously referring to FIG. 19-FIG. 20, in order to reduce the parasitic capacitance between adjacent leading wire posts 5, the adjacent leading wire posts 5 may be spaced by at least two memory cell groups TC0. In addition, referring to FIG. 19, in order to increase the uniformity of the semiconductor structure, the number of the memory cell groups TC0 spaced between the adjacent leading wire posts 5 may be the same. In addition, referring to FIG. 20, the number of the memory cell groups TC0 spaced between the adjacent leading wire posts 5 may be adjusted according to different areas of the directly facing regions, so as to balance the parasitic capacitance among different leading wire posts 5.

[0062] In some embodiments, referring to FIG. 19-FIG. 20, the width of the leading wire post 5 in the third direction Y is greater than the width of the leading wire post 5 in the first direction X. Therefore, not only can the spacing between the adjacent memory cell groups TC0 be reduced, so as to reduce the area occupied by the stacked structure on the surface of the substrate, but also the cross sectional area of the leading wire post 5 can be increased, so as to reduce the contact resistance of the leading wire post 5. In some other embodiments, the width of the leading wire post 5 in the third direction Y may be equal to the width of the leading wire post 5 in the first direction X.

[0063] It is to be noted that the example 1 and example 2 may be combined, that is, part of leading wire posts 5 is located on one side of the horizontal signal line 3 and the other part of leading wire posts 5 is located on the other side of the horizontal signal line 3.

[0064] In some embodiments, referring to FIG. 14-FIG. 20, there is one memory cell

in each layer of the memory cell group TC0. In another embodiment, referring to FIG. 21-FIG. 22, there are two memory cells TC in each layer of the memory cell group TC0, and two memory cells TC are respectively located in two opposite sides of the horizontal signal line 3 arranged in the third direction Y. Since the number of the memory cells TC in the memory cell group TC0 is increased, the storage capacity of the semiconductor is correspondingly enhanced.

[0065] In some embodiments, referring to FIG. 21, part of leading wire posts 5 may be located between adjacent memory cells TC0 of a stacked structure, and part of leading wire posts 5 may be located between adjacent memory cells TC0 of another stacked structure. That is, a plurality of leading wire posts 5 are located on two different sides of the horizontal signal line 3. For example, adjacent leading wire posts 5 are located on different sides of the horizontal signal line 3. In other words, two adjacent leading wire posts 5 are staggered in the first direction X, so that the parasitic capacitance may be reduced.

[0066] In some other embodiments, referring to FIG. 22, all the leading wire posts 5 are located on the same side of the horizontal signal line 3, so that it contributes to improving the uniformity of the arrangement mode of the leading wire posts 5, so as to simplify the manufacturing process of the semiconductor.

[0067] It is to be noted that in some embodiments, one leading wire post 5 may only be used for leading out one horizontal signal line 3 of one stacked structure. In some other embodiments, one leading wire post 5 may be shared by two stacked structures. Specifically, referring to FIG. 23-FIG. 24, FIG. 23 is a top view, and FIG. 24 is a section view of FIG. 23 in the third direction Y. The horizontal signal lines 3 of two adjacent stacked structures are arranged opposite. The leading wire post 5 is located between the horizontal signal lines 3 of the adjacent stacked structures, and the horizontal signal lines 3 of the same layer of the adjacent stacked structures are electrically connected through at least one leading wire post 5. Since the leading wire post 5 may be shared by two stacked structures, the number of the leading wire posts 5 may be decreased, so that it contributes to reducing the volume of the semiconductor structure.

[0068] It is to be noted that although the horizontal signal lines 3 of two stacked

structures are electrically connected, the memory cells TC corresponding to the horizontal signal lines 3 are still controlled by different WLs, and therefore, the memory cells TC of the two stacked structures can still be controlled independently.

[0069] In a case that the horizontal signal lines 3 are WLs, the horizontal signal lines 3 and the leading wire posts mainly have the following several position relationships.

[0070] First, it is to be noted that there are various position relationships between the WL and the channel region 22. For example, the WL may cover the entire channel region 22. Alternatively, the WL(s) may be contacted with the top surface and/or the bottom surface of the channel region 22. If the WL covers the entire channel region 22, the area of the side wall of the WL is larger. Since the side wall of the WL is contacted with a side wall of the leading wire post 5, the larger area of the side wall of the WL is beneficial to increasing the contact region between the WL and the leading wire post 5, thereby reducing the contact resistance. In a case that the WLs are located on the top surface and the bottom surface of the channel region 22, in order to increase the contact regions, the leading wire posts 5 may be simultaneously contacted with the WLs on the top surface and the bottom surface of the channel region 22.

[0071] In some other embodiments, referring to FIG. 25-FIG. 27, all the leading wire posts 5 are located on the same side of the horizontal signal line 3, so that it contributes to improving the uniformity of the arrangement of the leading wire posts 5, so as to simplify the manufacturing process of the semiconductor. Exemplarily, referring to FIG. 25, all the leading wire posts 5 are located on the side of the horizontal signal line 3 close to the first source/drain doped region 211. Referring to FIG. 26-FIG. 27, all the leading wire posts 5 are located on the side of the horizontal signal line 3 close to the second source/drain doped region 212.

[0072] Referring to FIG. 25-FIG. 27, in order to reduce the parasitic capacitance, the adjacent leading wire posts 5 may be spaced at least by two memory cell groups TC0. In addition, referring to FIG. 25 and FIG. 26, in order to increase the uniformity of the semiconductor structure, the number of memory cell groups TC0 between the adjacent leading wire posts 5 may be the same. Alternatively, referring to FIG. 27, the number of the memory cell groups TC0 spaced between the adjacent leading wire posts 5 may be

adjusted according to different areas of the directly facing regions, so as to balance the parasitic capacitance among different leading wire posts 5.

[0073] In some other embodiments, referring to FIG. 28, part of leading wire posts 5 may be located on one side of the horizontal signal line 3 and part of leading wire posts 5 may be located on the other side of the horizontal signal line 3. Exemplarily, adjacent leading wire posts 5 are located on different sides of the horizontal signal line 3, that is, the leading wire posts 5 may be staggered in the first direction X, so that the parasitic capacitance is reduced.

[0074] In an embodiment of the disclosure, the plurality of leading wire posts 5 and the plurality of horizontal signal lines are arranged along the third direction Y, and the leading wire posts 5 are connected to the horizontal signal lines 3. That is, an edge of the orthographic projection of the leading wire posts 5 on the surface of the substrate is in contact with an edge of the orthographic projection of the horizontal signal line 3 on the surface of the substrate. Since the leading wire posts 5 are directly connected to the horizontal signal lines 3, the numbers of the connection layers and the staircases may be decreased, thereby improving the integration level of the semiconductor structure.

[0075] As shown in FIG. 29-FIG. 44, another embodiment of the disclosure provides a semiconductor structure. The semiconductor structure is substantially same as the semiconductor structure in the aforementioned embodiments. The main difference lies in that orthographic projections of the plurality of leading wire posts 5 of the semiconductor structure on the surface of the substrate are at least partially overlapped with orthographic projections of the horizontal signal lines 3 on the surface of the substrate. Parts of the semiconductor structure same as or similar to the semiconductor structure in the aforementioned embodiments refer to detailed description in the aforementioned embodiments, which is not elaborated herein.

[0076] The semiconductor structure includes: a substrate (not shown in the drawings), on which a stacked structure is provided, and the stacked structure includes a plurality of memory cell groups TC0 arranged in the first direction X, and each of the memory cell groups TC0 includes multiple layers of memory cells TC arranged in the second direction Z, and the stacked structure further includes a plurality of horizontal signal lines 3

arranged in the second direction Z, and each of the horizontal signal lines 3 is contacted with one layer of the memory cells TC; a plurality of leading wire posts 5 arranged in the first direction X and extending along the second direction Z, and orthographic projections of the plurality of leading wire posts 5 on the surface of the substrate are at least partially overlapped with orthographic projections of the horizontal signal lines 3 on the surface of the substrate, and the leading wire posts 5 are connected to the horizontal signal lines 3.

[0077] That is, the leading wire posts 5 are directly connected to the horizontal signal lines 3 in an alternative manner by at least utilizing the space positions of part of the horizontal signal lines 3, so that it contributes to reducing the number of staircases or it is no longer to arrange a staircase area independently, thereby improving the integration level of the semiconductor structure.

[0078] The semiconductor structure will be described below in detail in combination with the drawings.

[0079] Referring to FIG. 29-FIG. 37, the leading wire post 5 is located on the top surface of the horizontal signal line 3 of the corresponding layer, and the bottom surface of the leading wire post 5 is contacted with the top surface of the horizontal signal line 3 of the corresponding layer. In some other embodiments, the bottom of the leading wire post 5 may be embedded into the horizontal signal line 3 of the corresponding layer; alternatively, the bottom of the leading wire post 5 may penetrate through the horizontal signal line 3 of the corresponding layer, that is, the side wall of the leading wire post 5 may also be contacted with the horizontal signal line 3 of the corresponding layer.

[0080] Referring to FIG. 29-FIG. 30, FIG. 32, FIG. 34 and FIG. 36, at least one leading wire post 5 penetrates through at least one horizontal signal line 3, that is, at least one of the leading wire posts 5 is connected to the horizontal signal line 3 of the non-top layer. It is to be noted that the leading wire post 5 connected to the horizontal signal line 3 of the non-top layer needs to occupy, besides the space position of the horizontal signal line 3 of the corresponding layer, the space position of the horizontal signal line 3 above the corresponding layer. Therefore, the leading wire post 5 will penetrate through the horizontal signal line 3 located above the corresponding layer. Referring to FIG. 31, with respect to the leading wire post 5 connected to the horizontal signal line 3 of the top layer,

the leading wire post 5 does not need to penetrate through the horizontal signal lines 3 out of the corresponding layer.

[0081] It is to be noted that the leading wire post 5 penetrates through the horizontal signal line 3 located above the corresponding layer 5, but the horizontal signal line 3 above the corresponding layer is not truncated completely.

[0082] Specifically, referring to FIG. 29-FIG. 44, the horizontal signal line 3 includes a contact region 31 and an exposed region 32 arranged in the third direction Y; the leading wire post 5 is connected to the contact region 31, and the exposed region 32 is exposed; and the third direction Y is perpendicular to the second direction Z and parallel to the surface of the substrate. That is to say, the leading wire post 5 is contacted with the contact region 31 of the horizontal signal line 3 of the corresponding layer and penetrates through the contact region 31 of the horizontal signal line 3 located above the corresponding layer, and the exposed regions 32 of all the horizontal signal lines 3 are exposed. Although the horizontal signal line 3 above the corresponding layer is penetrated, the horizontal signal line 3 will not be completely truncated since the exposed regions 32 are reserved, and the horizontal signal line 3 may still be contacted with the memory cell TC of the same layer.

[0083] In some embodiments, referring to FIG. 32-FIG. 33, FIG. 33 illustrates a partial enlarged drawing of the horizontal signal line 3 of the corresponding layer and the leading wire post 5 in FIG. 32. The exposed regions 32 are located on two opposite sides of the contact region 31. The orthographic projection of the leading wire post 5 on the surface of the substrate is overlapped with the orthographic projection of the contact region 31 on the surface of the substrate. That is to say, the contact region 31 is located in a center position of the horizontal signal line 3, the leading wire post 5 is connected to the center of the horizontal signal line 3 of the corresponding layer and penetrates through the center of the horizontal signal line 3 located above the corresponding layer, the exposed regions 32 of the horizontal signal line 3 are not truncated, and the horizontal signal line 3 may still be contacted with the memory cells TC of the same layer.

[0084] In some other embodiments, referring to FIG. 34-FIG. 38, FIG. 35 illustrates a partial enlarged drawing of the horizontal signal line 3 of the corresponding layer and the

leading wire post 5 in FIG. 34, FIG. 37 illustrates a partial enlarged drawing of the horizontal signal line 3 of the corresponding layer and the leading wire post 5 in FIG. 36, and FIG. 38 is a top view of the semiconductor structure shown in FIG. 36. The horizontal signal line 3 has two opposite sides arranged in the third direction Y, the exposed region 32 is located on one of the two opposite sides, and the contact region 31 is located on the other of the two opposite sides. That is, the leading wire post 5 is contacted with one side of the horizontal signal line 3 of the corresponding layer and the other side of the horizontal signal line 3 is exposed, the leading wire post 5 penetrates through one side of the horizontal signal line 3 above the corresponding layer, and the other side of the horizontal signal line 3 above the corresponding layer is not penetrated.

[0085] In an example, referring to FIG. 34-FIG. 35, the orthographic projection of the leading wire post 5 on the surface of the substrate is overlapped with the orthographic projection of the exposed region 32 on the surface of the substrate. That is, in the direction parallel to the substrate, the leading wire post 5 utilizes the space position of the horizontal signal line 3 and does not exceed the horizontal signal line 3, so that it contributes to improving the compact degree between the leading wire post 5 and the horizontal signal line 3, so as to improve the space utilization ratio.

[0086] In another example, referring to FIG. 36-FIG. 38, the leading wire post 5 is protruded relative to the contact region 31. That is, the leading wire post 5 is protruded relative to one side of the horizontal signal line 3. That is to say, only part of the bottom surface of the leading wire post 5 is in contact connection with the contact region 31. Protruding arrangement may reduce the area of the horizontal signal line 3 above the corresponding layer penetrated by the leading wire post 5, so that the resistance of the horizontal signal line 3 above the corresponding layer is reduced. Meanwhile, it may further guarantee that the leading wire post 5 has a large cross sectional area, so that the resistance of the leading wire post 5 is reduced.

[0087] It is to be noted that in some embodiments, the horizontal signal line 3 may be strip-like, that is, the orthographic projection of the horizontal signal line 3 on the surface of the substrate is rectangular. In some other embodiments, the horizontal signal line 3 may include a main body portion and a protrusion portion connected with each other. The

main body portion is strip-like, and the protrusion portion may be in shapes such as square or zigzag, that is, the length of the protrusion portion in the first direction X is smaller than the length of the main body portion in the first direction X. The main body portion and the protrusion portion may be arranged in the third direction Y. The main body portion is contacted with the memory cell group TC0, and the protrusion portion is contacted with the leading wire post 5. Exemplarily, the bottom surface of the leading wire post 5 is contacted with the top surface of the protrusion portion of the corresponding layer, and therefore, the leading wire post 5 may not need to penetrate through the main body portion above the corresponding layer, so that it contributes to reducing the resistance of the horizontal signal line 3 above the corresponding layer.

[0088] Referring to FIG. 29-FIG. 30, the memory cell TC includes the channel region 22 and source/drain doped regions 21 arranged in the third direction Y, and the source/drain doped regions 21 are located on two sides of the channel region 22. That is, the memory cell TC at least includes the transistor T. In some other embodiments, the memory cell TC may further include the capacitor C, and the transistor T and the capacitor C are arranged in the third direction Y. The source/drain doped regions 21 may include the first source/drain doped region 211 and the second source/drain doped region 212, the first source/drain doped region 211 may be contacted with the BL, and the second source/drain doped region 212 may be located on the side of the channel region 22 away from the first source/drain doped region 211.

[0089] The stacked structure also includes perpendicular signal lines 4 extending along the second direction Z and connected to multiple layers of memory cells TC in the same memory cell group TC0. One of the horizontal signal line 3 and the perpendicular signal line 4 is a BL, and the other of the horizontal signal line 3 and the perpendicular signal line 4 is a WL. The BL is contacted with the source/drain doped region 21, and the WL is contacted with the channel region 22.

[0090] Position relationships between the horizontal signal lines 3 and the leading wire posts 5 will be described below in detail in two situations: the horizontal signal lines are BLs and the horizontal signal lines are WLs.

[0091] In a case that the horizontal signal lines 3 are BLs, the horizontal signal lines 3

and the leading wire posts 5 mainly have the following several position relationships.

[0092] In example 1, referring to FIG. 38-FIG. 39, the leading wire post 5 directly faces the memory cell group TC0 in the third direction Y. Therefore, it contributes to improving the uniformity of position arrangement.

[0093] In example 2, referring to FIG. 40, the leading wire posts 5 and the memory cell groups TC are arranged alternatively in the first direction X. That is, the leading wire post 5 may directly face the space between adjacent memory cell groups TC0.

[0094] In example 3, referring to FIG. 41, the leading wire post 5 is arranged simultaneously opposite the memory cell group TC0 and the space between the adjacent memory cell groups TC0.

[0095] It is to be noted that in the case that the horizontal signal line 3 is the BL, in order to prevent the leading wire post 5 from cutting off the connection between the horizontal signal line 3 above the corresponding layer and the memory cell TC, the exposed region 32 may be located on the side close to the memory cell TC, and the contact region 31 may be located on the side away from the memory cell TC; alternatively, the exposed regions 32 may be located on two opposite sides of the contact region 31.

[0096] In some embodiment, referring to FIG. 42, there are two memory cells TC in each layer of the memory cell group TC0, and the two memory cells TC are respectively located in two opposite sides of the horizontal signal line 3 arranged in the third direction Y. In such case, one leading wire post 5 leads out more memory cells TC through the horizontal signal line 3, thereby facilitating to improve the integration level of the semiconductor structure.

[0097] In a case that the horizontal signal lines 3 are the WLs, the horizontal signal lines 3 and the leading wire posts 5 mainly have the following several position relationships.

[0098] In example 1, referring to FIG. 43, the leading wire post 5 is located between adjacent memory cell groups TC0, that is, the leading wire post 5 and the channel region

22 are staggered, so that the leading wire post 5 may be prevented from truncating the memory cell TC located above the corresponding layer, thereby reducing the number of the invalid memory cells TC.

[0099] In example 2, referring to FIG. 44, the orthographic projection of the leading wire post 5 on the surface of the substrate is overlapped with the orthographic projection of the channel region 22 on the surface of the substrate. That is, the leading wire post 5 may lead out the horizontal signal line 3 by utilizing the position of the channel region 22, so that it contributes to reducing the spacing between adjacent memory cell groups TC0, so as to improve the compact degree of the memory cell groups TC0, thereby improving the failure rate of the semiconductor structure.

[00100] In another embodiment of the disclosure, edges of the orthographic projection of the leading wire posts 5 on the surface of the substrate and the orthographic projection of the horizontal signal line 3 on the surface of the substrate are overlapped. That is, the leading wire post 5 may be directly connected to the horizontal signal line 3 by utilizing the space of the horizontal signal line 3 itself, and thus the numbers of the connection layers and the staircases may be decreased, thereby improving the integration level of the semiconductor structure.

[00101] As shown in FIG. 45-FIG. 46, another embodiment of the disclosure provides a method for manufacturing a semiconductor structure. It is to be noted that in order to conveniently describe and clearly illustrate operations of the method for manufacturing a semiconductor structure, FIG. 45-FIG. 56 all are partial schematic structural diagrams of the semiconductor structure. The method for manufacturing a semiconductor structure provided by an embodiment of the disclosure will be described below in detail in combination with the drawings.

[00102] A substrate is provided. A stacked structure is formed on the substrate, the stacked structure includes a plurality of memory cell groups TC0 arranged in a first direction X, and each of the memory cell groups TC0 includes multiple layers of memory cells TC arranged in a second direction Z. The stacked structure further includes a plurality of horizontal signal lines 3 arranged in the second direction Z, and each of the horizontal signal lines 3 is contacted with one layer of the memory cells TC.

[00103] Exemplarily, the memory cell TC may include the transistor T and the capacitor C. Specifically, the operation of forming the transistor T may include the following operations. Multiple spaced active layers are formed, and each of the active layers includes a plurality of active structures. The active structure is doped, so as to form the source/drain doped regions 21 and the channel region 22. A gate dielectric layer 6 is formed on the surface of the channel region 22. That is to say, the memory cell TC includes the channel region 22 and the source/drain doped regions 21 arranged in the third direction Y, and the source/drain doped regions 21 are located on two sides of the channel region 22; and the third direction Y is parallel to the surface of the substrate. In addition, it is necessary to form the insulating layer 12 between the transistors T of adjacent layers, so as to isolate the adjacent transistors T. The operation of forming the capacitor C may include the following operations. A capacitor supporting layer and a capacitor hole located in the capacitor supporting layer are formed. A lower electrode is formed on the inner wall of the capacitor hole, a capacitor dielectric layer 6 is formed on the surface of the lower electrode, and an upper electrode is formed on the surface of the capacitor dielectric layer 6. The lower electrode, the capacitor dielectric layer 6 and the upper electrode form the capacitor C.

[00104] A plurality of leading wire posts 5 arranged in the first direction X are formed. The plurality of leading wire posts 5 and the plurality of horizontal signal lines are arranged along the third direction Y, and the leading wire posts 5 are connected to the horizontal signal lines 3.

[00105] The method for forming the leading wire post 5 will be described below in detail.

[00106] It is to be noted first that the plurality of horizontal signal lines 3 include the first to Nth horizontal signal lines successively arranged in the second direction Z, N being a positive integer greater than 1. The first horizontal signal line is located in the top layer, and the Nth horizontal signal line is located in the bottom layer.

[00107] Referring to FIG. 45-FIG. 56, the through hole 8 is formed. The through hole 8 includes the first through hole to the Nth through hole, a side wall of the first horizontal signal line is exposed by the first through hole, and side walls of the first horizontal

signal line to the Nth horizontal signal line are exposed by the Nth through hole.

[00108] Taking the horizontal signal line 3 being a BL as an example, the operations of forming the through hole 8 will be described in detail.

[00109] Referring to FIG. 45-FIG. 46, an isolation structure is formed on the side wall of the horizontal signal line 3. In some embodiments, the isolation structure may include an etching barrier layer 13 and an isolation layer 14 arranged alternately. The isolation layer 14 and the horizontal signal line 3 are arranged in the same layer, and the etching barrier layer 13 is arranged directly opposite the insulating layer 12 between the adjacent horizontal signal lines 3 (referring to FIG. 10). In some other embodiments, the isolation structure may only include the isolation layer 14, and the isolation layer 14 covers the side walls of the horizontal signal line 3 and the insulating layer 12.

[00110] Continuously referring to FIG. 45-FIG. 46, a mask layer 71 is formed. The mask layer 71 has N openings 72, N being a positive integer greater than 1. The openings 72 are located on one side of the horizontal signal line 3. Exemplarily, the mask layer 71 may be a photoresist layer, and the photoresist layer is photoetched to form the openings 72. Alternatively, the mask layer 71 may be a hard mask layer 71 and a photoresist layer arranged in a stacked manner, and after the photoresist layer is photoetched, the hard mask layer 71 is etched, so as to form the openings 72.

[00111] Referring to FIG. 47-FIG. 48, the isolation layer 14 of the top layer is etched along the openings 72 until the etching barrier layer 13 of the top layer is exposed, so as to form a plurality of first sub-through holes 811. The first sub-through holes 811 expose side walls of the first horizontal signal line, and one of the first sub-through holes 811 serves as the first through hole 81.

[00112] Referring to FIG. 49-FIG. 50, a sacrificial layer 73 filling the first sub-through holes 811 is formed. Exemplarily, a material with a low dielectric constant, such as silicon oxide, is deposited in the first sub-through holes 811 to serve as the sacrificial layer 73.

[00113] Continuously referring to FIG. 49-FIG. 50, the mask layer 71 is patterned to enable the mask layer 71 to have (N-1) openings 72. Specifically, the photoresist layer

may be spin-coated again and photoetched, to form the openings 72.

[00114] Referring to FIG. 51-FIG. 52, the sacrificial layer 73 and the isolation layer 14 of the second layer are etched along the openings 72 to form (N-1) second sub-through holes 821. One of the second sub-through holes 821 serves as a second through hole 82.

[00115] Referring to FIG. 53-FIG. 54, the operations of forming the sacrificial layer 73, patterning the mask layer 71 and etching are repeated until the side wall of the Nth horizontal signal line 3 is exposed, that is, the top surface of the Nth etching barrier layer is exposed.

[00116] Based on FIG. 49-FIG. 54, the through holes 8 may be formed, and the through holes 8 include the first through hole 8 to the Nth through hole 8. Exemplarily, referring to FIG. 53-FIG. 54, the first through hole 81, the second through hole 82, the third through hole 84, the fourth through hole 84 and the fifth through hole 85 may be formed. It is to be noted that in the first direction X, depths of the first through hole 81, the second through hole 82, the third through hole 83, the fourth through hole 84 and the fifth through hole 85 successively arranged are increased in sequence. In other embodiments, in the first direction X, depths of the first through hole 81, the second through hole 82, the third through hole 83, the fourth through hole 84 and the fifth through hole 85 successively arranged may not be progressively increased or decreased, but the through holes are formed alternatively in depth, so as to avoid too large parasitic capacitance between the leading wire posts 5 with large depths among the subsequently formed leading wire posts 5.

[00117] It is to be noted that in a case that the horizontal signal line 3 is the WL, the operations of forming the through holes 8 are similar to the aforementioned operations, and the main difference lies in that the insulating layer 12 between the adjacent memory cell groups TC0 is etched to form the through holes 8. Other operations about forming the mask layer 71 and the sacrificial layer 73 may refer to the above detailed description.

[00118] Referring to FIG. 55-FIG. 56, the first contact portion to the Nth contact portion are respectively formed at the bottoms of the first through hole 81 to the Nth through hole, the first contact portion to the Nth contact portion are respectively arranged in the same

layers as the first horizontal signal line to the Nth horizontal signal line 3, and the contact portion 51 covers the side wall of the first horizontal signal 3 of the corresponding layer.

[00119] Continuously referring to FIG. 55-FIG. 56, after the contact portion 51 is formed, the dielectric layer 6 is formed on the side wall of the through hole 8. Exemplarily, an initial dielectric layer is formed on the side wall of the through hole 8 and the surface of the contact portion 51 through a chemical vapor deposition process. The initial dielectric layer on the surface of the contact portion 51 is removed, and the initial dielectric layer located on the side wall of the through hole 8 serves as the dielectric layer 6.

[00120] Continuously referring to FIG. 55-FIG. 56, an extension portion 52 filling the through hole 8 is formed, and the contact portion 51 and the extension portion 52 form the leading wire post 5. Exemplarily, metals such as copper, aluminum, titanium or tungsten are deposited in the through hole 8 as the leading wire post 5.

[00121] It is to be noted that the abovementioned method for forming the leading wire post 5 is merely exemplary description but is not limited thereto. The method for forming the leading wire post 5 may be adjusted according to a specific structure of the leading wire post 5.

[00122] As shown in FIG. 57-FIG. 60, another embodiment of the disclosure provides a method for manufacturing a semiconductor structure. The method for manufacturing a semiconductor structure is substantially same as the aforementioned method for manufacturing a semiconductor structure, and same or similar parts refer to detailed description in the aforementioned embodiments. In order to conveniently describe and clearly illustrate operations of the method for manufacturing a semiconductor, FIG. 57-FIG. 60 all are partial schematic structural diagrams of the semiconductor structure. The method for manufacturing a semiconductor structure will be described below in detail in combination with the drawings.

[00123] A substrate is provided. A stacked structure is formed on the substrate, the stacked structure includes a plurality of memory cell groups TC0 arranged in a first direction X, and each of the memory cell groups TC0 includes multiple layers of memory

cells TC arranged in a second direction Z. The stacked structure further includes a plurality of horizontal signal lines 3 arranged in the second direction Z, and each of the horizontal signal lines 3 is contacted with one layer of the memory cells TC.

[00124] The method about forming the stacked structure may refer to detailed description of the aforementioned embodiments.

[00125] Referring to FIG. 57-FIG. 60, the plurality of leading wire posts 5 arranged in the first direction and X and extending along the second direction Z are formed. Orthographic projections of the plurality of leading wire posts 5 on the surface of the substrate are at least partially overlapped with orthographic projections of the horizontal signal lines 3 on the surface of the substrate, and the leading wire posts 5 are connected to the horizontal signal lines 3.

[00126] The method for manufacturing the leading wire posts 5 will be described below in detail.

[00127] It is to be noted first that the plurality of horizontal signal lines 3 include the first to N^{th} horizontal signal lines successively arranged in the second direction Z, N being a positive integer greater than 1. The first horizontal signal line is located in the top layer, and the N^{th} horizontal signal line is located in the bottom layer.

[00128] Referring to FIG. 57-FIG. 58, the through holes 8 are formed, and the through holes 8 include the first through hole 81 to the N^{th} through hole. The top surface of the first horizontal signal line is exposed by the first through hole 81; the N^{th} through hole penetrates through the first horizontal signal line to the $(N-1)^{\text{th}}$ horizontal signal line, and exposes the top surface of the N^{th} horizontal signal line.

[00129] The operations of forming the through hole 8 are substantially same as the operations in the aforementioned embodiments, and the main difference lies in that the through hole 8 penetrates through one or more horizontal signal lines 3, and therefore, it is necessary to etch the one or more horizontal signal lines 3. In addition, in a case that the leading wire post 5 utilizes the position of the memory cell group TC0, it is further necessary to etch the channel region 22 and the insulating layer 12 located between memory cells TC of the upper layer and memory cells TC of the lower layer when the

through hole 8 is formed; and in a case that the leading wire post 5 utilizes the position between the adjacent memory cell groups TC0, it is further necessary to etch the insulating layer 12 between adjacent memory cells TC when the through hole 8 is formed. Other operations about forming the mask layer 71 and the sacrificial layer 73 may refer to detailed description of the aforementioned embodiments.

[00130] Referring to FIG. 59-FIG. 60, the dielectric layer 6 is formed on the side wall of the through hole 8. Specifically, an initial dielectric layer is formed on the inner walls of the through hole 8. The initial dielectric layer located on the bottom wall of the through hole 8 is removed to expose the horizontal signal line 3 of the corresponding layer, and the initial dielectric layer located on the side wall of the through hole 8 serves as the dielectric layer 6. The leading wire post 5 filling the through hole 8 is formed, and the bottom surface of the leading wire post 5 is electrically connected to the horizontal signal line 3.

[00131] In the embodiments of the disclosure, the horizontal signal line 3 is etched to form the through hole 8, and the dielectric layer 6 and the leading wire post 5 filling the through hole 8 are formed. Therefore, the leading wire post 5 may be electrically connected to the horizontal signal line 3 directly by utilizing the spatial position of the horizontal signal line 3, so that the number of the staircases may be reduced or the independent staircase area is not formed, thereby improving the integration level of the semiconductor structure.

[00132] The embodiments of the disclosure further provide a memory chip, including the semiconductor structure provided by the aforementioned embodiments.

[00133] The memory chip is a memory part for storing programs and various data information. Exemplarily, the memory chip may be a random access memory chip or a read-only memory chip. For example, the random access memory chip may include a Dynamic Random Access Memory (DRAM) or a Static Random Access Memory (SRAM). The integration level of the aforementioned semiconductor structure is high, which contributes to realizing microminiaturization of the memory chip.

[00134] The embodiments of the disclosure further provide an electronic device,

including the memory chip provided by the aforementioned embodiments.

[00135] Exemplarily, the electronic device may be a device such as a television, a computer, a mobile phone or a tablet computer. The electronic device may include a circuit board and a package structure, and the memory chip may be welded to the circuit board and protected by the package structure. In addition, the electronic device may further include a power supply for providing an operating voltage to the memory chip.

[00136] In the description of the specification, the description with reference to the terms “some embodiments”, “exemplarily”, and the like means that specific features, structures, materials, or features described in combination with the embodiments or examples are included in at least one embodiment or example of the disclosure. In the description, schematic expressions of the terms do not have to mean same embodiments or exemplary embodiments. Furthermore, specific features, structures, materials or characteristics described can be combined in any one or more embodiments or exemplary embodiments in proper manners. In addition, those skilled in the art can integrate or combine, without mutual contradiction, different embodiments or exemplary embodiments and integrate or combine features of different embodiments or exemplary embodiments described in the description.

[00137] Although the embodiments of the disclosure have been shown and described above, it can be understood that the embodiments are exemplary and should not be construed as limitation to the disclosure. Those of ordinary skill in the art can make changes, modifications, replacements and variations to the embodiments within the scope of the present disclosure. Any variations or and modifications made followed by claims and description of the disclosure shall fall within the scope of the disclosure.

CLAIMS

1. A semiconductor structure, comprising:

a substrate, on which a stacked structure is provided, wherein

the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and the stacked structure further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

a plurality of leading wire posts arranged in the first direction, wherein the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are connected to the horizontal signal lines.

2. The semiconductor structure according to claim 1, wherein each horizontal signal line is at least connected to one of the leading wire posts.

3. The semiconductor structure according to claim 2, wherein the plurality of horizontal signal lines are connected to the plurality of leading wire posts in one-to-one correspondence.

4. The semiconductor structure according to claim 1, wherein the leading wire posts extend in the second direction.

5. The semiconductor structure according to claim 1, wherein the leading wire posts connected to different horizontal signal lines are different in length in the second direction, and bottoms of the leading wire posts are contacted with the horizontal signal lines.

6. The semiconductor structure according to claim 1, wherein adjacent leading wire posts are arranged at an equal spacing in the first direction; or,

a spacing between the adjacent leading wire posts is in proportion to an area of a directly facing region.

7. The semiconductor structure according to claim 1, wherein the stacked structure further comprises:

multiple etching barrier layers arranged in the second direction, each etching barrier layer being contacted with a bottom surface of at least one of the leading wire posts.

8. The semiconductor structure according to claim 1, wherein the stacked structure further comprises: a dielectric layer, at least located on a side wall of a leading wire post facing a horizontal signal line, a lower surface of the dielectric layer being higher than the horizontal signal line connected to the leading wire post.

9. The semiconductor structure according to claim 1, wherein each memory cell comprises a channel region and source/drain doped regions arranged in the third direction, the source/drain doped regions being located on two sides of the channel region.

10. The semiconductor structure according to claim 9, wherein the horizontal signal line is a bit line, the bit line being contacted with the source/drain doped regions.

11. The semiconductor structure according to claim 10, wherein the leading wire post and the memory cell are respectively located on two opposite sides of the horizontal signal line arranged in the third direction.

12. The semiconductor structure according to claim 11, wherein a width of the leading wire post in the first direction is greater than or equal to that of the memory cell group; and/or

the width of the leading wire post in the first direction is greater than or equal to a spacing between adjacent memory cell groups; and/or

the width of the leading wire post in the first direction is greater than that of the leading wire post in the third direction.

13. The semiconductor structure according to claim 11, wherein the leading wire posts and the memory cell groups are directly opposite in the third direction; or

the leading wire posts and the memory cell groups are arranged alternatively in the first direction.

14. The semiconductor structure according to claim 10, wherein the leading wire post and the memory cell are located on a same side of the horizontal signal line.

15. The semiconductor structure according to claim 14, wherein a width of the leading wire post in the third direction is greater than that of the leading wire post in the first direction.

16. The semiconductor structure according to claim 10, wherein horizontal signal lines of two adjacent stacked structures are arranged opposite, a leading wire post is located between horizontal signal lines of the adjacent stacked structures, and horizontal signal lines of the same layers of the adjacent stacked structures are electrically connected through at least one of the leading wire posts.

17. The semiconductor structure according to claim 10, wherein each layer of memory cells in the memory cell group comprises two memory cells, and the two memory cells are respectively located in two opposite sides of the horizontal signal line arranged in the third direction.

18. The semiconductor structure according to claim 17, wherein adjacent leading wire posts are located on different sides of the horizontal signal line; or

all the leading wire posts are located on the same side of the horizontal signal line.

19. The semiconductor structure according to claim 9, wherein the horizontal signal line is a word line, the word line being contacted with the channel region.

20. The semiconductor structure according to claim 19, wherein adjacent leading wire posts are located on different sides of the horizontal signal line; or

all the leading wire posts are located on the same side of the horizontal signal line.

21. A semiconductor structure, comprising:

a substrate, on which a stacked structure is provided, wherein

the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and the stacked structure further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

a plurality of leading wire posts arranged in the first direction and extending along the second direction, wherein orthographic projections of the plurality of leading wire posts on a

surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are connected to the horizontal signal lines.

22. The semiconductor structure according to claim 21, wherein at least one of the leading wire posts penetrates through at least one of the horizontal signal lines.

23. The semiconductor structure according to claim 21, wherein each horizontal signal line comprises a contact region and an exposed region arranged in the third direction, a leading wire post is contacted with the contact region, and the third direction is perpendicular to the second direction and parallel to the surface of the substrate.

24. The semiconductor structure according to claim 23, wherein

the horizontal signal line has two opposite sides arranged in the third direction, the exposed region is located on one side of the two opposite sides, the contact region is located on the other side of the two opposite sides, and the leading wire post is protruded relative to the contact region.

25. The structure according to claim 21, wherein each memory cell comprises a channel region and source/drain doped regions arranged in a third direction, the source/drain doped regions being located on two sides of the channel region.

26. The semiconductor structure according to claim 25, wherein the horizontal signal line is a bit line, the bit line being contacted with the source/drain doped regions.

27. The semiconductor structure according to claim 26, wherein

the leading wire posts and the memory cell groups are directly opposite in the third direction; or

the leading wire posts and the memory cell groups are arranged alternatively in the first direction.

28. The semiconductor structure according to claim 25, wherein the horizontal signal line is a word line, the word line being contacted with the channel region.

29. The semiconductor structure according to claim 28, wherein

the leading wire post is located between adjacent memory cell groups; or

an orthographic projection of the leading wire post on the surface of the substrate is overlapped with an orthographic projection of the channel region on the surface of the substrate.

30. The semiconductor structure according to claim 21, wherein the horizontal signal line has two opposite sides arranged in a third direction, each layer of memory cells in the memory cell group comprises two memory cells, and the two memory cells are respectively located in two opposite sides of the horizontal signal line arranged in the third direction.

31. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a stacked structure on the substrate, wherein the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups

comprising multiple layers of memory cells arranged in a second direction, and further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

forming a plurality of leading wire posts arranged in the first direction, wherein the plurality of leading wire posts and the plurality of horizontal signal lines are arranged along a third direction, and the leading wire posts are connected to the horizontal signal lines.

32. The method for manufacturing a semiconductor structure according to claim 31, wherein the plurality of horizontal signal lines comprise a first horizontal signal line to an N^{th} horizontal signal line successively arranged in the second direction, N being a positive integer greater than 1;

the manufacturing method comprises:

forming a first through hole to an N^{th} through hole, wherein the first through hole exposes a side wall of the first horizontal signal line, and the N^{th} through hole exposes side walls of the first horizontal signal line to the N^{th} horizontal signal line;

respectively forming a first contact portion to an N^{th} contact portion at bottoms of the first through hole to the N^{th} through hole, wherein the first contact portion to the N^{th} contact portion respectively cover the side walls of the first horizontal signal line to the N^{th} horizontal signal line;

forming, after forming contact portions, dielectric layers on the side walls of the through holes; and

forming an extension portion filling each through hole, the contact portions and the extension portions forming the leading wire posts.

33. A method for manufacturing a semiconductor structure, comprising:

providing a substrate;

forming a stacked structure on the substrate, wherein the stacked structure comprises a plurality of memory cell groups arranged in a first direction, each of the memory cell groups comprising multiple layers of memory cells arranged in a second direction, and further comprises a plurality of horizontal signal lines arranged in the second direction, each of the horizontal signal lines being in contact with one layer of the memory cells; and

forming a plurality of leading wire posts arranged in the first direction and extending along the second direction, wherein orthographic projections of the plurality of leading wire posts on a surface of the substrate and orthographic projections of the horizontal signal lines on the surface of the substrate are at least partially overlapped, and the leading wire posts are connected to the horizontal signal lines.

34. The method for manufacturing a semiconductor structure according to claim 33, wherein the plurality of horizontal signal lines comprise a first horizontal signal line to an N^{th} horizontal signal lines successively arranged in the second direction, N being a positive integer greater than 1;

the manufacturing method comprises:

forming a first through hole to an N^{th} through hole, wherein the first through hole exposes a top surface of the first horizontal signal line, and the N^{th} through hole penetrates through the first horizontal signal line to the $(N-1)^{\text{th}}$ horizontal signal line, and exposes a top surface of the N^{th} horizontal signal line;

forming dielectric layers on side walls of the through holes; and

forming the leading wire posts filling the through holes.

35. A memory chip, comprising the semiconductor structure according to any one of claims 1-20 or the semiconductor structure according to any one of claims 21-30.

36. An electronic device, comprising the memory chip according to claim 35.