

ABSTRACT

WIDE-BAND SINGLE-ENDED TO DIFFERENTIAL CONVERTER IN CMOS TECHNOLOGY

A wide-band single-ended to differential converter (DC to 1 GHz) with very low amplitude and phase matching errors, of the order of 0.01dB and 0.15 degrees respectively and using CMOS technology, is comprised of a first and a second stage. The very low amplitude and phase matching errors have been achieved firstly by the use of capacitive means C_D across the gate and source of the first stage MOS transistor M_1 with a value equal to the drain to ground (reference potential) parasitic capacitance of the tail current source device for the first stage, and secondly by using equal valued capacitive means C_{F1} , C_{F2} in the second stage and setting their values to be several (5-10) times more than the gate-drain parasitic capacitances of either of the differential transistors of the second stage.

(FIGURE 6 IS SUGGESTED FOR PUBLICATION)