type of substrate commonly being referred to as an “HR substrate” for high-resistivity substrate. The latter is advantageously combined with a charge-trapping layer, i.e. a trap-rich layer. However, this type of substrate is incompatible with use of transistors the threshold voltage of which may be controlled via a back-side gate (back bias voltage).

Specifically, the presence of this layer containing trapped charges hinders back biasing (application of a potential difference to the back side) and may furthermore lead to an accelerated diffusion of dopants, thus preventing the production of high-quality PN junctions, because of problems with junction leakage.

Apart from FD-SOI structures comprising one BOX layer, FD-SOI structures comprising two BOX layers, which are called “double BOX” structures, have been produced.

The double-BOX technology is advantageous in the case where the FD-SOI structure comprises double-gate transistors the gate electrodes of which are formed both above and below the conduction channel. Thus, the SOI layer of the back gate, which is called the back-gate SOI layer, is electrically separated from the SOI layer of the front gate, which is called the front-gate SOI layer, by a first BOX layer, and is also electrically separated from the basic substrate by a second BOX layer.

Document US 2010/0176482 describes an example of such an FD-SOI structure comprising two BOX layers, for a CMOS technology.

According to this document, CMOS structures with a high-k gate dielectric and with a gate length of as small as 30 nm are fabricated using an optimised process allowing a good isolation between the devices and the back gate to be obtained.

The existing double-BOX technology is used for digital applications, and not both for radiofrequency and digital applications.

BRIEF DESCRIPTION OF THE INVENTION

Embodiments of the invention seek to provide a semiconductor-on-insulator structure allowing the aforementioned drawbacks to be overcome. Embodiments of the invention aim to provide such a structure allowing digital applications and radiofrequency applications to be combined.

An aspect of the invention provides a semiconductor-on insulator multilayer structure comprising:

- a stack, called the back stack, of the following layers from a back side to a front side of the structure:
    - a semiconductor carrier substrate the electrical resistivity of which is comprised between 500 Ω.cm and 30 kΩ.cm,
    - a first electrically insulating layer,
    - a first semiconductor layer,
- at least one trench isolation that extends through the back stack at least down to the first electrically insulating layer, and that electrically isolates two adjacent regions of the multilayer structure,

the multilayer structure mainly being characterized in that it furthermore comprises:

- at least one FD-SOI first region comprising a stack, called the front stack, arranged on the back stack, said front stack comprising:
  - a second electrically insulating layer arranged on the first semiconductor layer,
  - a second semiconductor layer called the active layer, arranged on the second electrically insulating layer,

  wherein the first electrically insulating layer has a thickness larger than that of the second electrically insulating layer, and the first semiconductor layer has a thickness larger than that of the active layer, said FD-SOI first region furthermore comprising at least one digital component in the active layer,
- at least one RF-SOI second region electrically isolated from the FD-SOI region by a trench isolation, comprising at least one radiofrequency component plumb with the first electrically insulating layer.

According to embodiments, the structure has the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the back stack furthermore comprises a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer;
- the charge-trapping layer is made of polysilicon or of porous silicon;
- the radiofrequency component is arranged in the first semiconductor layer;
- the RF-SOI second region comprises the front stack arranged on the back stack, and wherein the radiofrequency component is arranged in the active layer;
- the first semiconductor layer is made of crystalline material;
- the first semiconductor layer is made of amorphous material;
- the second semiconductor layer is made of crystalline material;
- the first electrically insulating layer is a layer of silicon oxide;
- the second electrically insulating layer is a layer of silicon oxide;
- the first electrically insulating layer has a thickness comprised between 50 nm and 1500 nm;
- the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm;
- the first semiconductor layer has a thickness comprised between 10 nm and 200 nm;
- the active layer has a thickness comprised between 3 nm and 30 nm.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- providing a first donor substrate,
- forming a weakened zone in said first donor substrate, so as to delineate a first semiconductor layer,
- transferring said first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form a back stack comprising the carrier substrate, the first electrically insulating layer and the transferred first semiconductor layer,
- providing a second donor substrate,
- forming a weakened zone in said second donor substrate, so as to delineate a second semiconductor layer, called the active layer,
- transferring said semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack comprising the second electrically insulating layer and the transferred second semiconductor layer,
- forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,
- producing:
    - at least one digital component in the active layer, in the FD-SOI region, and
    - at least one radiofrequency component plumb with the first electrically insulating layer.

Another aspect of the invention provides a process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:

- forming a back stack by depositing a first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
- providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate a second semiconductor layer,
- transferring said second semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack on the back stack,
- forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in

order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,

- producing:
    - at least one digital component in the active layer, in the FD-SOI region, and
    - at least one radiofrequency component plumb with the first electrically insulating layer.

According to embodiments, the processes have the following various features, which may be implemented alone or in technically feasible combinations thereof:

- the method comprises, before the radiofrequency component is produced, a step of selectively removing the active layer and the second electrically insulating layer of the RF-SOI region, and wherein the radiofrequency component is then formed in the first semiconductor layer;
- the process furthermore comprises, before the transferring step, forming a charge-trapping layer on the receiver substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer.

The multilayer structure accordingly to embodiments of the invention can serve as carrier for the fabrication of transistors, in particular MOSFETs. MOSFETs are semiconductor devices comprising three active electrodes, namely an input electrode called the gate, an output electrode called the drain, and a third electrode called the source. These transistors allow a voltage (or a current) output on the drain to be controlled by virtue of the gate.

In the present text, the term “on”, when it relates to the position of a first layer with respect to a second layer, or the position of a component with respect to a layer, does not necessarily imply that the first layer makes direct contact with the second or that the component makes direct contact with the layer. Unless otherwise specified, this term does not exclude one or more other layers being intermediate between the first layer and second layer, or between the component and the layer.

DESCRIPTION OF THE FIGURES

Other advantages and features of the invention will become apparent upon reading the following description given by way of illustrative and non-limiting example, with reference to the following appended figures:

Figure 1 is a schematic of a first embodiment of a multilayer structure according to the invention, comprising two FD-SOI regions and one RF-SOI region, in which a digital

CLAIMS

1. Semiconductor-on-insulator multilayer structure, comprising:
- a stack, called the back stack, of the following layers from a back side to a front side of the structure:
a semiconductor carrier substrate the electrical resistivity of which is comprised between 500 Ω.cm and 30 kΩ.cm,
a first electrically insulating layer,
a first semiconductor layer,
- at least one trench isolation that extends through the back stack at least down to the first electrically insulating layer, and that electrically isolates two adjacent regions of the multilayer structure,
the multilayer structure being characterized in that it furthermore comprises:
- at least one FD-SOI first region comprising a stack, called the front stack, arranged on the back stack, said front stack comprising:
a second electrically insulating layer arranged on the first semiconductor layer,
a second semiconductor layer called the active layer, arranged on the second electrically insulating layer,
wherein the first electrically insulating layer has a thickness larger than that of the second electrically insulating layer, and the first semiconductor layer has a thickness larger than that of the active layer, said FD-SOI first region furthermore comprising at least one digital component in the active layer,
- at least one RF-SOI second region electrically isolated from the FD-SOI region by a trench isolation, comprising at least one radiofrequency component plumb with the first electrically insulating layer.

2. Structure according to Claim 1, wherein the back stack furthermore comprises a charge-trapping layer arranged between the carrier substrate and the first electrically insulating layer.

3. Structure according to Claim 2, wherein the charge-trapping layer is made of polysilicon or of porous silicon.

4. Structure according to one of Claims 1 to 3, wherein the radiofrequency component is arranged in the first semiconductor layer.

5. Structure according to one of Claims 1 to 3, wherein the RF-SOI second region comprises the front stack arranged on the back stack, and wherein the radiofrequency component is arranged in the active layer.

6. Structure according to one of the preceding claims, wherein the first semiconductor layer is made of crystalline material.

7. Structure according to one of the Claims 1 to 5, wherein the first semiconductor layer is made of amorphous material.

8. Structure according to one of the preceding claims, wherein the second semiconductor layer is made of crystalline material.

9. Structure according to one of the preceding claims, wherein the first electrically insulating layer is a layer of silicon oxide.

10. Structure according to one of the preceding claims, wherein the second electrically insulating layer is a layer of silicon oxide.

11. Structure according to one of the preceding claims, wherein the first electrically insulating layer has a thickness comprised between 50 nm and 1500 nm.

12. Structure according to one of the preceding claims, wherein the second electrically insulating layer has a thickness comprised between 10 nm and 100 nm.

13. Structure according to one of the preceding claims, wherein the first semiconductor layer has a thickness comprised between 10 nm and 200 nm.

14. Structure according to one of the preceding claims, wherein the active layer has a thickness comprised between 3 nm and 30 nm.

15. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
- providing a first donor substrate,
- forming a weakened zone in said first donor substrate, so as to delineate a first semiconductor layer,
- transferring said first semiconductor layer to a semiconductor carrier substrate, a first electrically insulating layer being at the interface between the donor substrate and the carrier substrate so as to form a back stack comprising the carrier substrate, the first electrically insulating layer and the transferred first semiconductor layer,
- providing a second donor substrate,

- forming a weakened zone in said second donor substrate, so as to delineate a second semiconductor layer, called the active layer,
- transferring said semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack comprising the second electrically insulating layer and the transferred second semiconductor layer,
- forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,
- producing:

at least one digital component in the active layer, in the FD-SOI region, and

at least one radiofrequency component plumb with the first electrically insulating layer.

16. Process for fabricating a semiconductor-on-insulator multilayer structure, comprising the following steps:
- forming a back stack by depositing a first semiconductor layer on a carrier substrate covered with a first electrically insulating layer,
- providing a donor substrate,
- forming a weakened zone in said donor substrate, so as to delineate a second semiconductor layer,
- transferring said second semiconductor layer to the back stack, a second electrically insulating layer being at the interface between the second donor substrate and the back stack, so as to form a front stack on the back stack,
- forming at least one trench isolation that extends through the front stack and through the back stack at least down to the first electrically insulating layer, in order to electrically isolate two adjacent regions, including at least one FD-SOI region and at least one RF-SOI region,
- producing:

at least one digital component in the active layer, in the FD-SOI region, and

at least one radiofrequency component on the first semiconductor layer.

17. Process according to Claim 15 or Claim 16, comprising, before the radiofrequency component is produced, a step of selectively removing the active layer and the second electrically insulating layer of the RF-SOI region, and wherein the radiofrequency component is then formed in the first semiconductor layer.

18. Process according to one of Claims 15 to 17, furthermore comprising, before the transferring step, forming a charge-trapping layer on the receiver substrate, said charge-trapping layer being arranged between the carrier substrate and the first electrically insulating layer.