

A DIAGNOSIS FRAMEWORK TO SHORTEN YIELD LEARNING CYCLES OF ADVANCED PROCESSES

ABSTRACT

The present disclosure relates to a diagnosis framework to shorten yield learning cycles of technology node manufacturing processes from the high defect density stage to technology maturity. A plurality of defect under test (DUT) structures are designed to capture potential manufacturing issues associated with defect formation. A test structure is formed by arranging the DUT structures within a DUT carrier unit, which has been yield-hardened through heuristic yield analysis such that a defect density of the DUT carrier unit is essentially zero. Possible outcomes of an application of test patterns and various failure scenarios associated with defects formed within the DUT structures within the DUT carrier unit are simulated and stored in a look-up table (LUT). The LUT may then be referenced to determine a location of a defect within the test structure without the need for iterative analysis to correctly select defect candidates for physical failure analysis (PFA).

Figure 1