CLAIMS

1. A transmission circuit, applicable to a Dynamic Random Access Memory, DRAM, and comprising:

an upper-layer clock bonding pad, configured to transmit a clock signal;

M upper-layer data bonding pads, configured to transmit data signals;

a lower-layer clock bonding pad, electrically connected with the upper-layer clock bonding pad, wherein an area of the lower-layer clock bonding pad is smaller than that of the upper-layer clock bonding pad; and

M lower-layer data bonding pads, electrically connected with the M upper-layer data bonding pads in a one-to-one correspondence, wherein an area of each lower-layer data bonding pad is smaller than that of each upper-layer data bonding pad, and a distance between each lower-layer data bonding pad and the lower-layer clock bonding pad is less than a distance between an upper-layer data bonding pad corresponding to the lower-layer data bonding pad and the upper-layer clock bonding pad;

wherein the upper-layer clock bonding pad and the upper-layer data bonding pads are located on a first layer, the lower-layer clock bonding pad and the lower-layer data bonding pads are located on a second layer, a dielectric layer is arranged between the first layer and the second layer, and the first layer, the dielectric layer and the second layer are all located on a same substrate, M being an integer greater than or equal to 2;

characterized in that the lower-layer data bonding pads are arranged in two parallel rows, and the lower-layer clock bonding pad is located in one of the two parallel rows, and has a same number of lower-layer data bonding pads on two sides thereof; and

part of the upper-layer data bonding pads and the upper-layer clock bonding pad are

arranged in a same row, and remaining upper-layer data bonding pads are arranged in a same column around two or more sides of the two parallel rows of the lower-layer data bonding pads and the lower-layer clock bonding pad.

2. The transmission circuit of claim 1, further comprising: a first metal connecting line, located between the lower-layer clock bonding pad and the upper-layer clock bonding pad; and a second metal connecting line, located between a lower-layer data bonding pad and an upper-layer data bonding pad corresponding to the lower-layer data bonding pad, wherein a length of the first metal connecting line is smaller than that of the second metal connecting line.

3. The transmission circuit of claim 2, wherein the first metal connecting line comprises: a first conductive hole, penetrated through the dielectric layer and contacted with the lower-layer clock bonding pad; and a first metal layer, located on one side of the dielectric layer away from the first layer and contacted with the first conductive hole and the upper-layer clock bonding pad; and

the second metal connecting line comprises: a second conductive hole, penetrated through the dielectric layer and contacted with the lower-layer data bonding pad; and a second metal layer, located on one side of the dielectric layer away from the first layer and contacted with the second conductive hole and the upper-layer data bonding pad;

wherein a length of the first conductive hole is the same as that of the second conductive hole, and a length of the first metal layer is smaller than that of the second metal layer.

4. The transmission circuit of claim 2, wherein the first metal connecting line comprises a first conductive plug, penetrated through the dielectric layer and contacted with the lower-layer clock bonding pad and the upper-layer clock bonding pad; and

the second metal connecting line comprises a second conductive plug, penetrated through the dielectric layer and contacted with the lower-layer data bonding pad and the upper-layer data bonding pad;

wherein a length of the first conductive plug is smaller than that of the second conductive plug.

5. The transmission circuit of claim 1, wherein the area of the lower-layer clock bonding pad is the same as that of the lower-layer data bonding pad.

6. The transmission circuit of claim 1, further comprising a plurality of lower-layer test bonding pads, wherein the plurality of lower-layer test bonding pads have a same area, and an area of a lower-layer test bonding pad is greater than that of the lower-layer data bonding pad.