

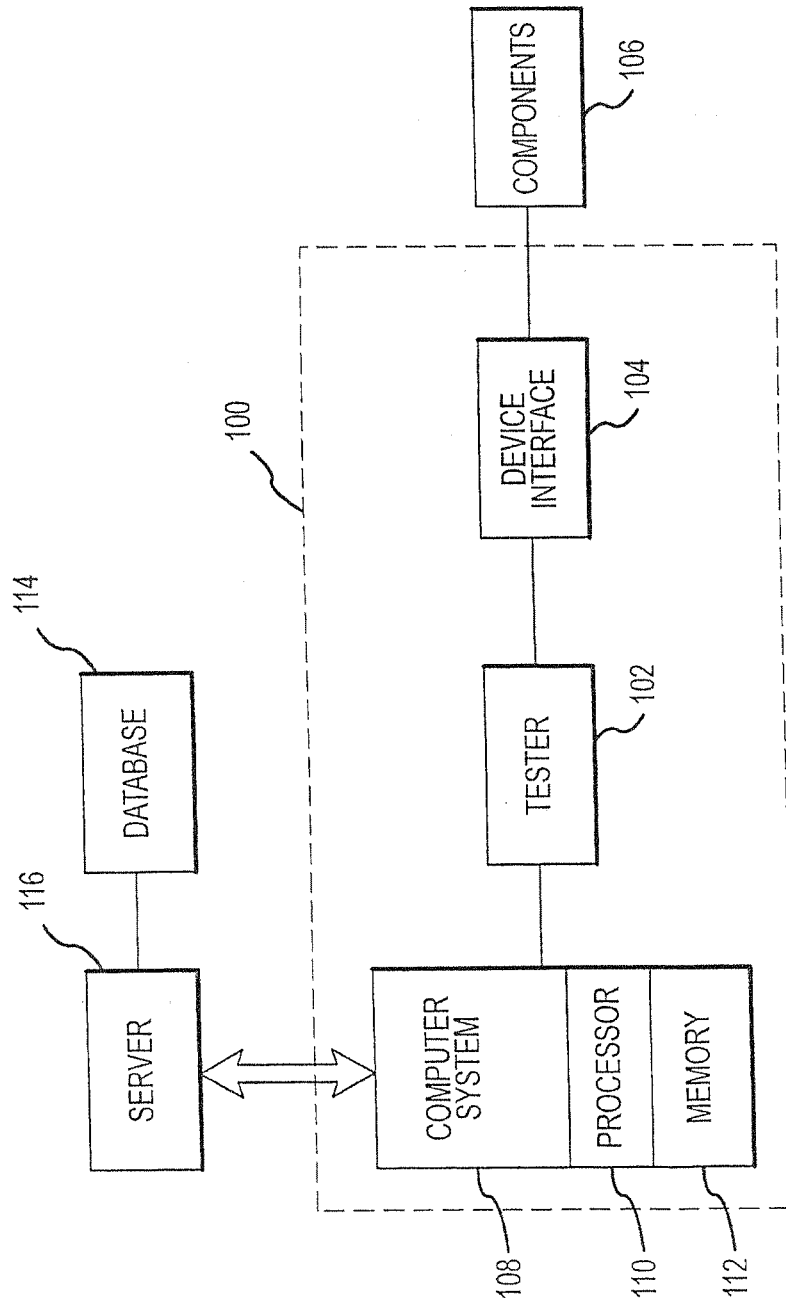


FIG.1

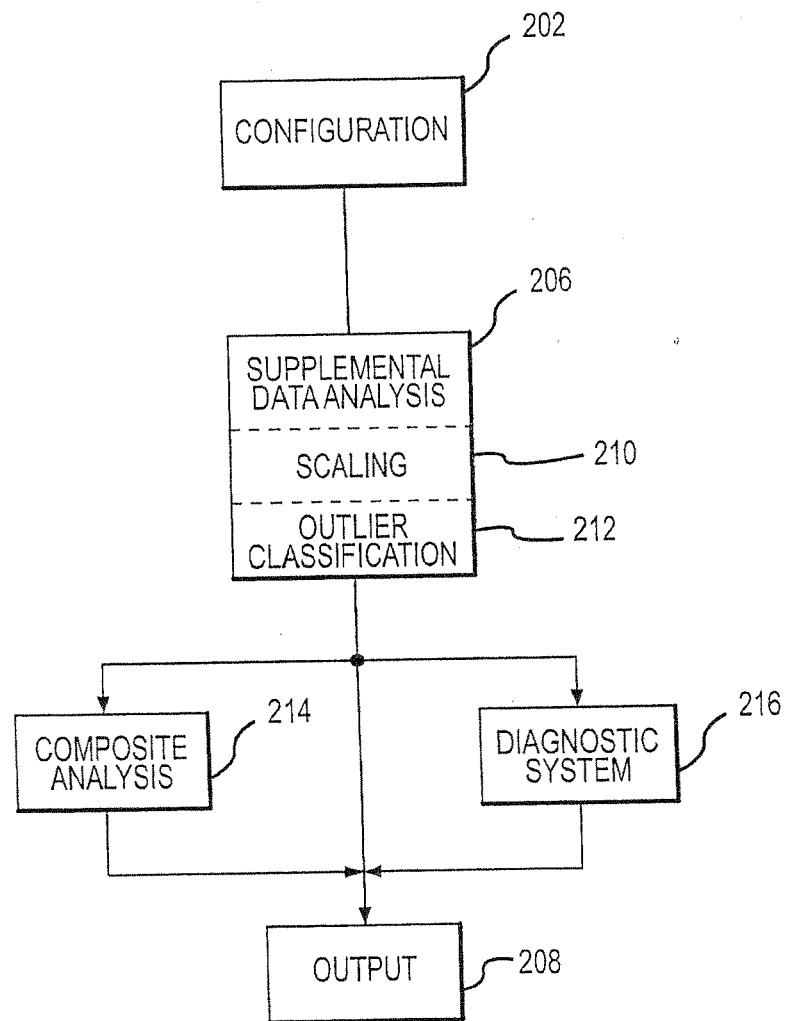


FIG.2

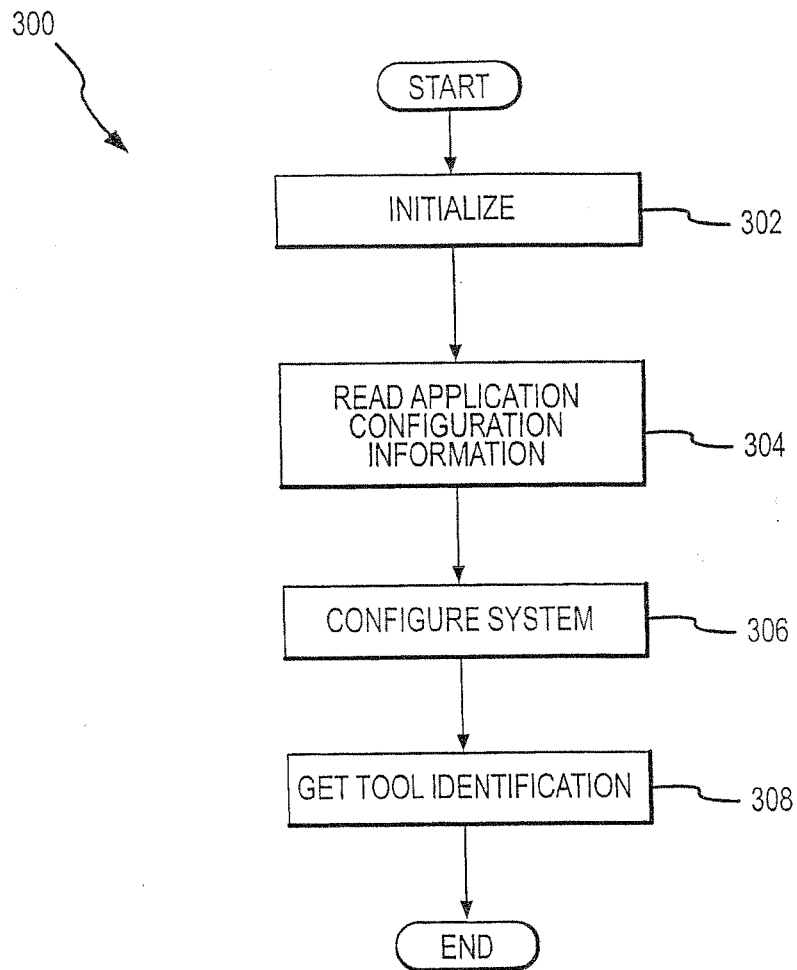


FIG.3

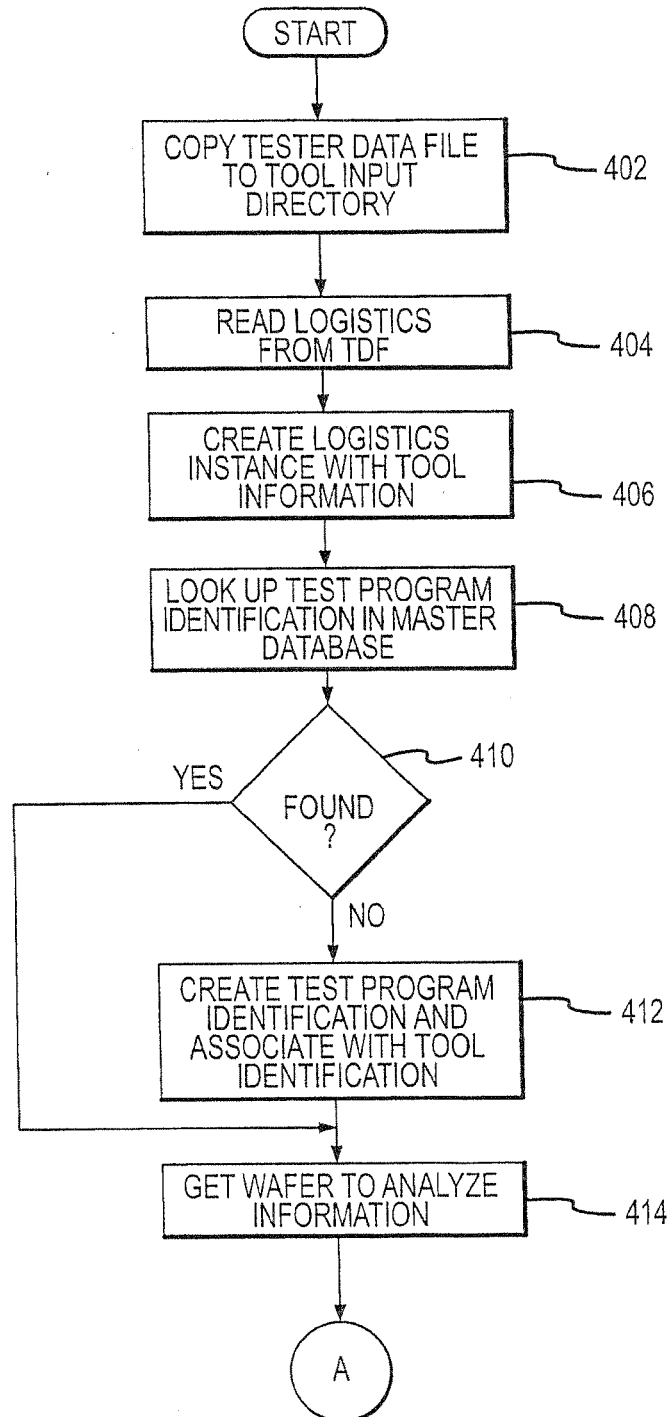


FIG.4A

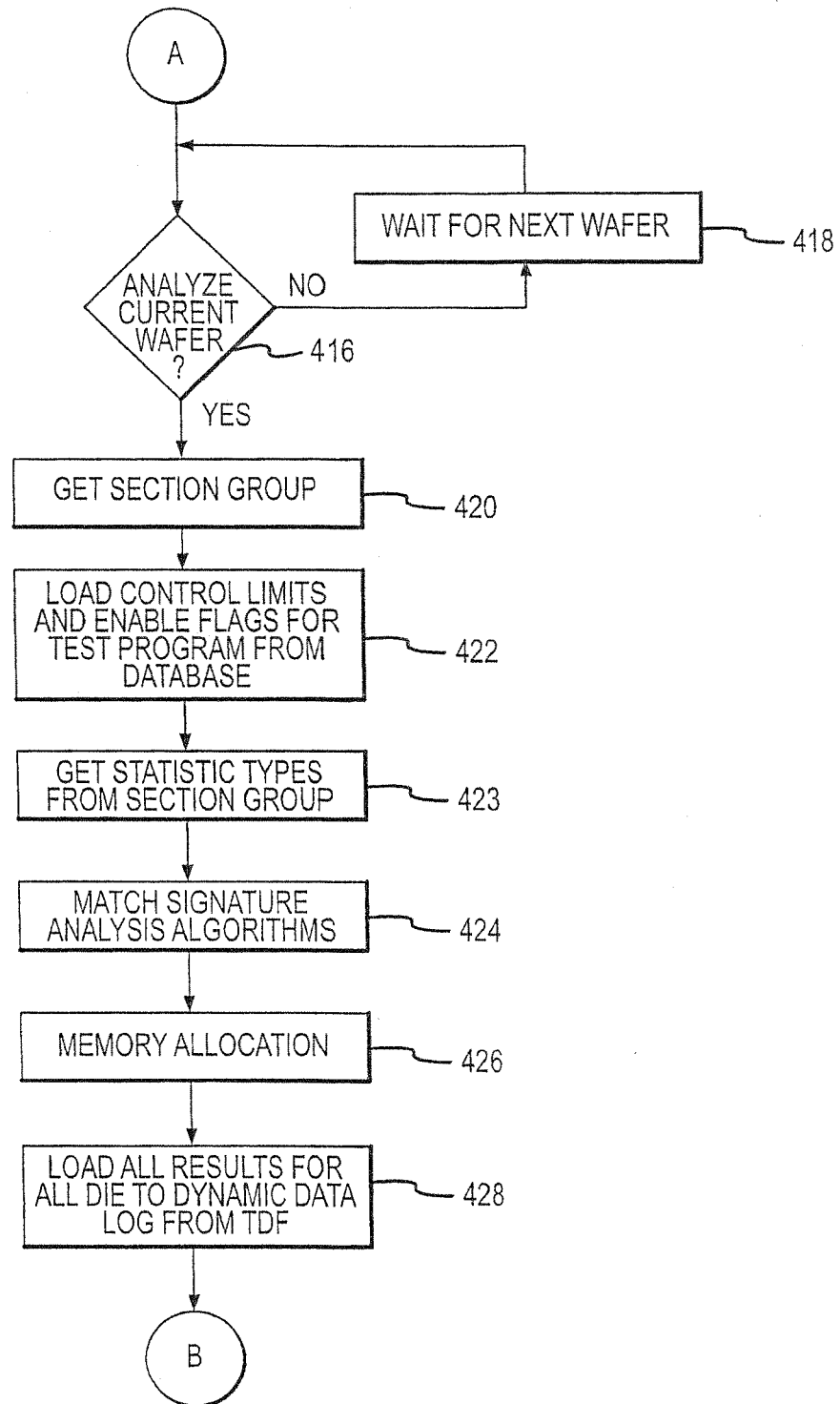


FIG.4B

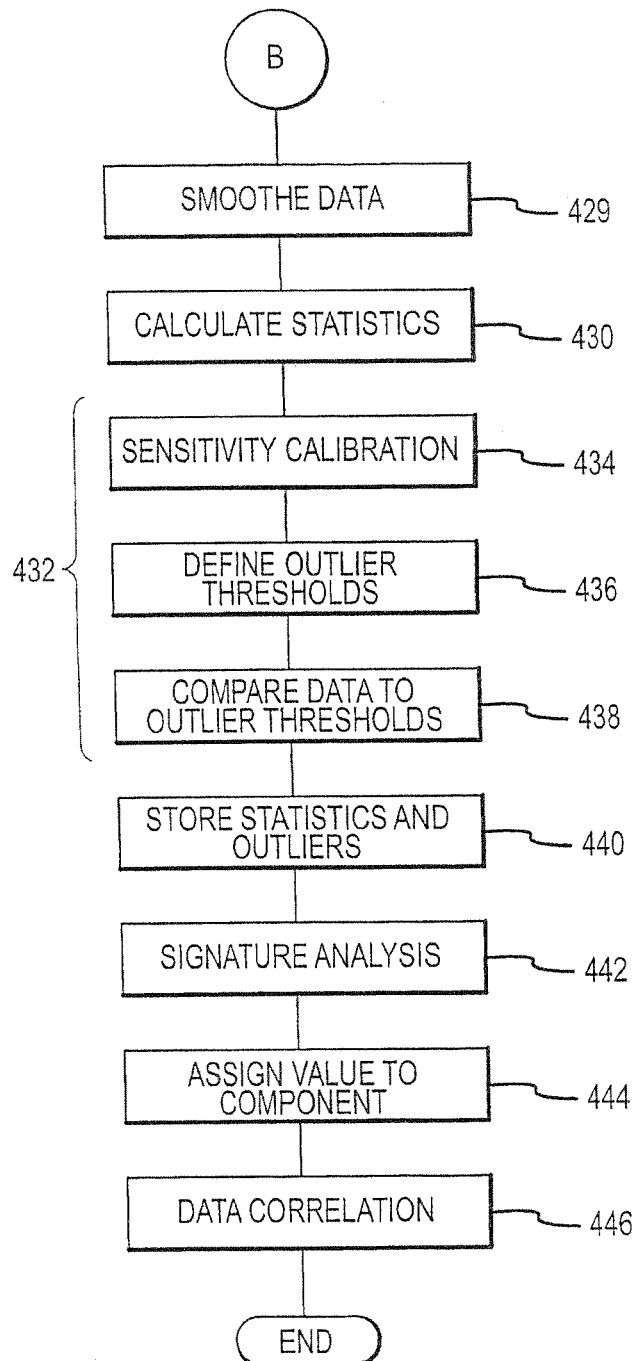


FIG. 4C

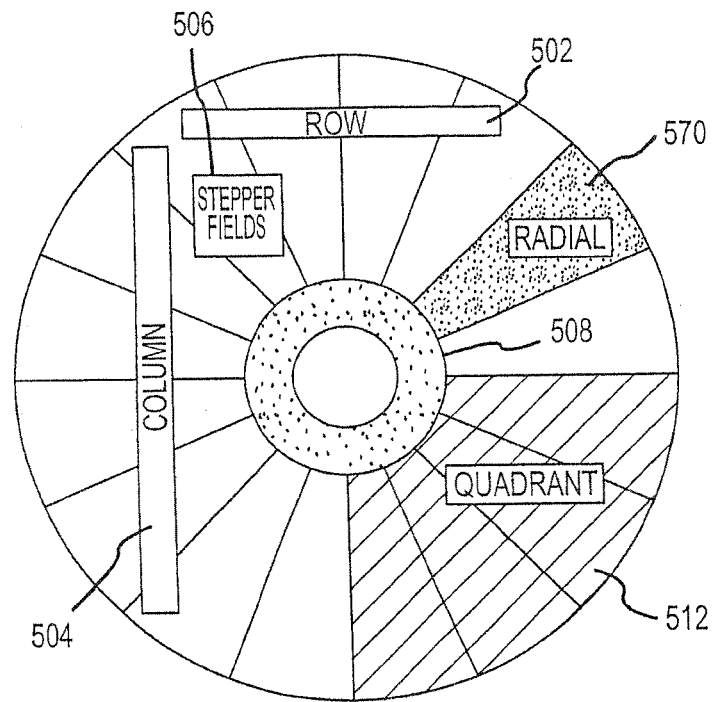


FIG.5

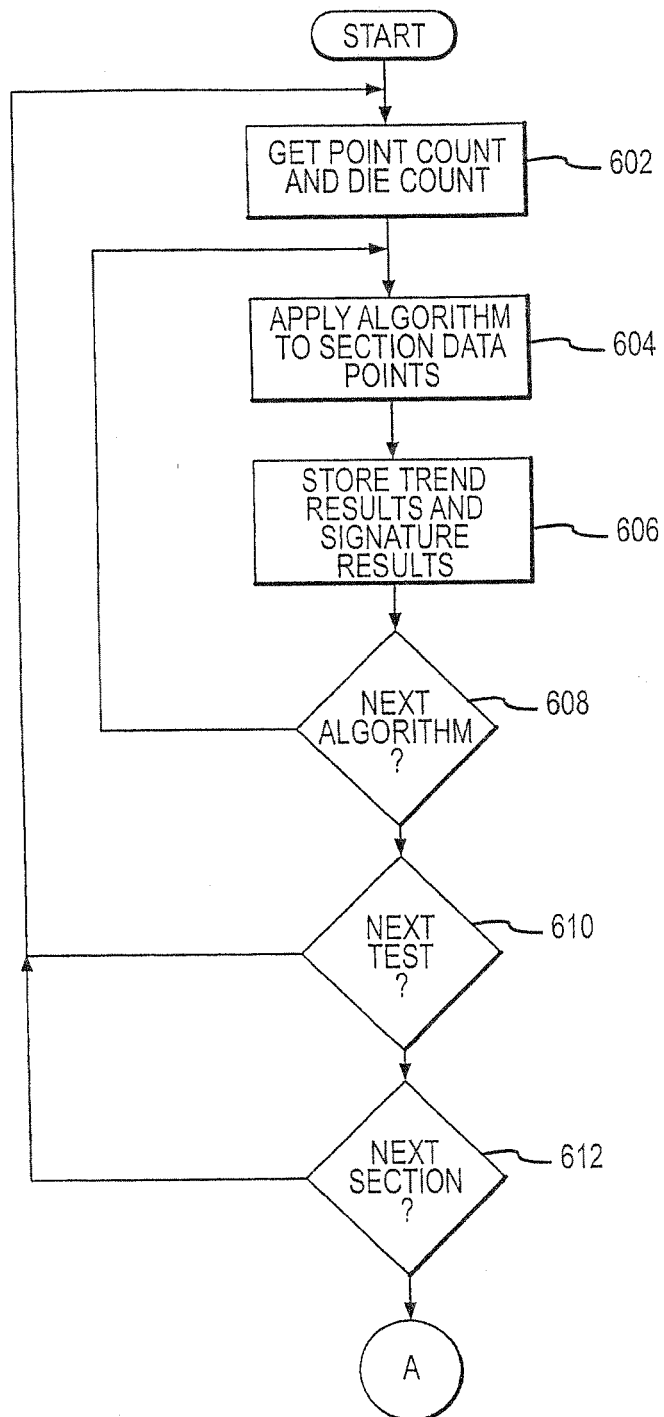


FIG.6A

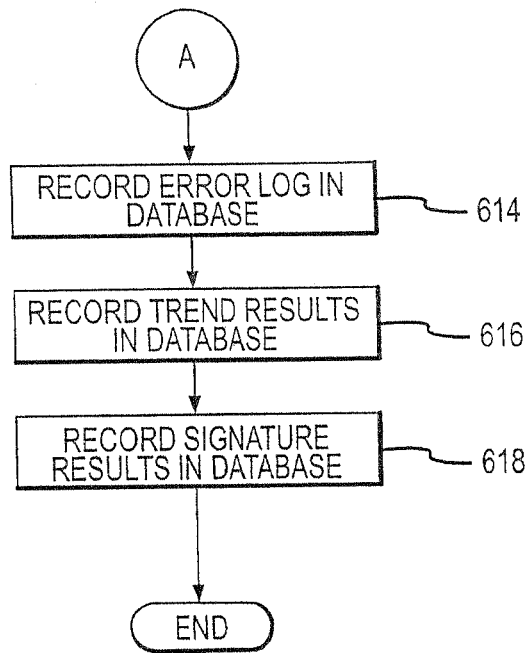


FIG. 6B

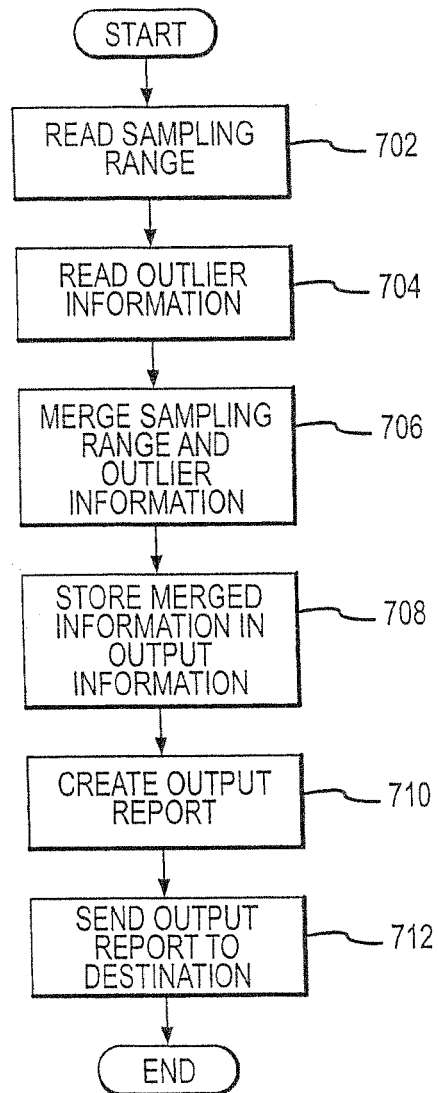


FIG.7

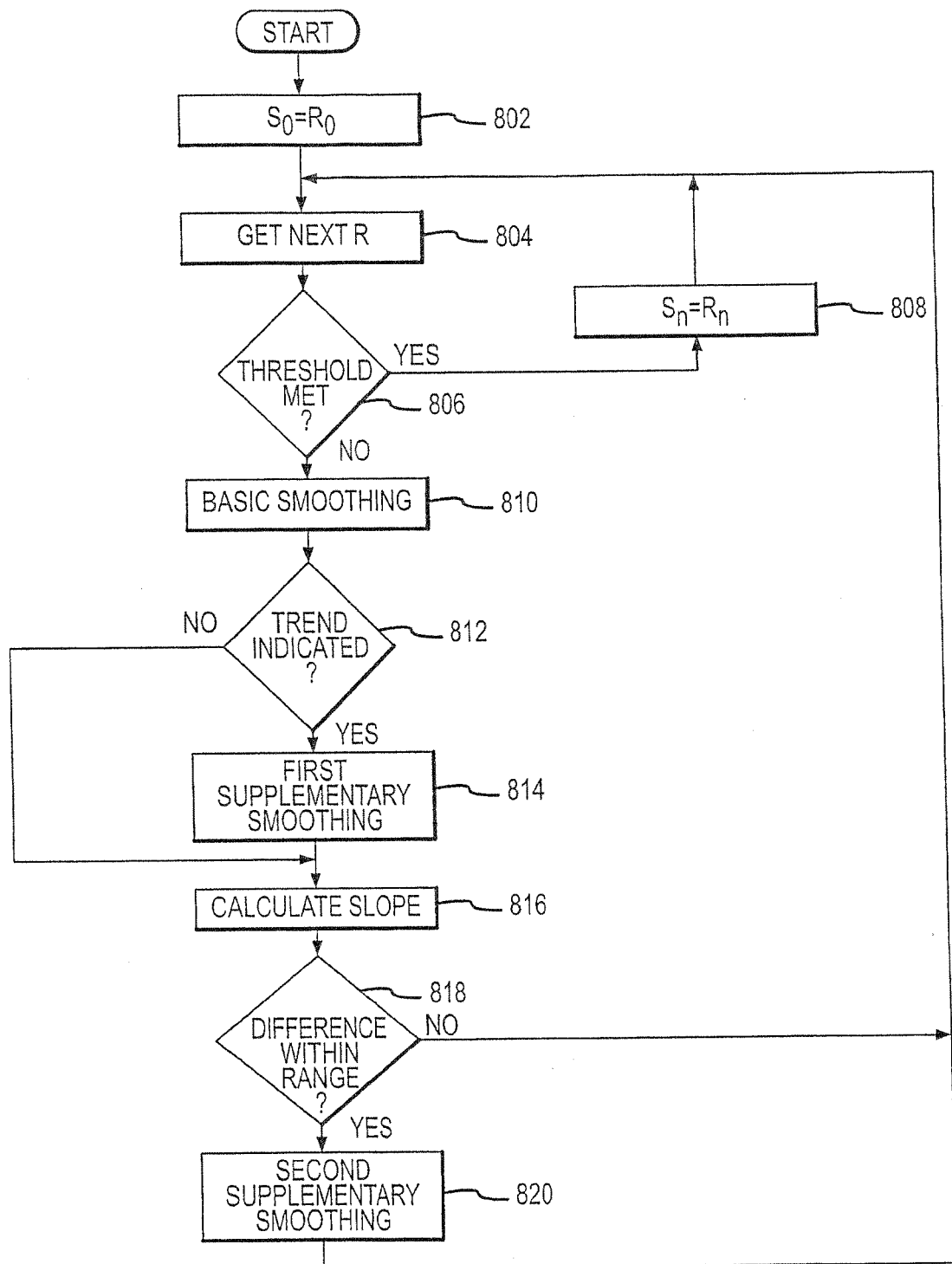


FIG.8

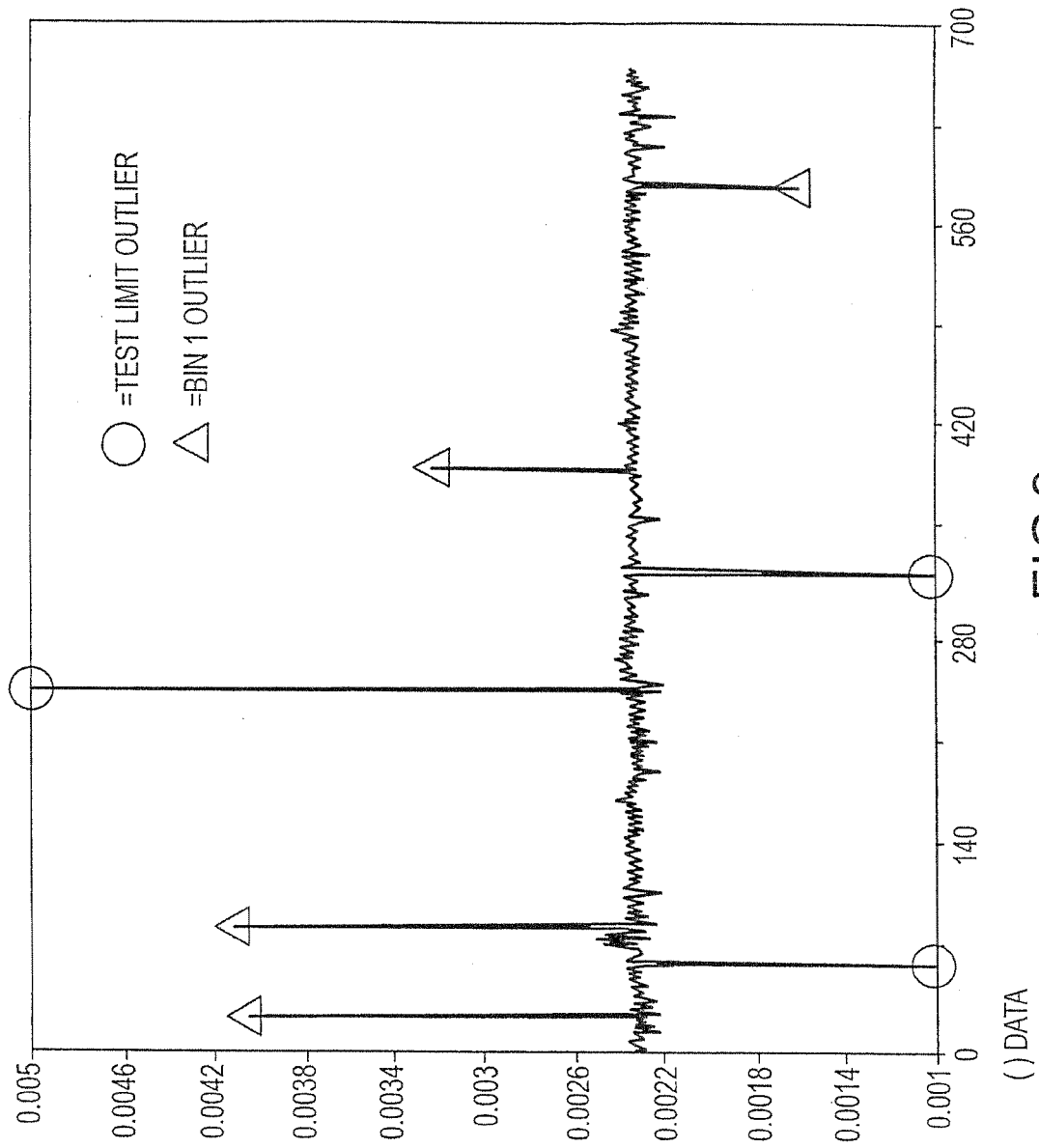


FIG.9

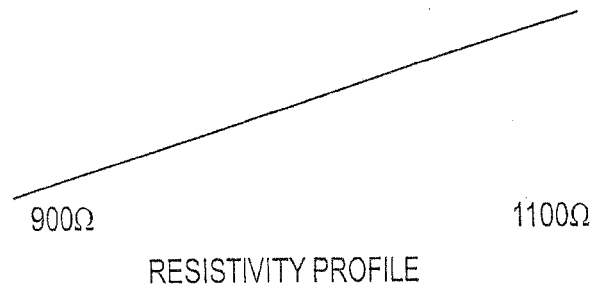
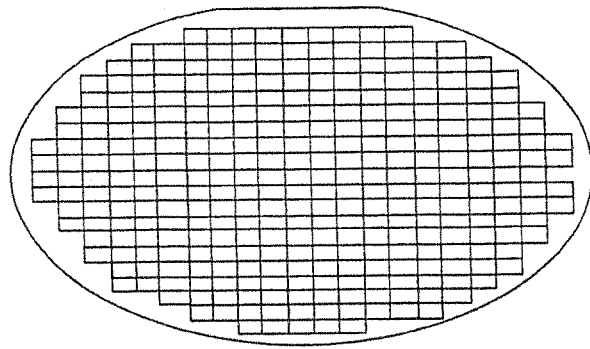


FIG.10

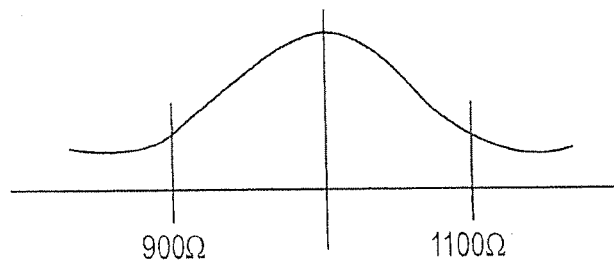


FIG.11

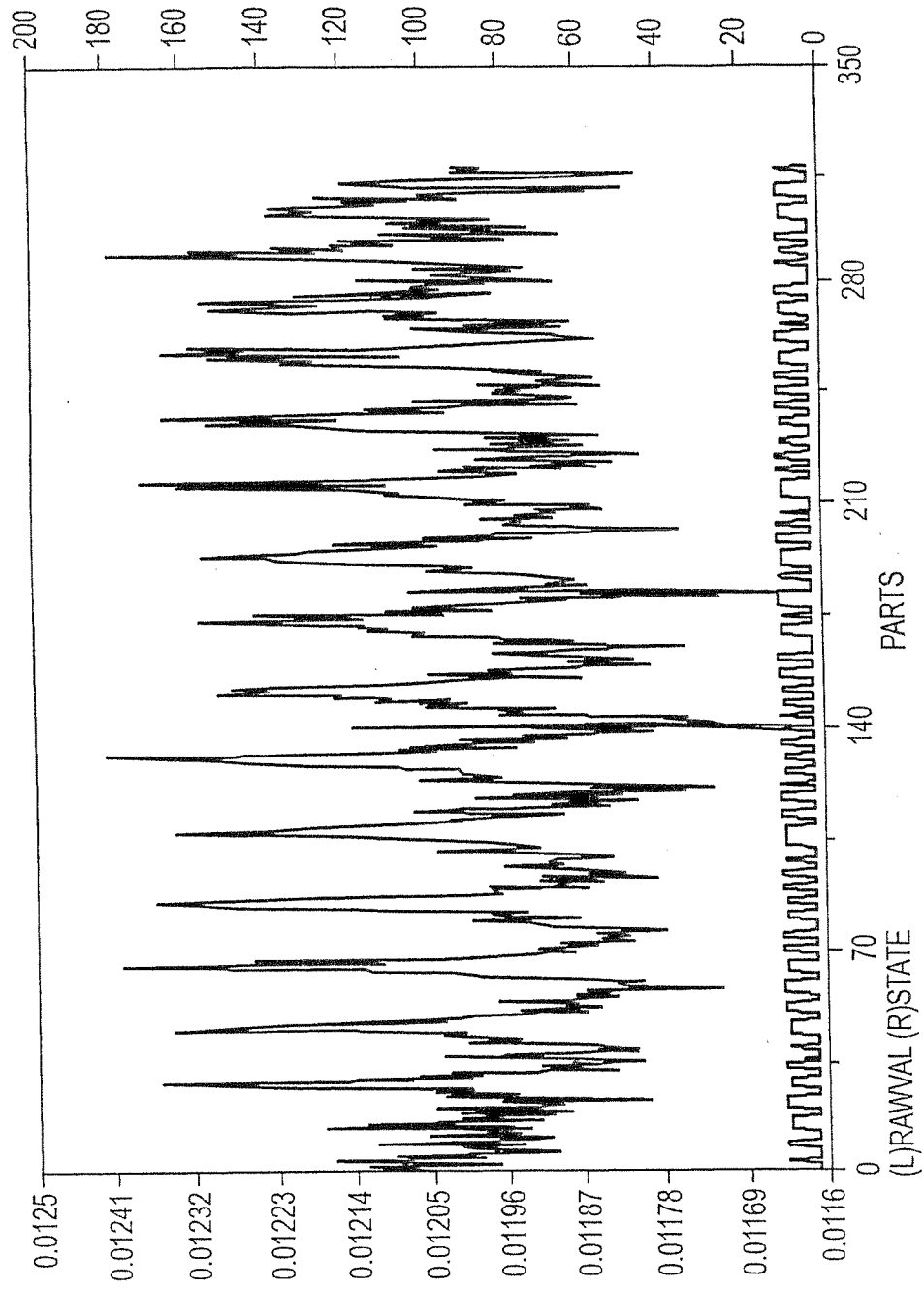


FIG.12A

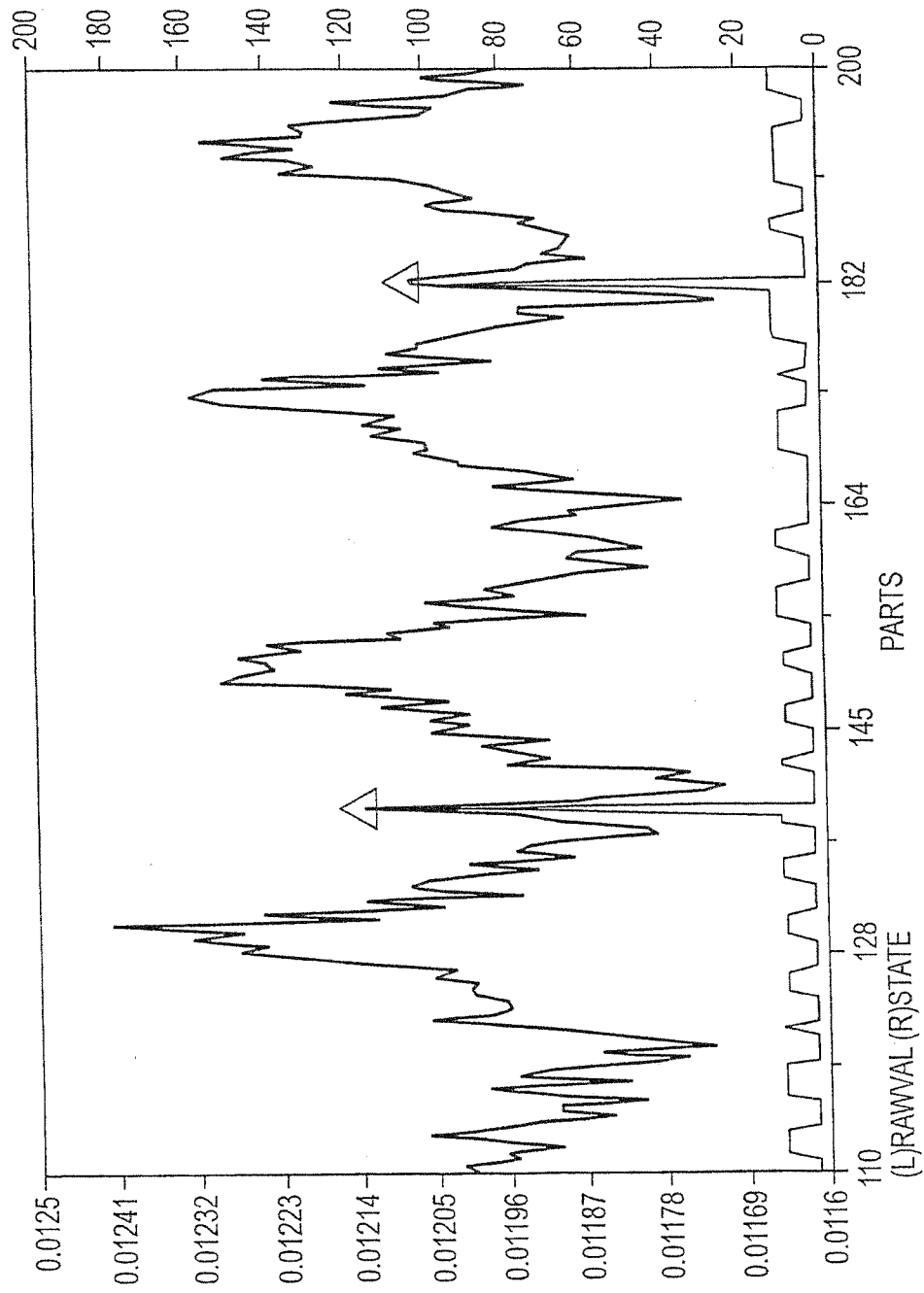


FIG.12B

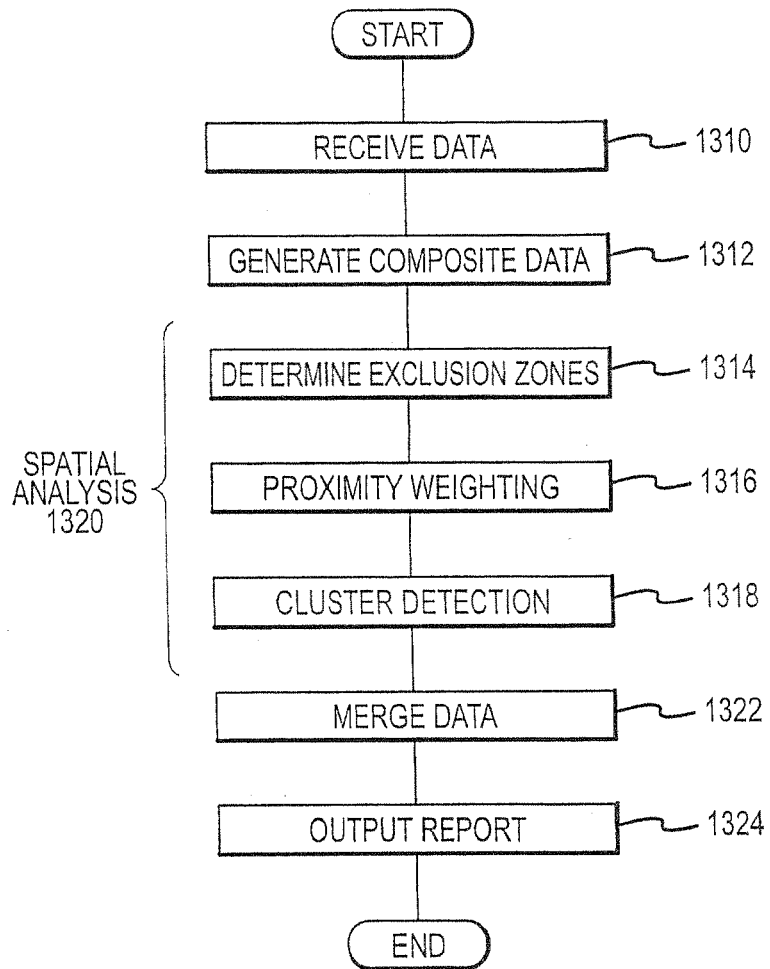


FIG.13

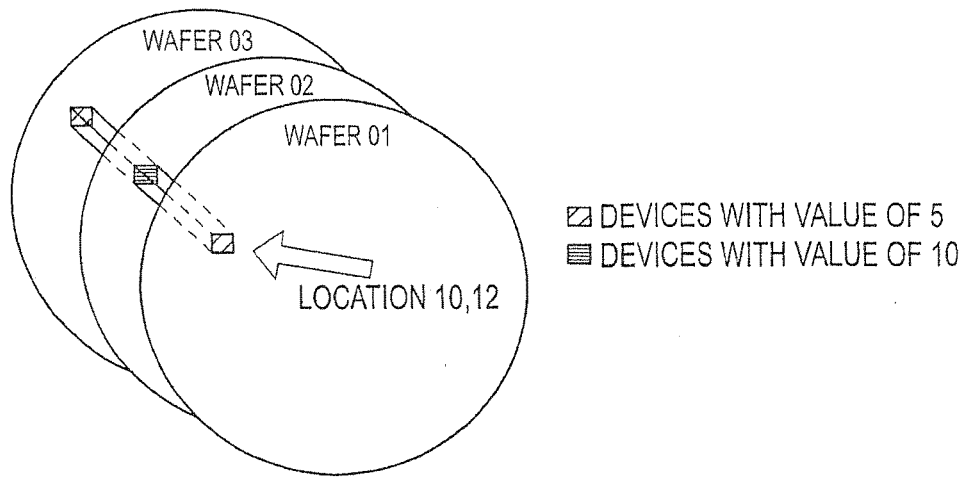


FIG.14

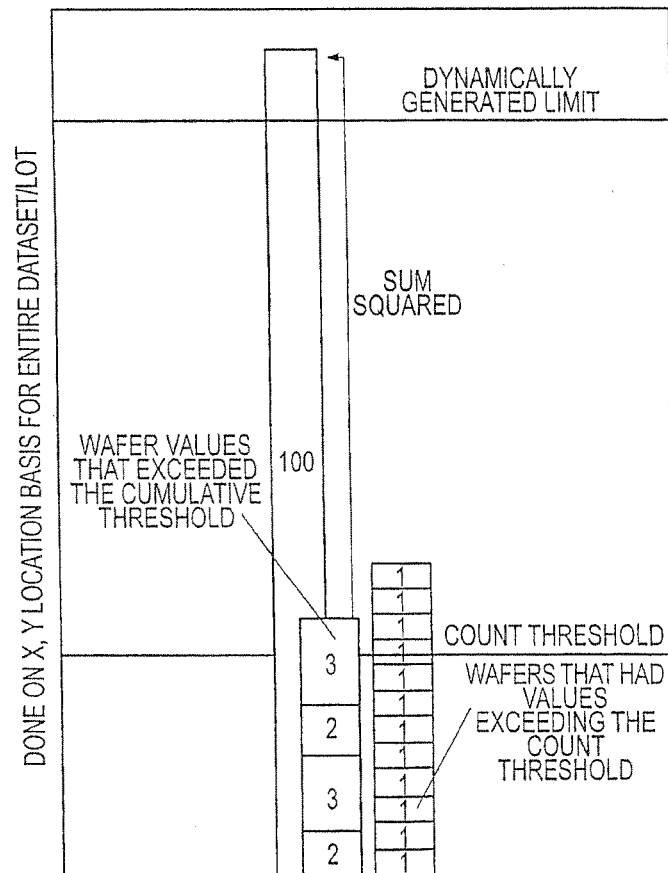


FIG.15C

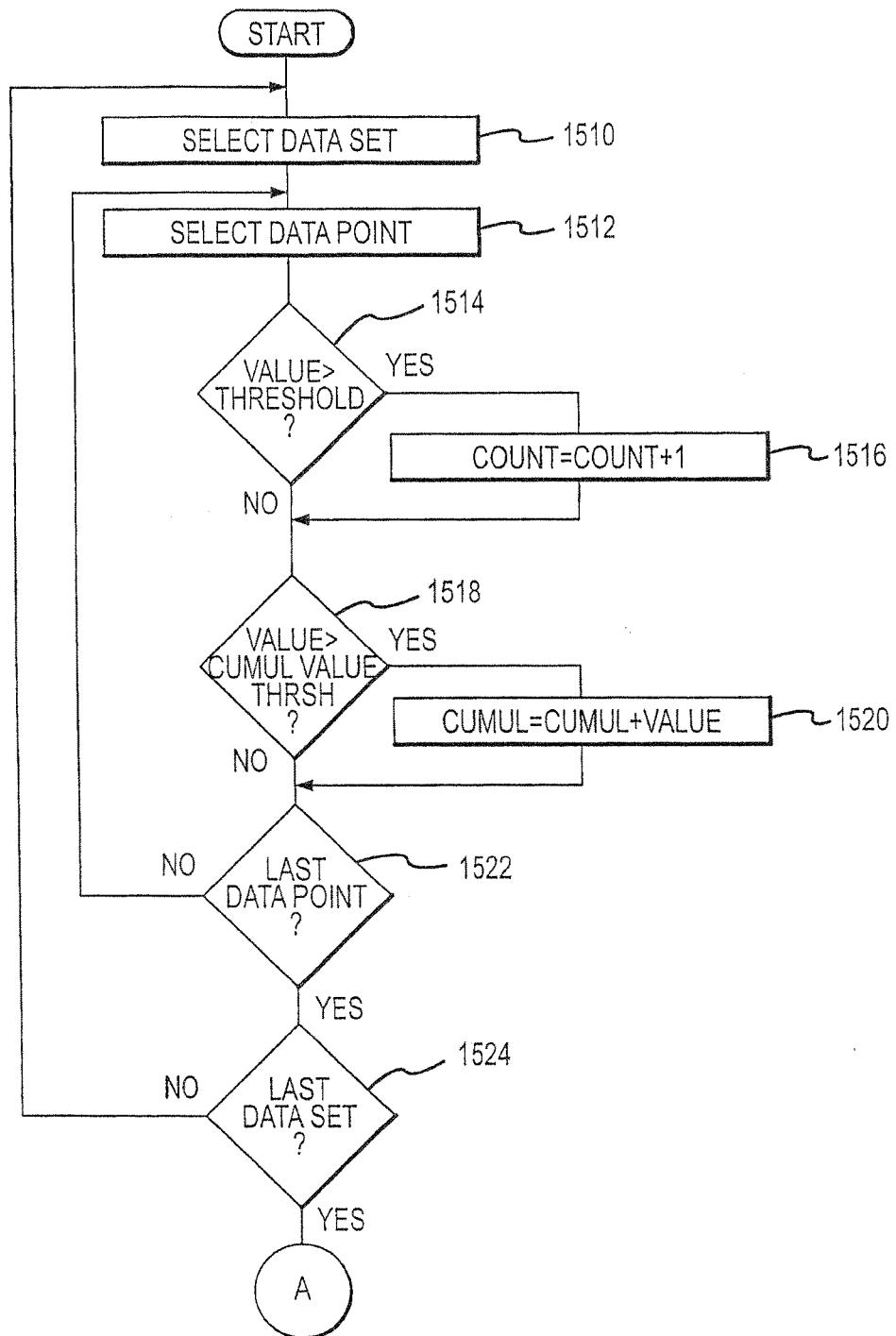


FIG. 15A

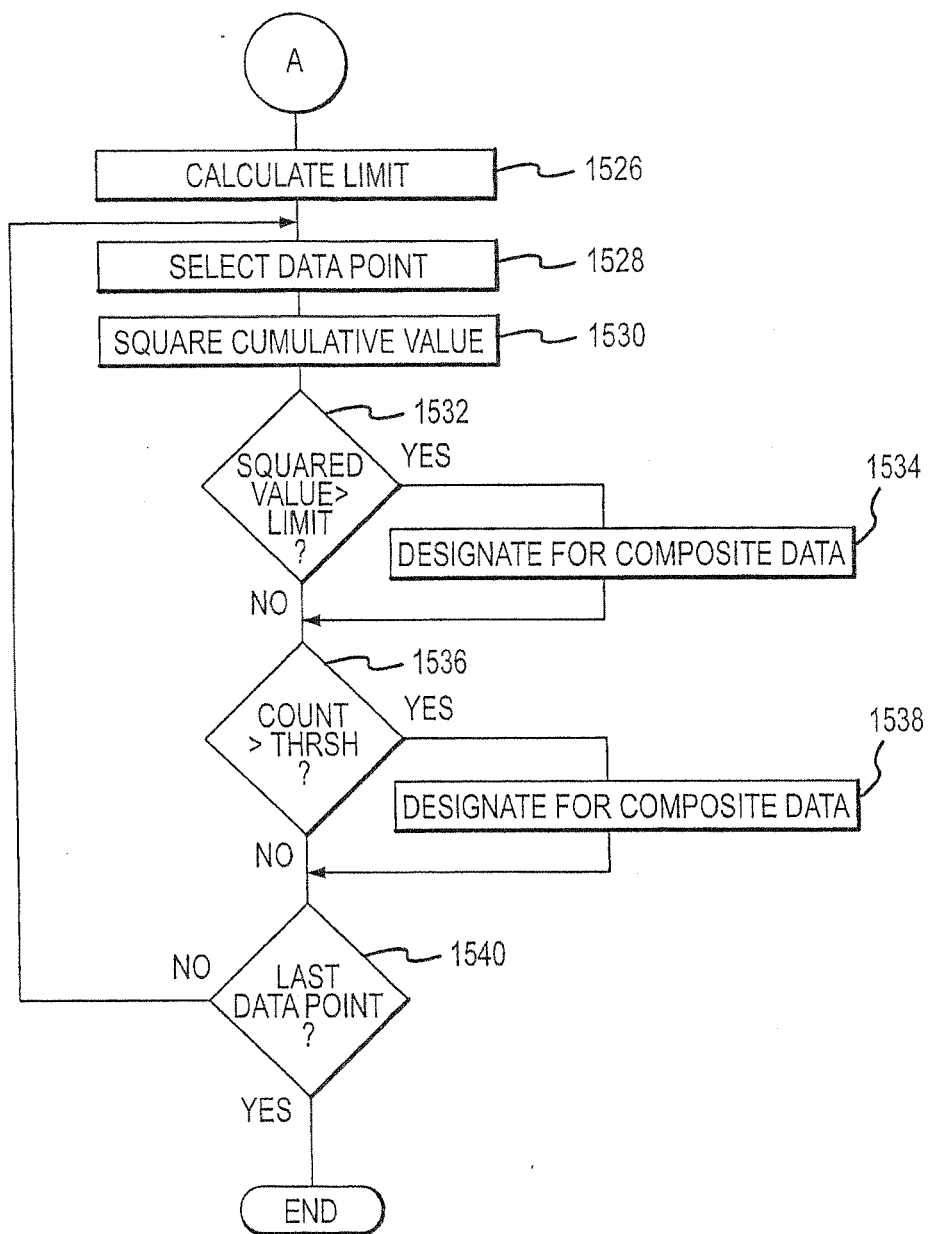


FIG.15B

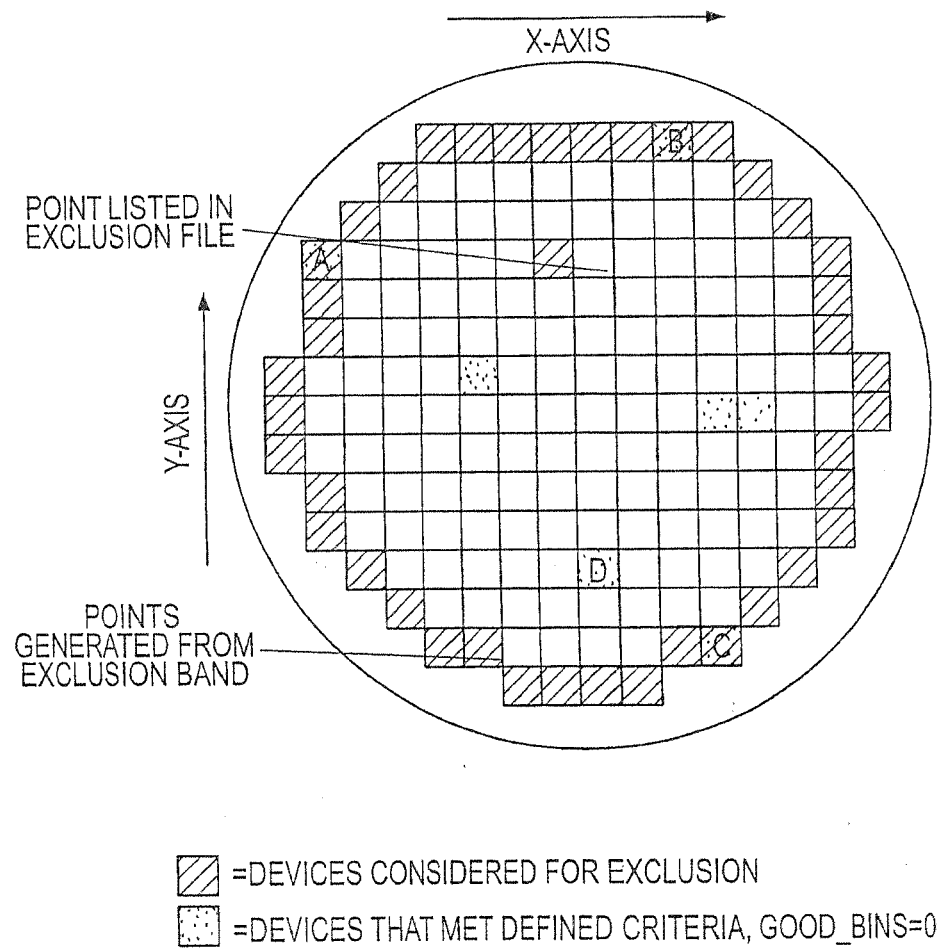


FIG.16

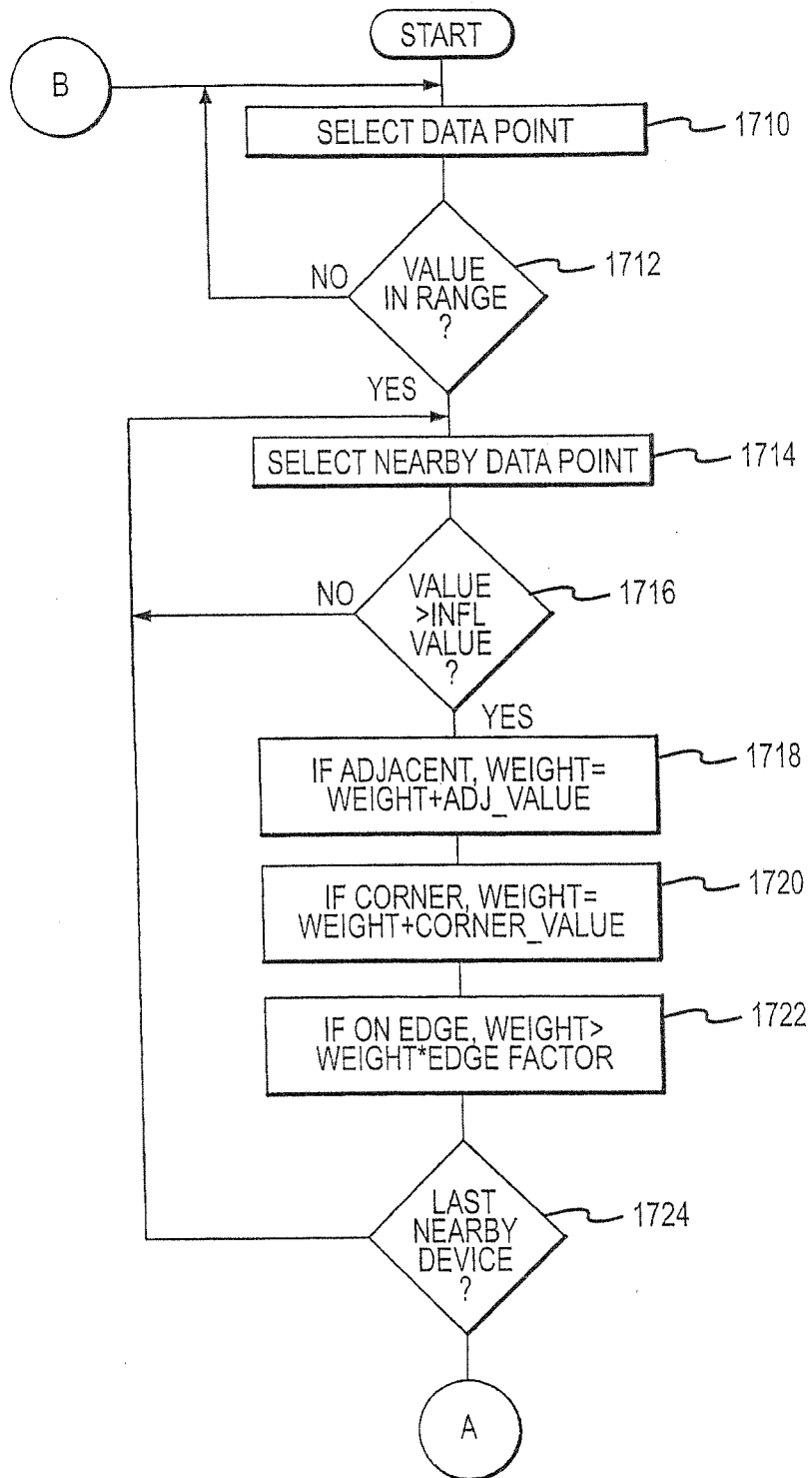


FIG.17A

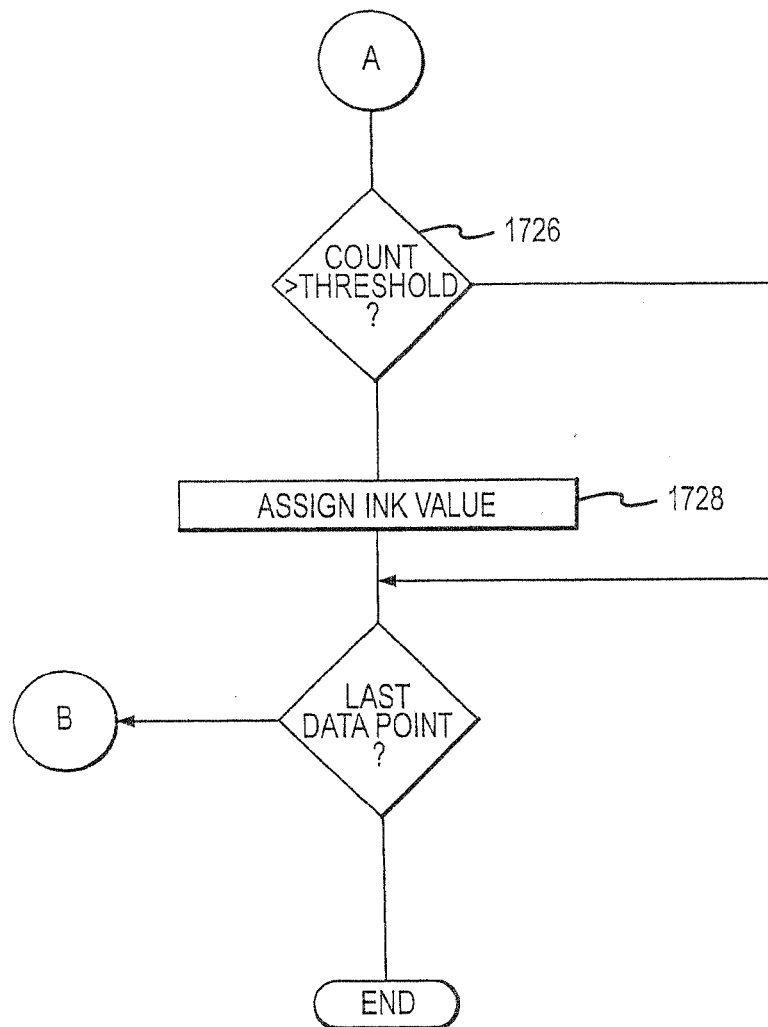


FIG.17B

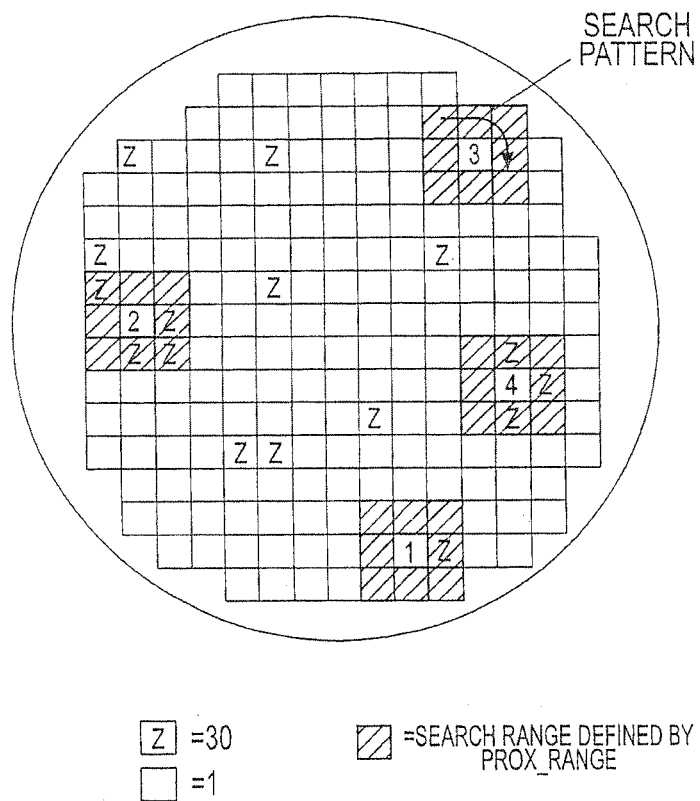


FIG.18

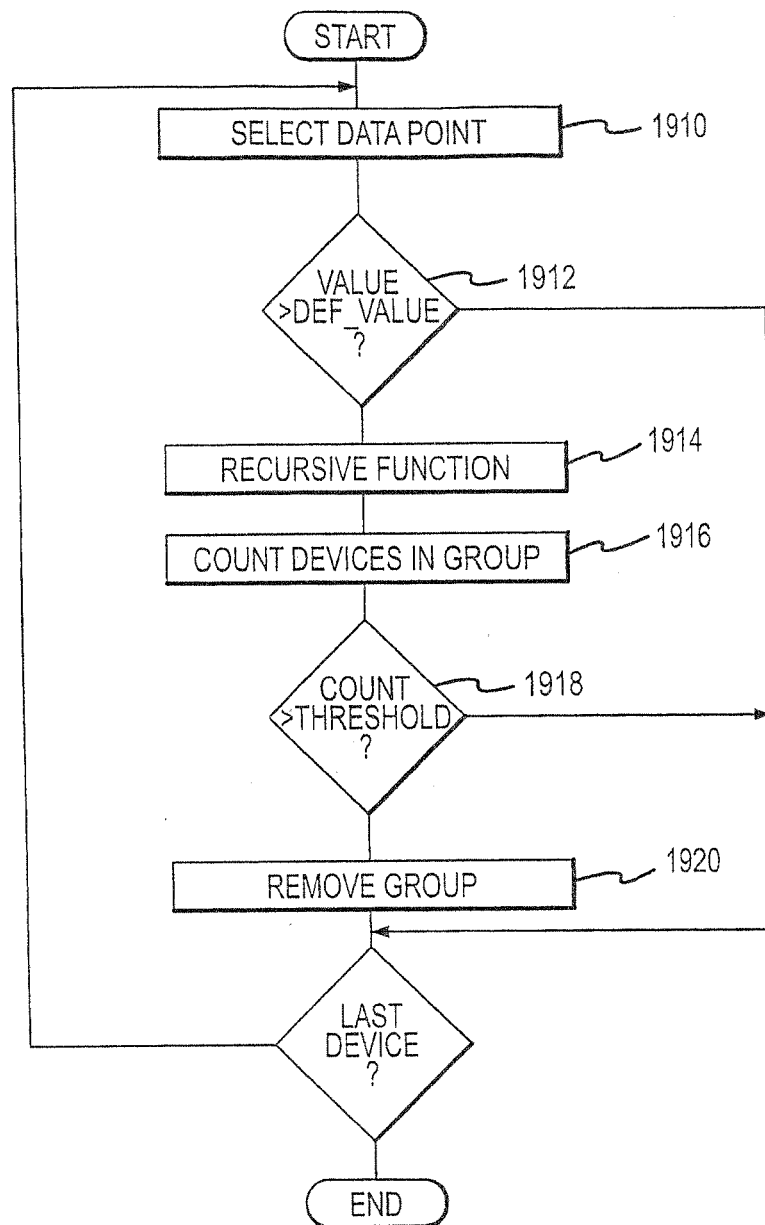
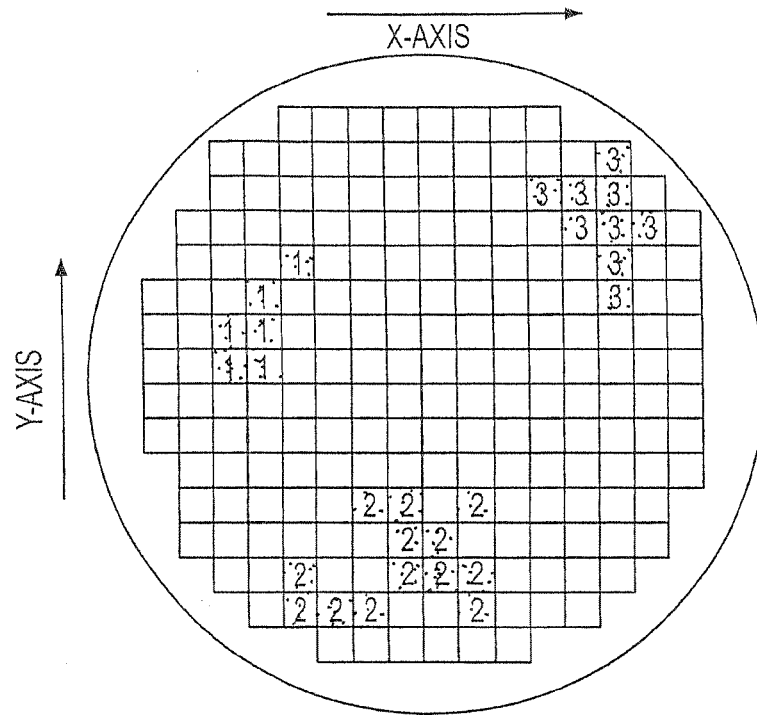


FIG. 19



 = DEVICES THAT HAVE VALUES MATCHING THE DEFINITION_VALUE
 = GROUP INDEX

FIG.20

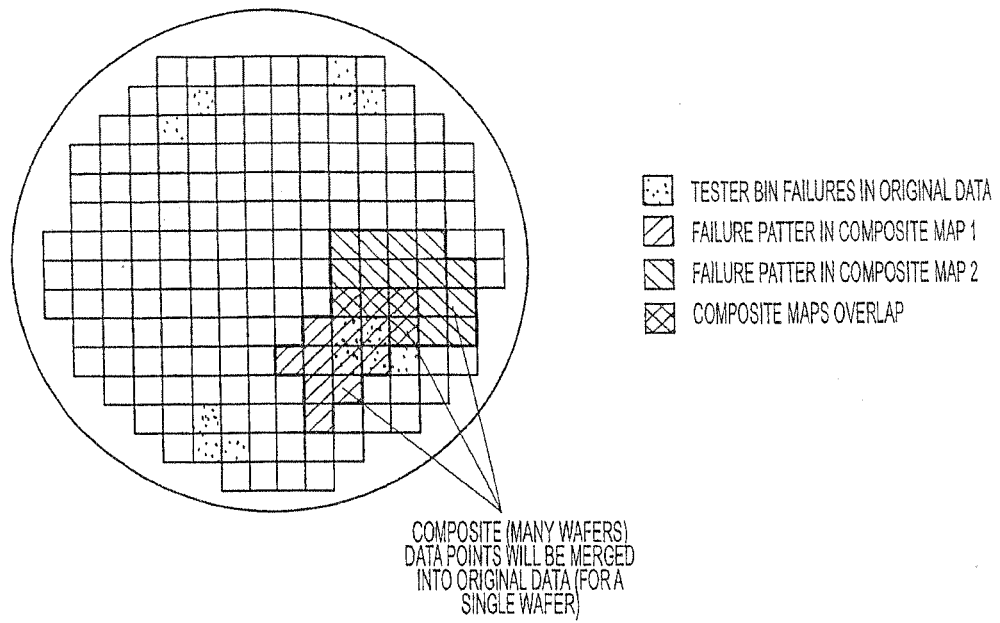


FIG.21

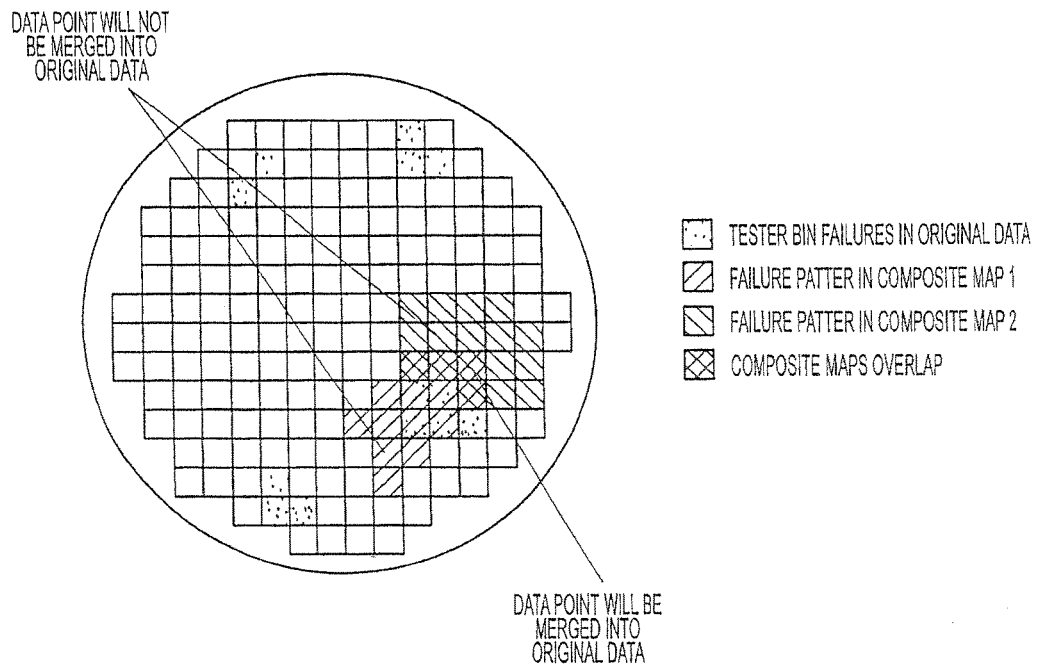


FIG.22

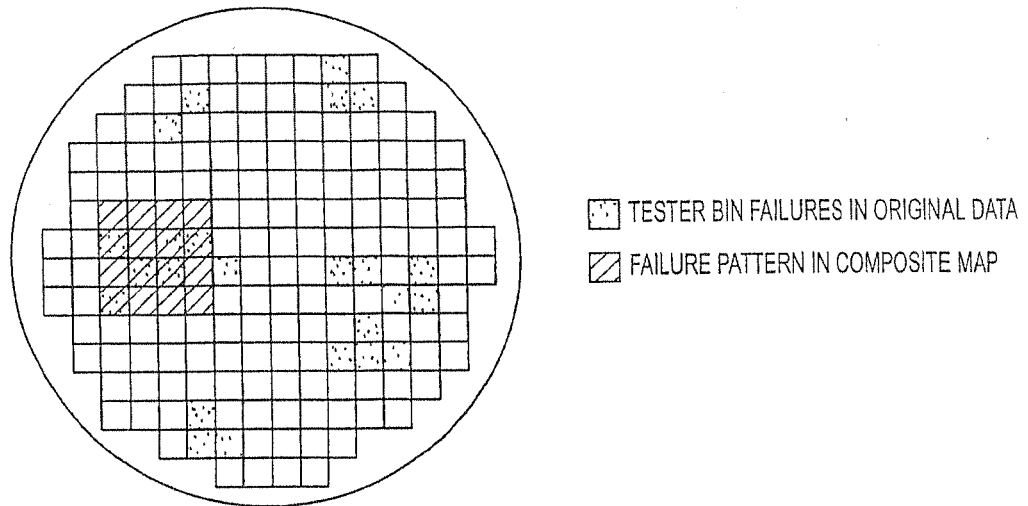


FIG.23

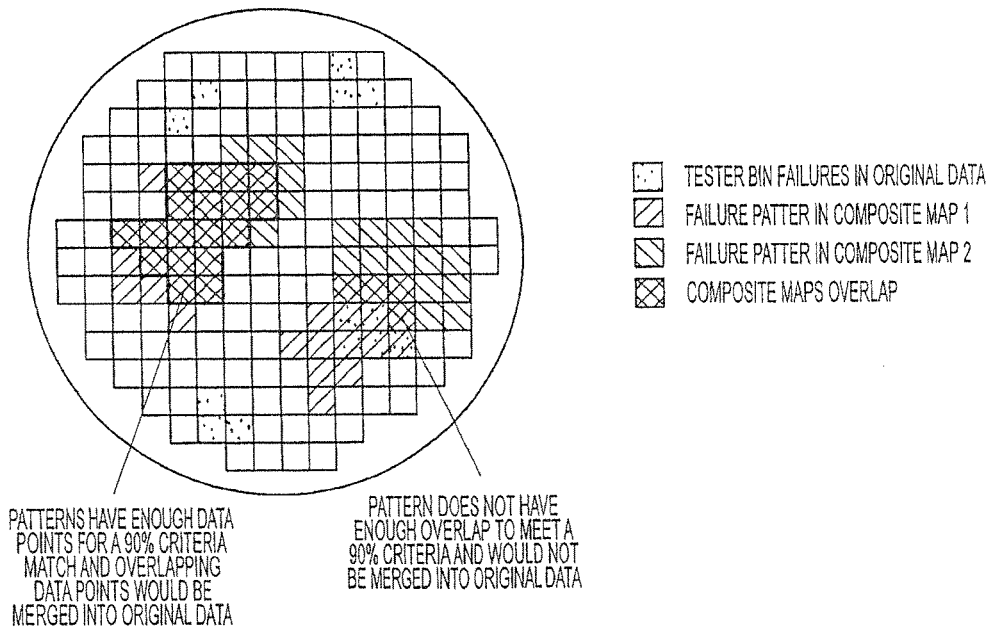


FIG.24

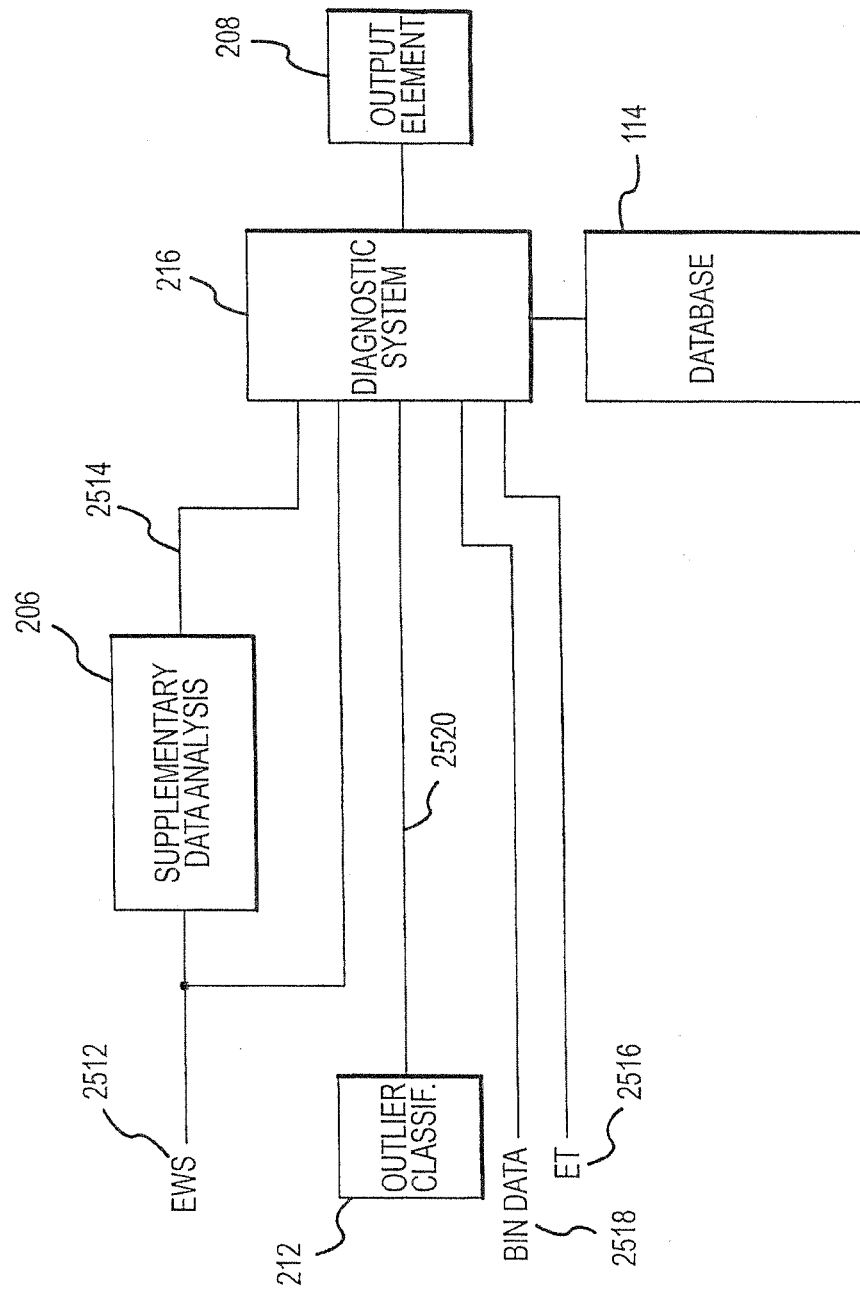


FIG.25

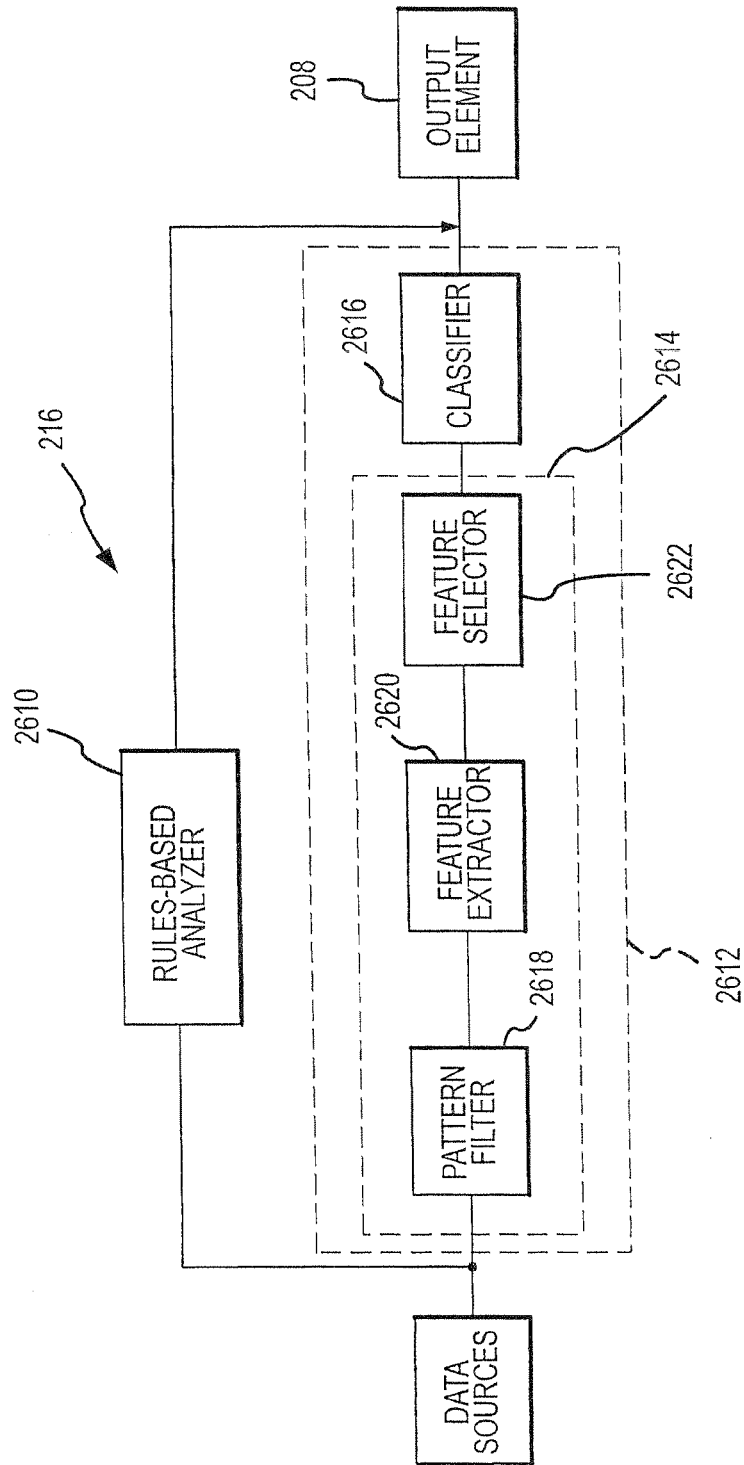


FIG.26

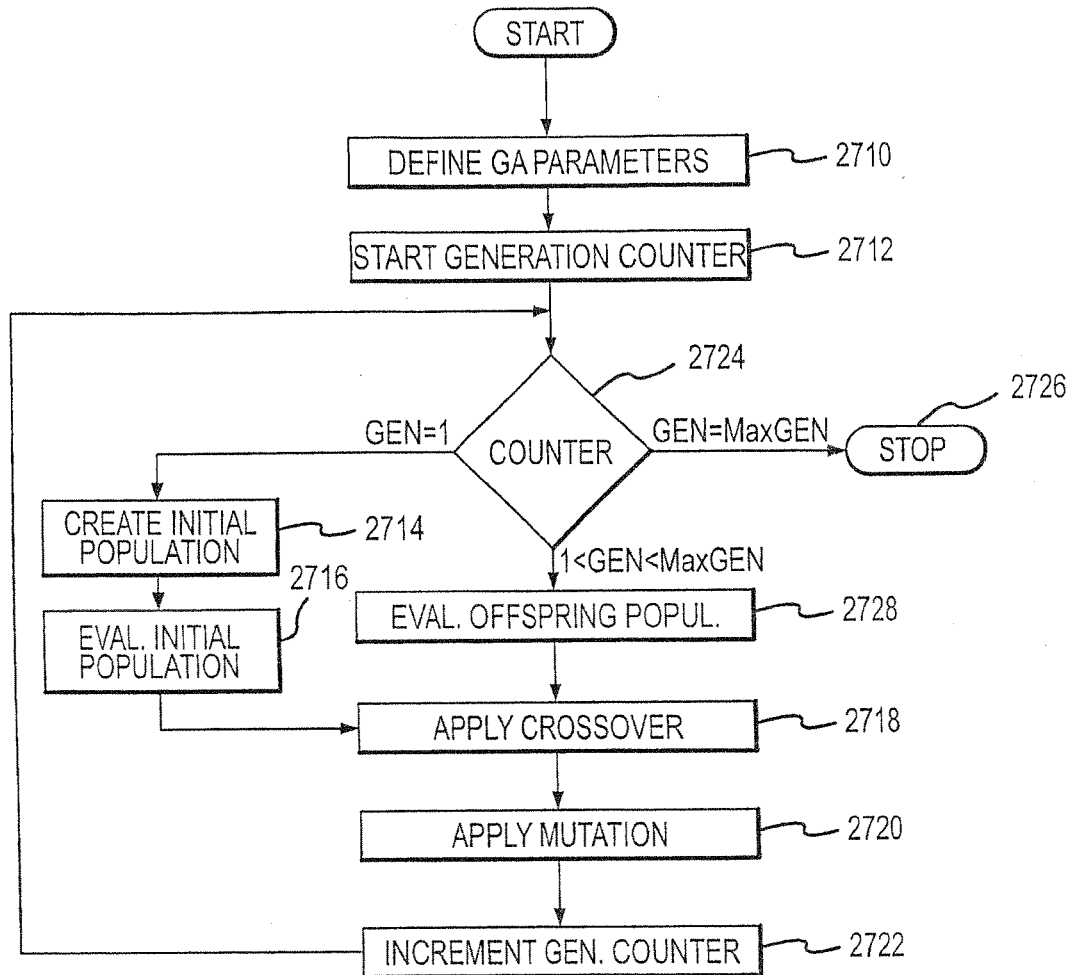


FIG.27

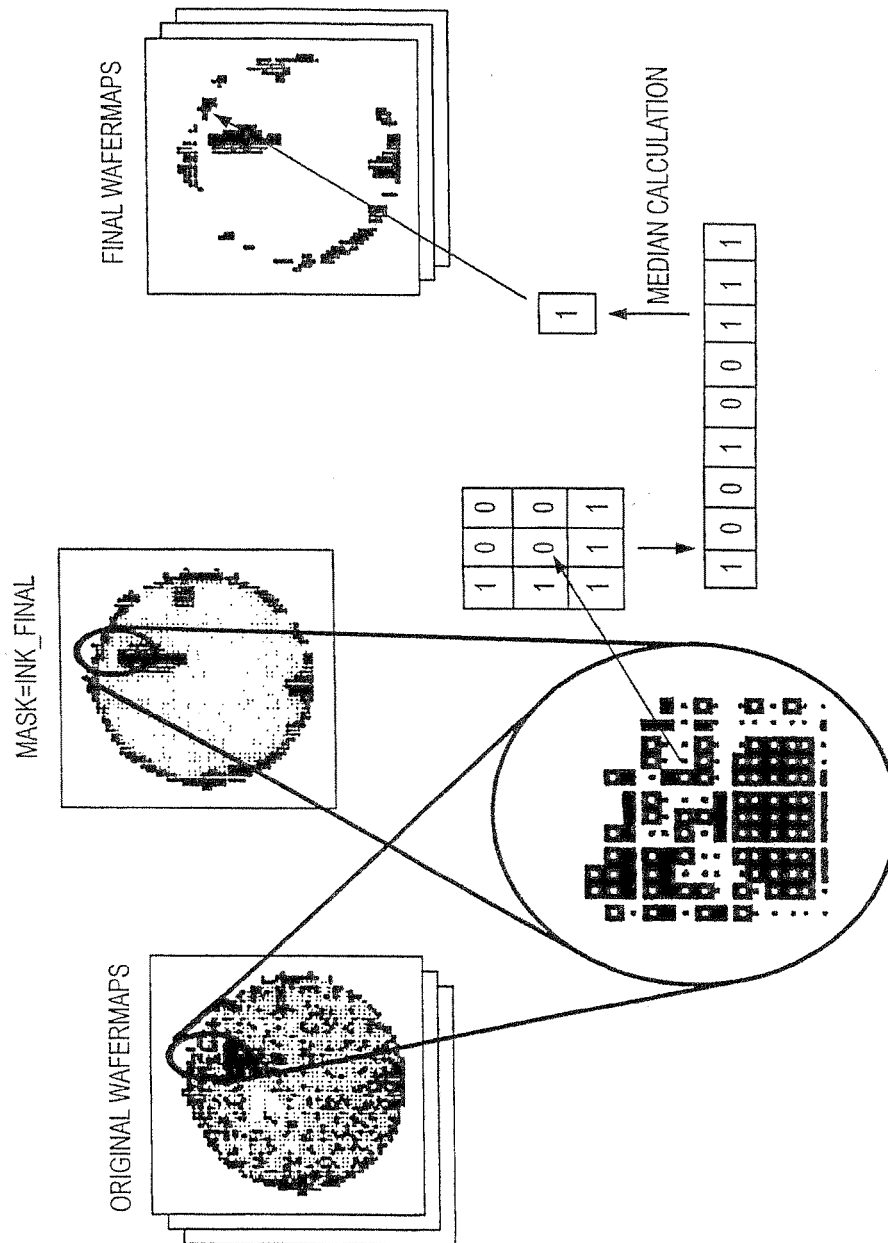


FIG.28

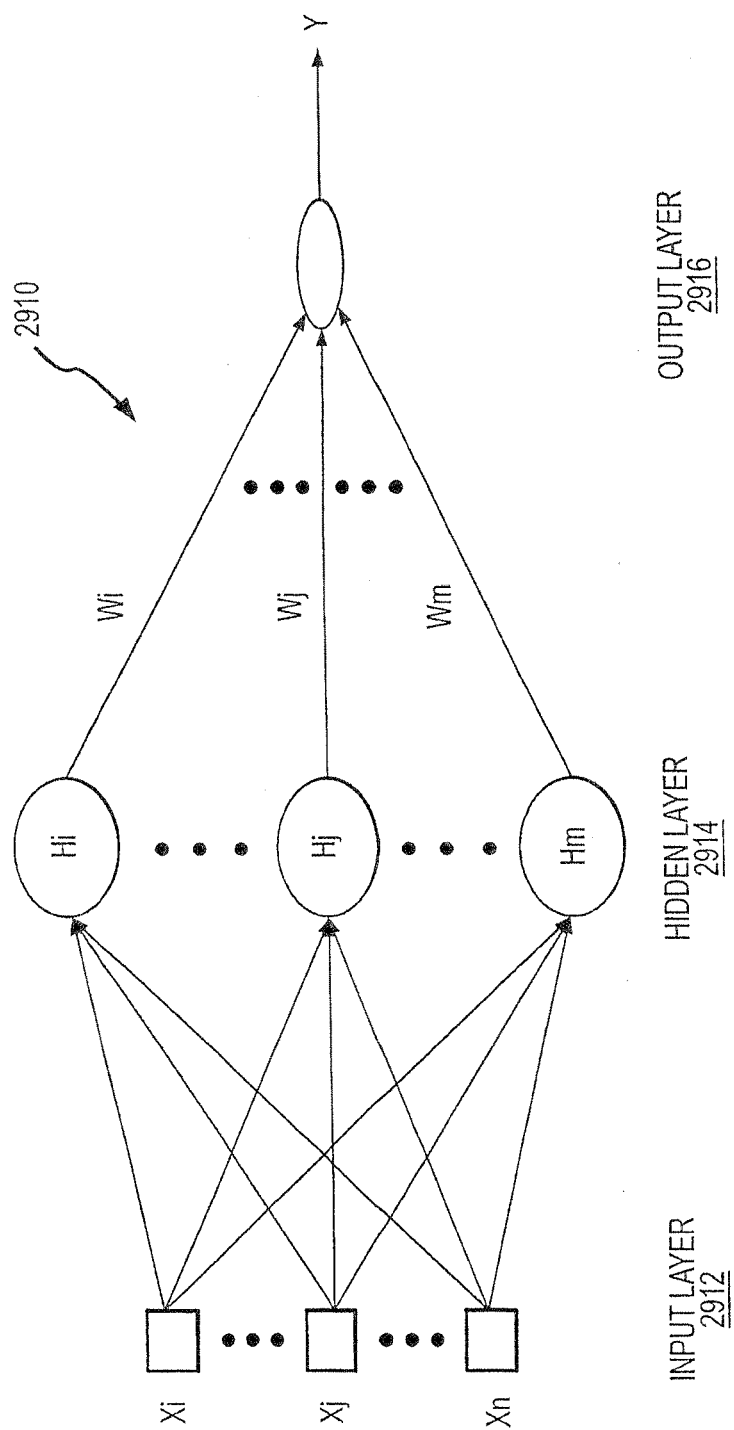


FIG.29

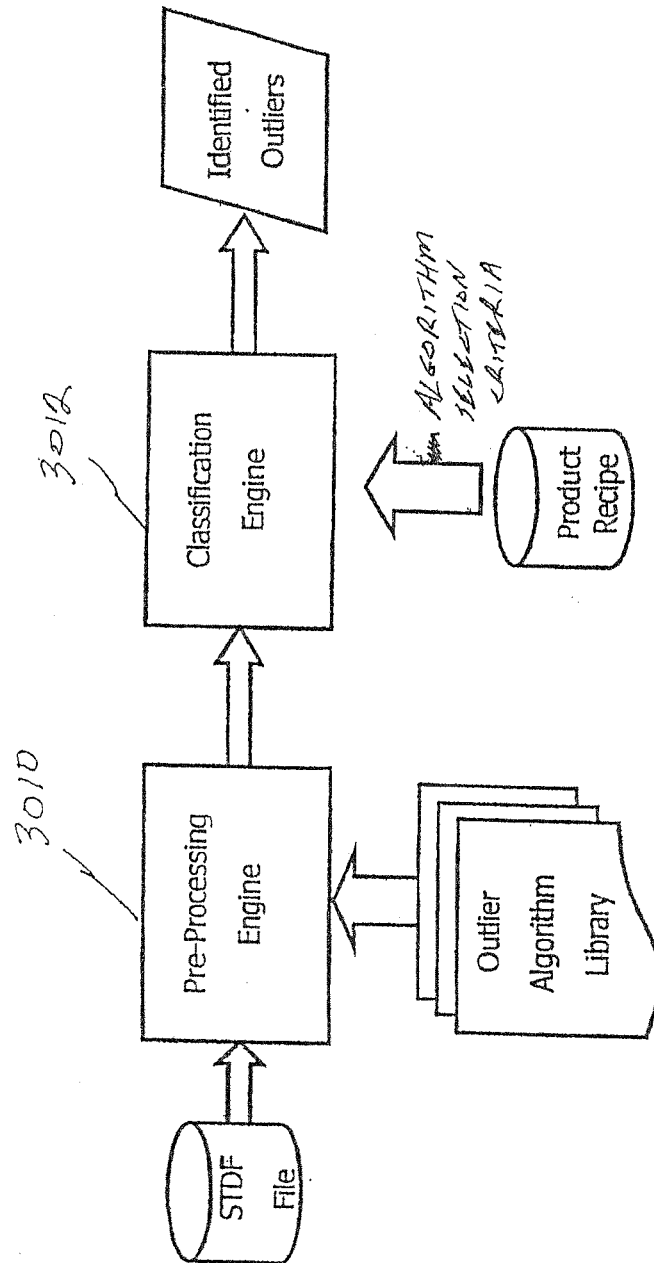


FIG. 30

Input Data - Scenarios Relation

	Residue	Probing Fault	Metal Bridging	Contamination
Yield Patt.	- Wipe Out - Bulls eye pattern - Good, bad, good again	- Wipe out - Row or part row - Initially good, then suddenly bad	- Wipe out - Wafer has a spotted face, and failures appear randomly across the surface	Usually confined to a part of the wafer, but could be present across the whole wafer if the problem is gross
PC Data	Nominal	Nominal	Nominal	- Could be nominal - CMOS, Vt shifts, increase leakage curr. Bipolar, reduced transistor hfe and low BV test
EWS Res.	- Continuity Test Fail (opens) - Some Supply Current Failures to low test lim.	- Continuity Test Fail. (opens) - Some Parametric Failures depending upon the degree of the problem	- Possible cont, test fail. (shorts) - Significantly high number of supply current failures (high limit)	- Possible cont. test failures - Significantly high supply current failures and IHH/III test failures
Bin Sign.	- Increase of bin 6 - Possibly some bin 10 failures	- Increase of bin 6 - Possibly some bin 10 - Also some bin 20	- Increase of bin 10 - Possible bin 6 failures	- Increased bin 10 - Also bin 12 - Possible bin 6
Outlier	Unlikely to provide useful info in affected areas	Unlikely to provide useful in affected areas, but if param. results are present in the EWS there could be increased signature activity and critical outliers detected	Generally would not expect to see increased signature bin activity	Possible some critical outlier in the results for good parts either side of the area of yield loss

FIG. 31A

Input Data - Scenarios Relation

	Scratches	Parametric Variation	Stepper/Reticle Problem
Yield Patt.	• Lines of adjacent failures not more than two die wide	• Bulls eye • Hot Spot • Half and half • Gradient • Crescent	• Repeated rows and columns across a wafer
PC Data	• Nominal unless a scratch passes through a test site	• Provided the critical parameter is measured, would expect a correlation with yield pattern.	• Depending upon the cause/location results could be nominal
EWS Res.	• Nominal in the not affected area. • Within, cont. and supply current failures.	• Nominal, out the yield pattern • Otherwise, majority of failures falling in one or two bins	• Nominal out the affected area • Otherwise, majority of failures falling in one or two bins: cont. or specific param. test
Bin Sign.	• Increased bin 6 • Possible bin 10 failures	• Increased bin 20/30 • Preceding bins will be nominal	• Increased count for the bin associated with failing test
Outlier	• Unlikely to provide useful info in affected areas	• Possible some critical outliers, in the results for good parts either side of the area of yield loss	• May increased signature bin activity including critical outliers, in the results for good parts either side of the area of yield loss

FIG. 31B

Stage 2. Classification

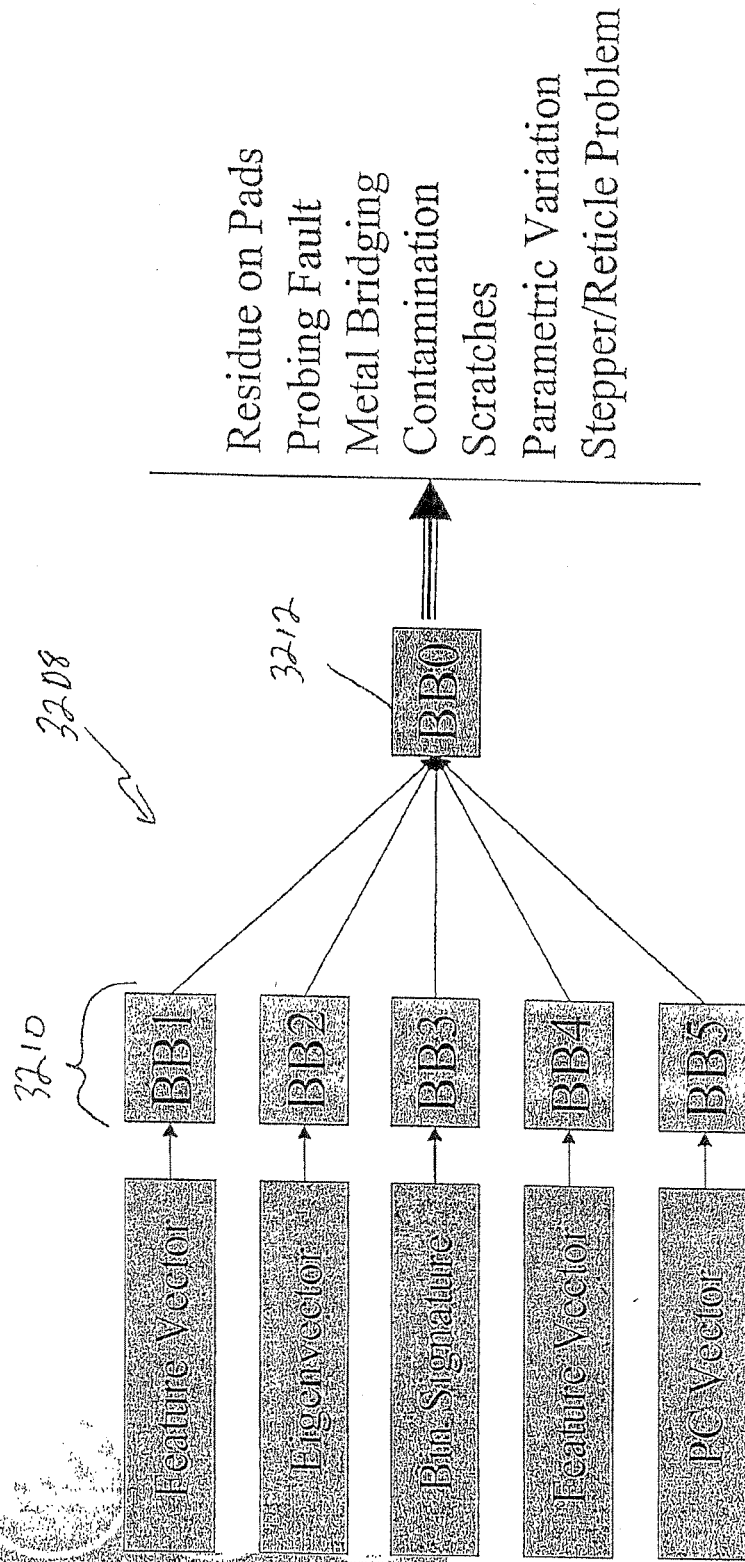


FIG. 32

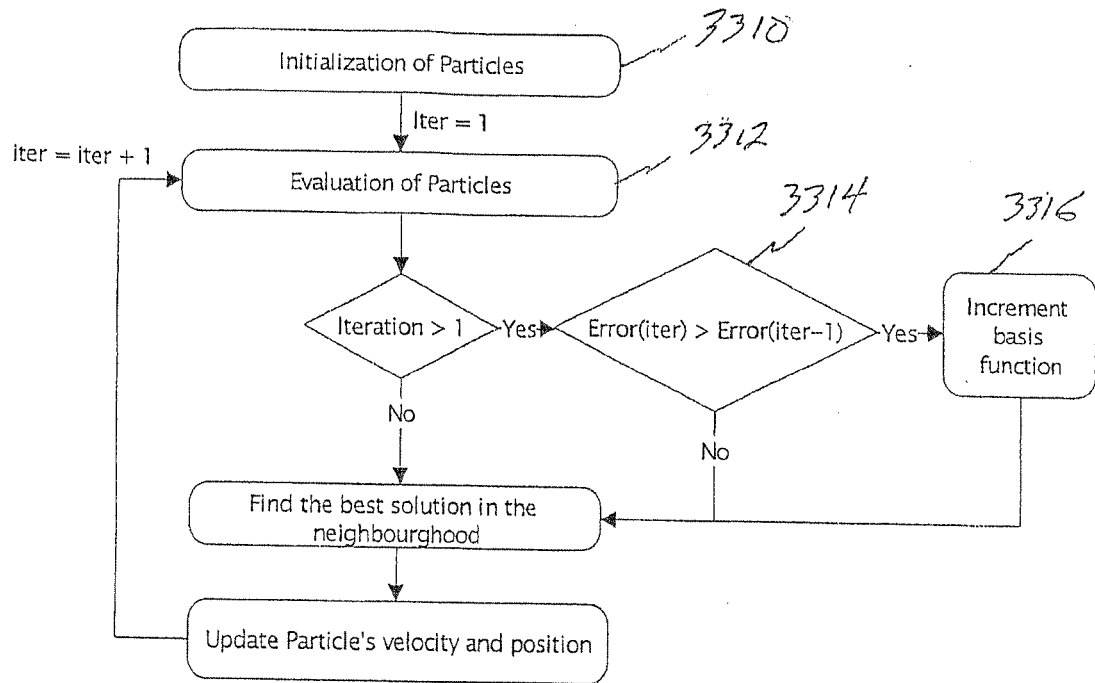


Figure 33