CLAIMS:

1. A method of manufacturing a ferrite rod usable for operation within the micro-wave and millimeter-wave regime, the method comprising the steps of:

etching (2690) a first cavity into a first surface of a first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1);

providing a first passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) at least at the first surface of the first semiconductor substrate in the first cavity;

depositing (2691) a first ferrite layer (310, 410, 610, 810, 1010, 1210) into the first cavity;

etching (2692) a second cavity into a second surface of a second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2);

providing a second passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) at least at the second surface of the second semiconductor substrate in the second cavity;

depositing (2693) a second ferrite layer (310, 410, 610, 810, 1010, 1210) into the second cavity;

attaching (2694) the first surface of the first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1) to the second surface of the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2) such that the first ferrite layer (310, 410, 610, 810, 1010, 1210) contacts the second ferrite layer (310, 410, 610, 810, 1010, 1210) to form a Faraday rotation or phase-shifting element.

2. The method of claim 1, wherein said etching the first cavity into the first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1) and said etching the second cavity into the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2) each comprise:

performing isotropic semiconductor etching to selectively remove a layer of the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2).

3. The method of claim 1, wherein etching the first cavity into the first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1) and providing a first passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) at least at the first surface of the first semiconductor substrate in the first cavity and etching the second cavity into the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2) and providing a second passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) at least at the second surface of the second semiconductor substrate in the second cavity each comprise:

growing a temporary passivation layer (102, 204) on the semiconductor substrate;

applying a resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203) to the temporary passivation layer (102, 204);

performing a lithography and developing step to selectively remove the resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203);

performing a first etching step to selectively remove the temporary passivation layer (102, 204);

stripping the resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203) from the temporary passivation layer (102, 204);

performing isotropic semiconductor etching to selectively remove a layer of the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2);

stripping the temporary passivation layer (102, 204); and

growing a final passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205).

4. The method of claim 3, wherein said first etching step comprises an anisotropic etching step, and wherein said growing a temporary passivation layer (102, 204) comprises

thermally oxidising the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2) such that the temporary passivation layer comprises a first oxidation layer (102); and/or

applying low-stress low-pressure chemical vapour deposition to the semiconductor substrate such that the temporary passivation layer comprises a nitride layer (204).

5. The method of claim 1, wherein said depositing a ferrite layer (310, 410, 610, 810, 1010, 1210) into the cavity comprises:

arc plasma spraying of the ferrite layer (310, 410, 610, 810, 1010, 1210) in powder form; and/or

performing wet chemical deposition of the ferrite layer (310, 410, 610, 810, 1010, 1210).

6. The method of claim 5, wherein said depositing a ferrite layer (310, 410, 610, 810, 1010, 1210) into the cavity further comprises:

annealing of the ferrite layer (310, 410, 610, 810, 1010, 1210);

chemical mechanical polishing of the ferrite layer (310, 410, 610, 810, 1010, 1210) and/or

hot phosphoric acid wet etching of the ferrite layer (310, 410, 610, 810, 1010, 1210).

7. The method of claim 2, wherein attaching the first surface of the first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1) to the second surface of the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2) comprises, for at least one semiconductor substrate of the first and second semiconductor substrates (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2):

applying a resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203) to a surface of the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2) comprising the first or second cavity;

performing a lithography and developing step to selectively remove the resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203);

performing a first etching step to selectively remove at least a part of the passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205);

stripping the resist coating (103, 203, 403, 503, 603, 703, 803, 903, 1003, 1103, 1203) from the surface of the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2);

assembling the first and second semiconductor substrates (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2) such that the respective first and second surfaces face each other.

8. The method of claim 7, wherein the method further comprises, before assembling the first and second semiconductor substrates and after strippping the resist coating, the steps of chemical mechanical polishing of the first surface of the first semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1);

applying a second resist coating (503, 703, 903);

performing a lithography and developing step to selectively remove the second resist coating; and

heating the assembled structure comprising the first and second semiconductor substrates (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2).

9. The method of claim 8, wherein the method further comprises, after strippping the resist coating, the step of

depositing a gold and adhesion layer (420, 720, 820, 1120) on the second surface of the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2);

after selectively removing the second resist coating etching the gold and adhesion layer (420, 720, 820, 1120); and

stripping the second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203);

wherein said heating the assembled structure comprises heating the assembled structure to create eutectic Gold:Silicon bonds (425, 725).

10. The method of claim 8, wherein the method further comprises, after selectively removing the second resist coating, the steps of

depositing a gold and adhesion layer (420, 720, 820, 1120) on the second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203) and on the second surface of the second semiconductor substrate (401-2, 601-2, 801-2, 1001-2, 1201-2); and

lifting off the second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203);

wherein said heating the assembled structure comprises heating the assembled structure to create eutectic Gold:Silicon bonds (425, 725).

11. The method of claim 7, wherein the method further comprises, before assembling the first and second semiconductor substrates and after strippping the resist coating, the steps of

applying a second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203);

performing a lithography and developing step to selectively remove the second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203); and

applying heat and pressure to the assembled structure comprising the first and second semiconductor substrates (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2).

12. The method of claim 11, wherein the method further comprises the steps of

depositing a gold and adhesion layer (420, 720, 820, 1120) on the respective first or second surface after strippping the resist coating, wherein said applying a second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203) comprises applying a second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203) to the gold and adhesion layer (420, 720, 820, 1120); and

etching the gold and adhesion layer (420, 720, 820, 1120) ;

wherein the method further comprises the step of stripping of the second resist coating (403, 503, 603, 703, 803, 903, 1003, 1103, 1203) after etching the gold and adhesion layer;

wherein said applying heat and pressure to the assembled structure comprises applying heat and pressure to the assembled structure to create Gold:Gold bonds (930, 1130).

13. The method of claim 7, wherein the method further comprises,after strippping the resist coating, applying a glue layer (1240) on the respective first or second surface; and curing the glue layer (1240).

~~14. A ferrite rod (310, 410, 610, 810, 1010, 1210) usable for operation within the micro-wave and millimeter-wave regime comprising:~~

~~a first ferrite layer (310, 410, 610, 810, 1010, 1210) and a second ferrite layer (310, 410, 610, 810, 1010, 1210);~~

~~wherein a first surface of the first ferrite layer is in direct contact with a first surface of the second ferrite layer and wherein the ferrite rod further comprises a passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) arranged at a second surface of the first~~

~~ferrite layer (310, 410, 610, 810, 1010, 1210) and the second ferrite layer (310, 410, 610, 810, 1010, 1210), respectively, weherein the ferrite rod forms a Faraday rotation or phase-shifting element.~~

~~15.~~ An electronic device usable within the micro-wave and millimeter-wave regime comprising:

a semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2); and

a ferrite rod (310, 410, 610, 810, 1010, 1210) ~~A ferrite rod (310, 410, 610, 810, 1010, 1210)~~ usable for operation within the micro-wave and millimeter-wave regime comprising:

a first ferrite layer (310, 410, 610, 810, 1010, 1210) and a second ferrite layer (310, 410, 610, 810, 1010, 1210);

wherein a first surface of the first ferrite layer is in direct contact with a first surface of the second ferrite layer and wherein the ferrite rod further comprises a passivation layer (105, 205, 305, 405, 605, 805, 1005, 1205) arranged at a second surface of the first ferrite layer (310, 410, 610, 810, 1010, 1210) and the second ferrite layer (310, 410, 610, 810, 1010, 1210), respectively, weherein the ferrite rod forms a Faraday rotation or phase-shifting element~~.~~

~~according to claim 14~~; and

wherein the ferrite rod (310, 410, 610, 810, 1010, 1210) is integrated in the semiconductor substrate (101, 201, 301, 401-1, 601-1, 801-1, 1001-1, 1201-1, 401-2, 601-2, 801-2, 1001-2, 1201-2).

1~~5~~6. An electronic device device as claimed in claim 1~~4~~5, wherein the ferrite rod is integrated in the semiconductor substrate according to any one of the method claims 1 to 13~~.~~.

1~~6~~7. An electronic device as claimed in any of the claims 1~~4~~5 ~~t~~or 1~~5~~6, wherein the electronic device comprises a phase shifting device that includes the ferrite rod.