CLAIMS

We claim:

1. A method for processing a silicon substrate, comprising:

applying an anisotropic etchant to a surface of the silicon substrate, the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

forming an indentation on the surface of the silicon substrate with the applied anisotropic etchant, the indentation being defined by at least one plane with a Si(1,1,1) lattice orientation; and

forming a light emitting diode structure on the at least one plane with the Si(1,1,1) lattice orientation of the indentation.

2. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is greater than about 100 microns; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic

chemical vapor deposition (MOCVD), the N-type GaN, InGaN, and P-type GaN materials having surfaces generally conforming to the zigzag pattern of the first and second Si(1,1,1) planes.

3. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is less than about 1 micron; and

forming a light emitting diode structure includes:

depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic chemical vapor deposition (MOCVD); and

coalescing at least one of the N-type GaN, InGaN, and P-type GaN materials during the MOCVD operation.

4. The method of claim 1 wherein

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH),

ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence.

5. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane, a second Si(1,1,1) plane, and a Si(1,0,0) plane extending between the first and second Si(1,1,1) planes.

6. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane and a second Si(1,1,1) plane intercepting the first Si(1,1,1) plane at a junction.

7. The method of claim 1 wherein forming a light emitting diode structure includes depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the at least one plane of the indentation in sequence, the plane having the Si(1,1,1) lattice orientation.

8. The method of claim 1 wherein:

forming an indentation includes forming an indentation extending toward the silicon substrate from the surface to a depth; and

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a desired value of the depth.

9. A method for processing a silicon substrate, comprising:

reacting a surface of a silicon substrate with an anisotropic etchant, at least a portion of the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

removing silicon material from the surface of the silicon substrate along a Si(1,0,0) plane faster than along a Si(1,1,1) plane, thereby exposing the Si(1,1,1) plane; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the exposed Si(1,1,1) plane in sequence via epitaxial growth.

10. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

11. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP).

12. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$; and

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop.

13. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes generally conforming the N-type GaN, InGaN, and P-type GaN materials to the Si(1,1,1) plane.

14. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, the N-type GaN, InGaN, and P-type GaN materials individually forming a zigzag pattern.

15. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes coalescing at least one of the N-type GaN material, the InGaN material, and a P-type GaN material to the Si(1,1,1) plane.

16. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, at least one of the N-type GaN, InGaN, and P-type GaN materials having a generally planar surface.

17. A light emitting diode, comprising:

an N-type gallium nitride (GaN) material;

a P-type GaN material spaced apart from the N-type GaN material; and

an indium gallium nitride (InGaN) material directly between the N-type GaN material and the P-type GaN material;

wherein at least one of the N-type GaN, InGaN, and P-type GaN materials has a non-planar surface.

18. The light emitting diode of claim 17 wherein non-planar surface has a zigzag pattern.

19. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane and a second plane joined together at a junction.

20. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane and a second plane joined together at a junction, the first and second planes forming an angle of about 72°.

21. The light emitting diode of claim 17 wherein non-planar surface has a plurality of indentations formed by a first plane, a second plane, and a third plane extending between the first and second planes, the first and second planes forming an angle of about 54° and 126° with the third plane, respectively.

22. The light emitting diode of claim 17 wherein the N-type GaN, InGaN, and P-type GaN materials individually have a surface with a zigzag pattern.

23. The light emitting diode of claim 17 wherein at least one of the N-type GaN, InGaN, and P-type GaN materials have a first surface and a second surface opposite the first surface, the first surface being non-planar and the second surface being generally planar.

24. The light emitting diode of claim 17 wherein at least one of the N-type GaN, InGaN, and P-type GaN materials have a first surface and a second surface opposite the first surface, the first surface having a zigzag pattern and the second surface being generally planar.

CLAIMS

We claim:

1. A method for processing a silicon substrate, comprising:

applying an anisotropic etchant to a surface of the silicon substrate, the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

forming an indentation on the surface of the silicon substrate with the applied anisotropic etchant, the indentation being defined by at least one plane with a Si(1,1,1) lattice orientation; and

forming a light emitting diode structure on the at least one plane with the Si(1,1,1) lattice orientation of the indentation, wherein forming the light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence and coalescing at least one of the N-type GaN, InGaN, and P-type GaN materials during deposition, and wherein the coalescing reduces a dislocation density in at least one of the N-type GaN, InGaN, and P-type GaN materials.

2. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is greater than about 100 microns; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic chemical vapor deposition (MOCVD), the N-type GaN, InGaN, and P-type GaN materials having surfaces generally conforming to the zigzag pattern of the first and second Si(1,1,1) planes.

3. The method of claim 1 wherein

the method further includes:

depositing a mask material on the surface of the silicon substrate; and

patterning the mask material to form a plurality of openings to the surface of the silicon substrate;

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate via the openings;

forming an indentation includes forming a plurality of indentations individually having a first Si(1,1,1) plane and a second Si(1,1,1) plane both extending toward the silicon substrate from the surface to a depth, the first and second Si(1,1,1) planes forming a zigzag pattern;

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a value of the depth that is less than about 1 micron; and

forming a light emitting diode structure includes:

depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence via metal organic chemical vapor deposition (MOCVD); and

coalescing at least one of the N-type GaN, InGaN, and P-type GaN materials during the MOCVD operation.

4. The method of claim 1 wherein

applying an anisotropic etchant includes applying a solution containing at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP) to the surface of the silicon substrate; and

forming a light emitting diode structure includes depositing an N-type gallium nitride (GaN) material, an indium gallium nitride (InGaN) material, and a P-type GaN material on the first and second Si(1,1,1) planes in sequence.

5. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane, a second Si(1,1,1) plane, and a Si(1,0,0) plane extending between the first and second Si(1,1,1) planes.

6. The method of claim 1 wherein forming an indentation includes forming an indentation having a first Si(1,1,1) plane and a second Si(1,1,1) plane intercepting the first Si(1,1,1) plane at a junction.

7. The method of claim 1 wherein forming a light emitting diode structure includes depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the at least one plane of the indentation in sequence, the plane having the Si(1,1,1) lattice orientation.

8. The method of claim 1 wherein:

forming an indentation includes forming an indentation extending toward the silicon substrate from the surface to a depth; and

the method further includes adjusting at least one of a concentration of the anisotropic etchant, an etching temperature, and an etching period to achieve a desired value of the depth.

9. A method for processing a silicon substrate, comprising:

reacting a surface of a silicon substrate with an anisotropic etchant, at least a portion of the silicon substrate having a Si(1,0,0) lattice orientation at the surface;

removing silicon material from the surface of the silicon substrate along a Si(1,0,0) plane faster than along a Si(1,1,1) plane, thereby exposing the Si(1,1,1) plane; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material on the exposed Si(1,1,1) plane in sequence via epitaxial growth and coalescing at least one of the N-type GaN, InGaN, and P-type GaN materials during deposition, wherein the coalescing reduces a dislocation density in at least one of the N-type GaN, InGaN, and P-type GaN materials.

10. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

11. The method of claim 9 wherein reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with at least one of tetra-methyl-ammonium hydroxide (TMAH), potassium hydroxide (KOH), ammonium hydroxide (NH_4OH), and ethylenediamine pyrocatechol (EDP).

12. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$; and

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop.

13. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes generally conforming the N-type GaN, InGaN, and P-type GaN materials to the Si(1,1,1) plane.

14. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, the N-type GaN, InGaN, and P-type GaN materials individually forming a zigzag pattern.

15. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes coalescing at least one of the N-type GaN material, the InGaN material, and a P-type GaN material to the Si(1,1,1) plane.

16. The method of claim 9 wherein

reacting a surface of a silicon substrate with an anisotropic etchant includes reacting the surface of the silicon substrate with the anisotropic etchant as follows:

$$Si + 4(OH^-) \rightarrow Si(OH)_4 + 4e^-$$

removing silicon material includes preferentially removing the silicon material along the Si(1,0,0) plane while using the Si(1,1,1) plane as an etch stop; and

depositing an N-type GaN material, an InGaN material, and a P-type GaN material includes depositing the N-type GaN, InGaN, and P-type GaN materials on the exposed Si(1,1,1) plane, at least one of the N-type GaN, InGaN, and P-type GaN materials having a generally planar surface.