

What is claimed is:

1. A semiconductor device comprising:
 - a substrate comprising a lower wire;
 - an etch stop layer on the substrate, the etch stop layer contacts the substrate;
 - an interlayer insulating layer on the etch stop layer;
 - an upper wire disposed in the interlayer insulating layer and separated from the lower wire; and
 - a via formed in the interlayer insulating layer and the etch stop layer and connecting the lower wire with the upper wire,
 - wherein the via comprises a first portion in the etch stop layer and a second portion in the interlayer insulating layer, and
 - wherein a sidewall of the first portion of the via comprises a step configuration.
2. The semiconductor device of claim 1, wherein the sidewall of the first portion of the via comprises first and second sidewalls extending away from the substrate, and a third sidewall connecting the first sidewall with the second sidewall.
3. The semiconductor device of claim 2, wherein the first sidewall is closer to an upper surface of the substrate than the second sidewall is,
 - wherein the first portion of the via comprises a third portion corresponds to the first sidewall, and a fourth portion corresponds to the second sidewall, and
 - wherein a width of the third portion of the via is smaller than a width of the fourth portion of the via.
4. The semiconductor device of claim 3, wherein the etch stop layer comprises first to third etch stop patterns stacked on one another sequentially,
 - wherein the first etch stop pattern surrounds the third portion of the via, and
 - wherein the second and third etch stop patterns surround the fourth portion of the via.

5. The semiconductor device of claim 2, wherein the etch stop layer comprises first to third etch stop patterns stacked on one another sequentially, and

wherein the third sidewall comes in contact with a part of an upper surface of the first etch stop pattern.

6. The semiconductor device of claim 2, wherein the etch stop layer comprises first to third etch stop patterns stacked on one another sequentially, and

wherein the third sidewall comes in contact with a part of an upper surface of the second etch stop pattern.

7. The semiconductor device of claim 1, wherein the etch stop layer comprises a lower etch stop pattern and an upper etch stop pattern stacked on the substrate sequentially,

wherein the first portion of the via comprises a third portion in the lower etch stop pattern and a fourth portion in the upper etch stop pattern, and

wherein a width of the third portion is smaller than a width of the fourth portion at a boundary between the lower etch stop pattern and the upper etch stop pattern.

8. The semiconductor device of claim 7, wherein the lower etch stop pattern comprises a first etch stop pattern on the substrate, and

wherein the upper etch stop pattern comprises second and third etch stop patterns stacked on the first etch stop pattern sequentially.

9. The semiconductor device of claim 7, wherein the lower etch stop pattern comprises first and second etch stop patterns stacked on the substrate sequentially, and

wherein the upper etch stop pattern comprises a third etch stop pattern stacked on the second etch stop pattern.

10. The semiconductor device of claim 1, wherein the etch stop layer comprises first to third etch stop patterns stacked on one another sequentially,

wherein the first etch stop pattern and the third etch stop pattern comprises a same material, and

wherein the second etch stop pattern comprises a different material from the material of the first and third etch stop patterns.

11. A semiconductor device comprising:

a substrate comprising a lower wire;

an etch stop layer comprising first to third etch stop patterns stacked on the substrate sequentially;

an interlayer insulating layer disposed on the third etch stop pattern;

an upper wire disposed in the interlayer insulating layer and separated from the lower wire; and

a via formed in the interlayer insulating layer and the etch stop layer and connecting the lower wire with the upper wire,

wherein the first etch stop pattern and the third etch stop pattern comprises a same material,

wherein the second etch stop pattern comprises a different material from the material of the first and third etch stop patterns, and

wherein a lower surface of the first etch stop pattern contacts the substrate, a part of an upper surface of the first etch stop pattern contacts the via.

12. The semiconductor device of claim 11, wherein the first etch stop pattern and the third etch stop pattern contain a same metal element, and

wherein the second etch stop pattern does not contain the metal element contained in the first and third etch stop patterns.

13. The semiconductor device of claim 11, wherein the first and third etch stop patterns contain aluminum element, and

wherein the second etch stop pattern does not contain the aluminum element.

14. The semiconductor device of claim 11, wherein the via comprises a first portion in the etch stop layer, and a second portion in the interlayer insulating layer, and wherein a sidewall of the first portion of the via comprises stepwise.

15. The semiconductor device of claim 11, wherein the via comprises a first portion in the etch stop layer, and a second portion in the interlayer insulating layer, wherein the first portion of the via comprises a third portion having a first width and a fourth portion having a second width larger than the first width at a boundary between the first etch stop pattern and the second etch stop pattern, and wherein the fourth portion is disposed on the third portion.

16. A semiconductor device comprising:
a substrate comprising a lower wire;
an etch stop layer comprising a lower etch stop pattern and an upper etch stop pattern stacked on the substrate sequentially, the lower etch stop pattern contacts the substrate;
an interlayer insulating layer disposed on the upper etch stop pattern;
an upper wire disposed in the interlayer insulating layer and comprising a longer side extended in a first direction; and
a via formed in the interlayer insulating layer and in the etch stop layer and connecting the lower wire with the upper wire,
wherein a first width of the via in the lower etch stop pattern in the first direction is smaller than a second width of the via in the upper etch stop pattern in the first direction at a boundary between the lower etch stop pattern and the upper etch stop pattern.

17. The semiconductor device of claim 16, wherein, at the boundary between the lower etch stop pattern and the upper etch stop pattern, a width of the via in the upper etch stop pattern in a second direction intersecting with the first direction is greater than a width of the via in the lower etch stop pattern in the second direction.

18. The semiconductor device of claim 16, wherein, at the boundary between the lower etch stop pattern and the upper etch stop pattern, a width of the via in the upper etch stop pattern in a second direction intersecting with the first direction is equal to a width of the via in the lower etch stop pattern in the second direction.

19. The semiconductor device of claim 16, wherein the lower etch stop pattern comprises a first etch stop pattern on the substrate, and

wherein the upper etch stop pattern comprises second and third etch stop patterns stacked on the first etch stop pattern sequentially.

20. The semiconductor device of claim 16, wherein the lower etch stop pattern comprises first and second etch stop patterns stacked on the substrate sequentially, and

wherein the upper etch stop pattern comprises a third etch stop pattern stacked on the second etch stop pattern.