shaped structure to increase bearing capacity as described above with reference to FIGs. 5A and 5B. The first supports 111 may have the same arrangement as the supports shown in FIG. 5A, or the same arrangement as the supports shown in FIG. 5B.

[00100] FIGs. 8A and 8B are a plan view and a cross-sectional diagram, respectively, which illustrate a forming process of slits 121 and first openings 123 and a forming process of second openings 125. FIG. 8A illustrates a plan view of one layer of the interlayer insulating layers 101 and FIG. 8B illustrates a cross section of a stack structure taken along line A-A' of FIG. 8A.

[00101] Referring to FIGs. 8A and 8B, the slits 121 and the first openings 123, which pass through the preliminary stack structure PST, shown in FIG. 7B, may be simultaneously formed. The first supports 111 of FIG. 7A may be disposed between the slits 121, adjacent to each other. The first openings 123 may open side portions of the first supports 111 of FIG. 7A. Each of the first openings 123 may overlap some of the first supports 111. The first supports 111, overlapped with the first openings 123, may be partially etched. Each of the first supports 111P, remaining without being removed by the forming process of the first openings 123, may be defined as the first portion SP1 of the support described above with reference to FIGs. 5A, 5B,

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

interlayer insulating layers stacked to be spaced apart from each other;

a support passing through the interlayer insulating layers;

at least one opening interposed between a sidewall of the support and each of the interlayer insulating layers to expose the sidewall of the support; and

electrode patterns filling spaces between the interlayer insulating layers,

wherein the at least one opening extends between the sidewall of the support and the each of the electrode patterns.

2. The semiconductor device of claim 1, further comprising a plurality of slits passing through the interlayer insulating layer,

wherein the at least one opening is formed along the sidewall of the support which faces at least one of the slits.

3. The semiconductor device of claim 2, wherein each of the electrode patterns comprises:

a first conductive pattern penetrated by the support;

a second conductive patterns disposed adjacent to each of

the slits and extending along a side portion of the first conductive pattern which faces each of the slits; and

a third conductive pattern disposed adjacent to one of the at least one opening.

4. The semiconductor device of claim 3, wherein the first conductive pattern includes a first conductive material, and

wherein each of the second and third conductive patterns includes a second conductive material having a lower resistance than the first conductive material.

5. The semiconductor device of claim 3, wherein the first conductive pattern extends between the second conductive pattern and the third conductive pattern.

6. The semiconductor device of claim 3, wherein the second conductive pattern is coupled to the third conductive pattern.

7. The semiconductor device of claim 3, wherein the support includes protrusions protruding towards the slits to form a T-shape, and

wherein the third conductive pattern extends along a sidewall of at least one of the protrusions.

8. The semiconductor device of claim 1, further comprising channel structures passing through the interlayer insulating layers and the electrode patterns.

9. A method of manufacturing a semiconductor device, the method comprising:

forming a stack structure including interlayer insulating layers and sacrificial layers, which surround a support and are alternately stacked on each other;

forming a plurality of slits which pass through the stack structure, wherein the support is disposed between the slits;

forming a first opening which passes through the stack structure, wherein the first opening opens a side portion of the support, wherein the first opening is interposed between the side portion of the support and each of the interlayer insulating layers;

forming second openings by removing the sacrificial layers through the slits and the first opening; and

forming an electrode pattern in each of the second openings through the slits and the first opening, wherein the first opening extends between the side portion of the support and the electrode pattern.

10. The method of claim 9, wherein the forming of the electrode pattern comprises:

forming a first conductive material filling each of the second openings through the slits and the first opening;

forming a first conductive pattern by partially etching the first conductive material through the slits and the first opening, wherein the first conductive pattern is exposed by a corresponding one of portions of the second openings, the portions of the second openings adjacent to the slits and the first opening;

filling the portions of the second openings with a second conductive material through the slits and the first opening; and

forming a second conductive pattern adjacent to each of the slits, and a third conductive pattern adjacent to the first opening by etching the second conductive material.

11. The method of claim 10, wherein the second conductive material has a lower resistance than the first conductive material.

12. The method of claim 10, wherein the first conductive material includes a titanium nitride layer, and

wherein the second conductive material includes tungsten.

13. The method of claim 10, wherein the second conductive pattern and the third conductive pattern are coupled to each other.

14. The method of claim 10, wherein the second conductive pattern and the third conductive pattern are separated from each other by the first conductive pattern.