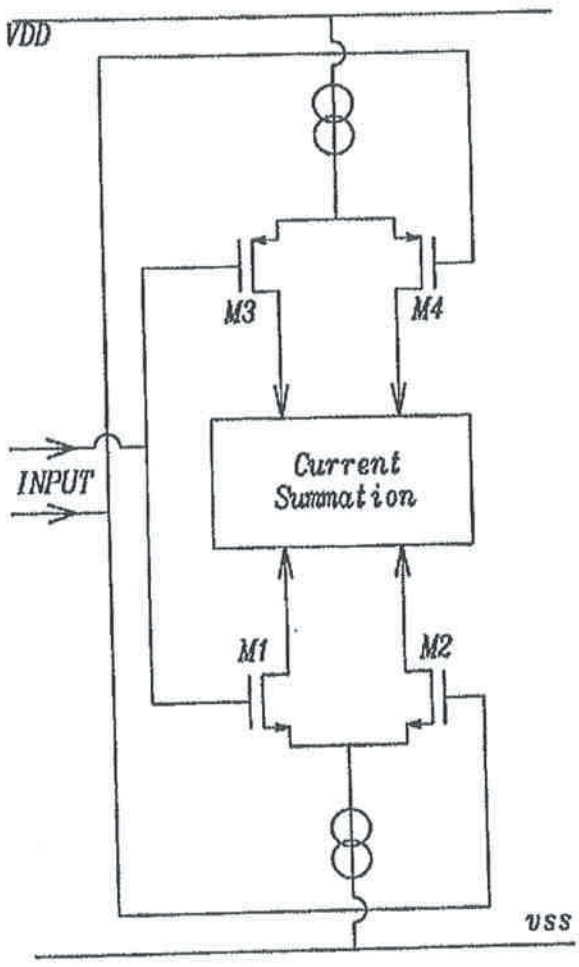


FIG. 1 – Prior Art

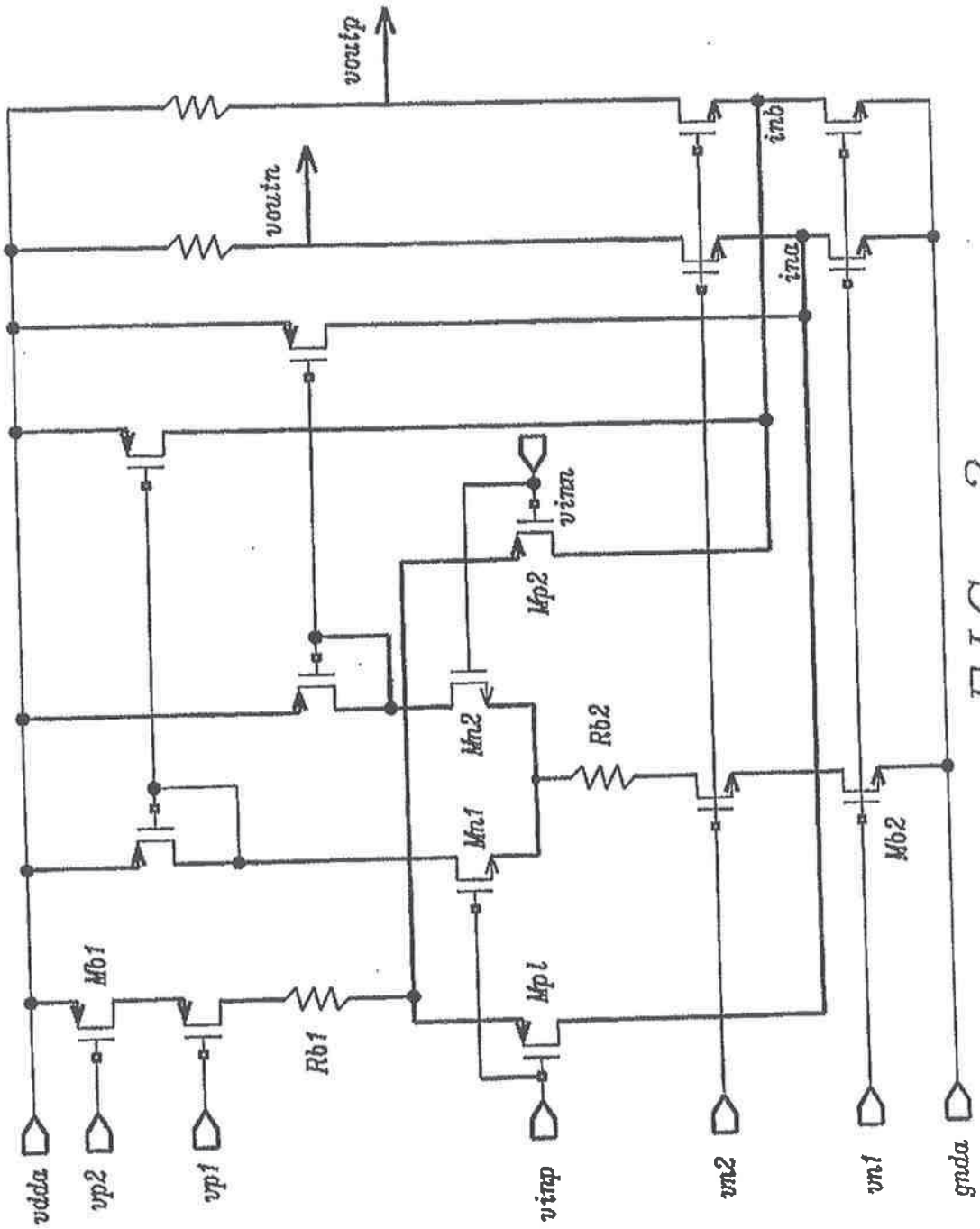
voutp
vouin
inb
ina
vinn
Mp2
Mn2
Rb2
Mn1
Mb2
Mb1
Mp1
Rb1
vdda
vp2
vp1
vinp
vm2
vm1
gnda

FIG. 2

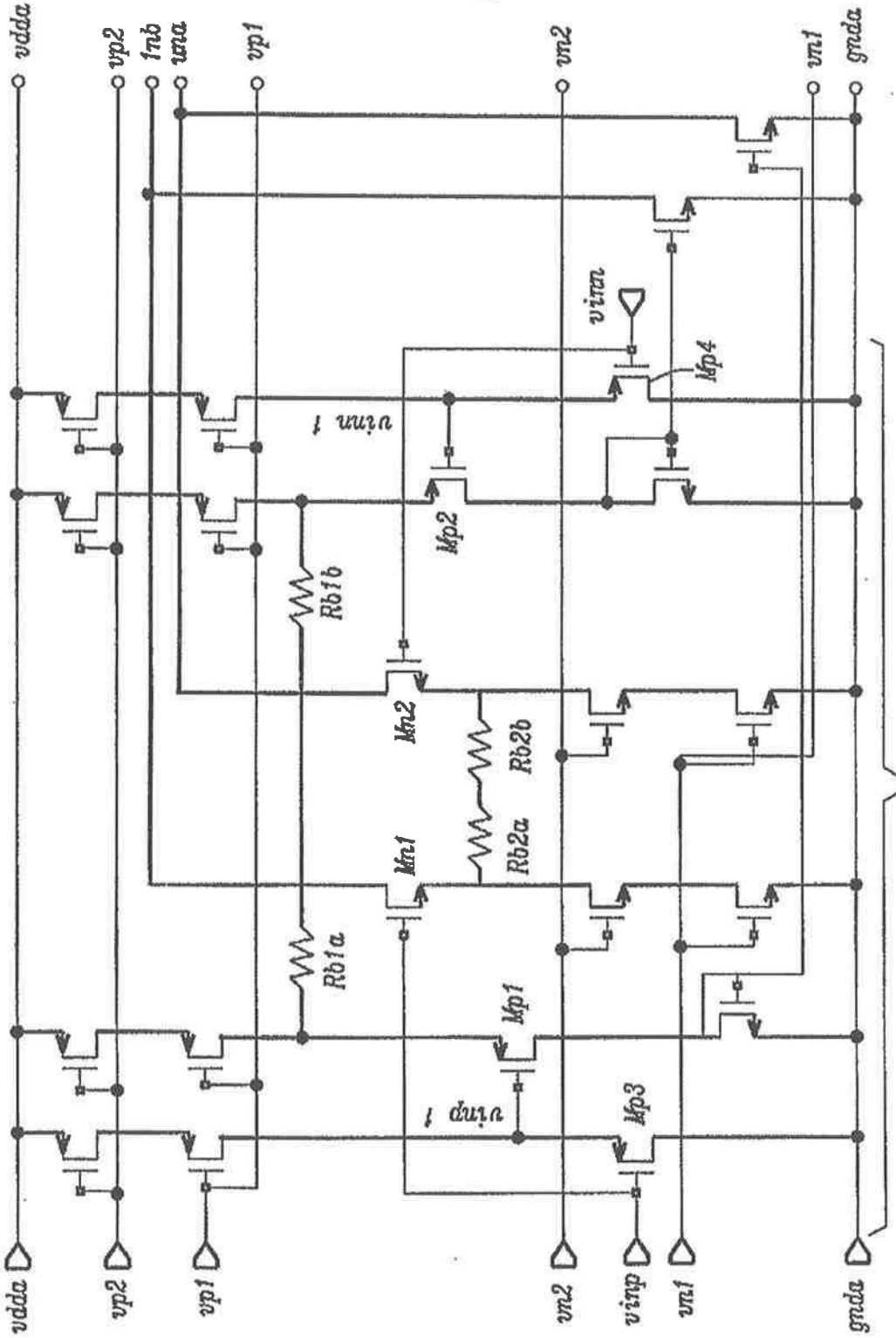
vdda
vp2
vnb
vna
vp1
vm2
vm1
gnda
vinn
Mp4
vinn
Mp2
Rb1b
Mn2
Rb2b
Rb2a
Mn1
Rb1a
Mp1
vinp
Mp3
differential amplifier
vdda
vp2
vp1
vm2
vinp
vm1
gnda

FIG. 3a

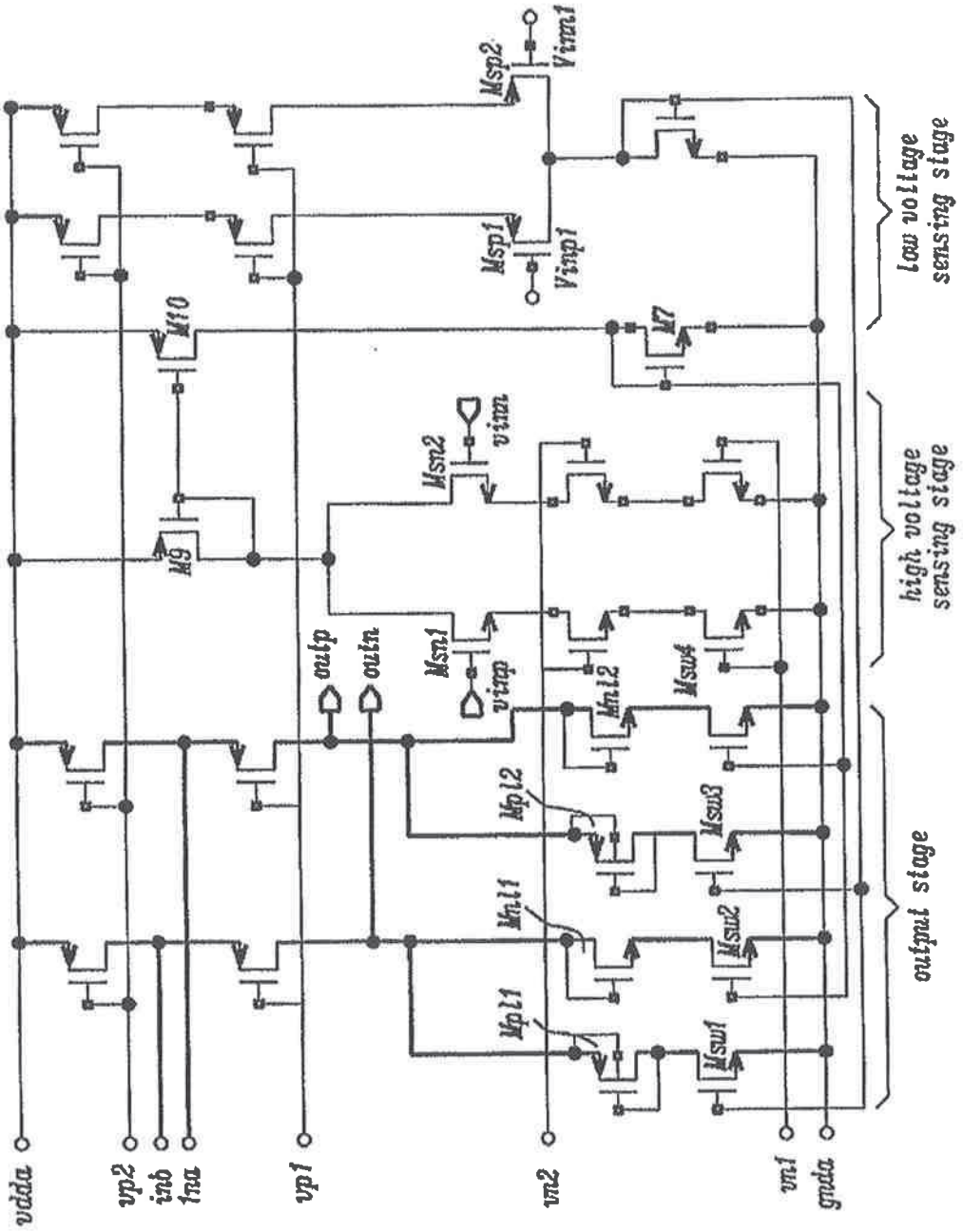
vdda
vp2
inb
1na
vp1
vn2
vn1
gnda
Mpl1
Mnl1
Mpl2
Mnl2
Msw1
Msw2
Msw3
Msw4
Msn1
Msn2
Msp1
Msp2
Vinp1
Vinn1
vinp
vinn
outp
outn
M9
M10
M7
output stage
high voltage sensing stage
low voltage sensing stage

FIG. 3b

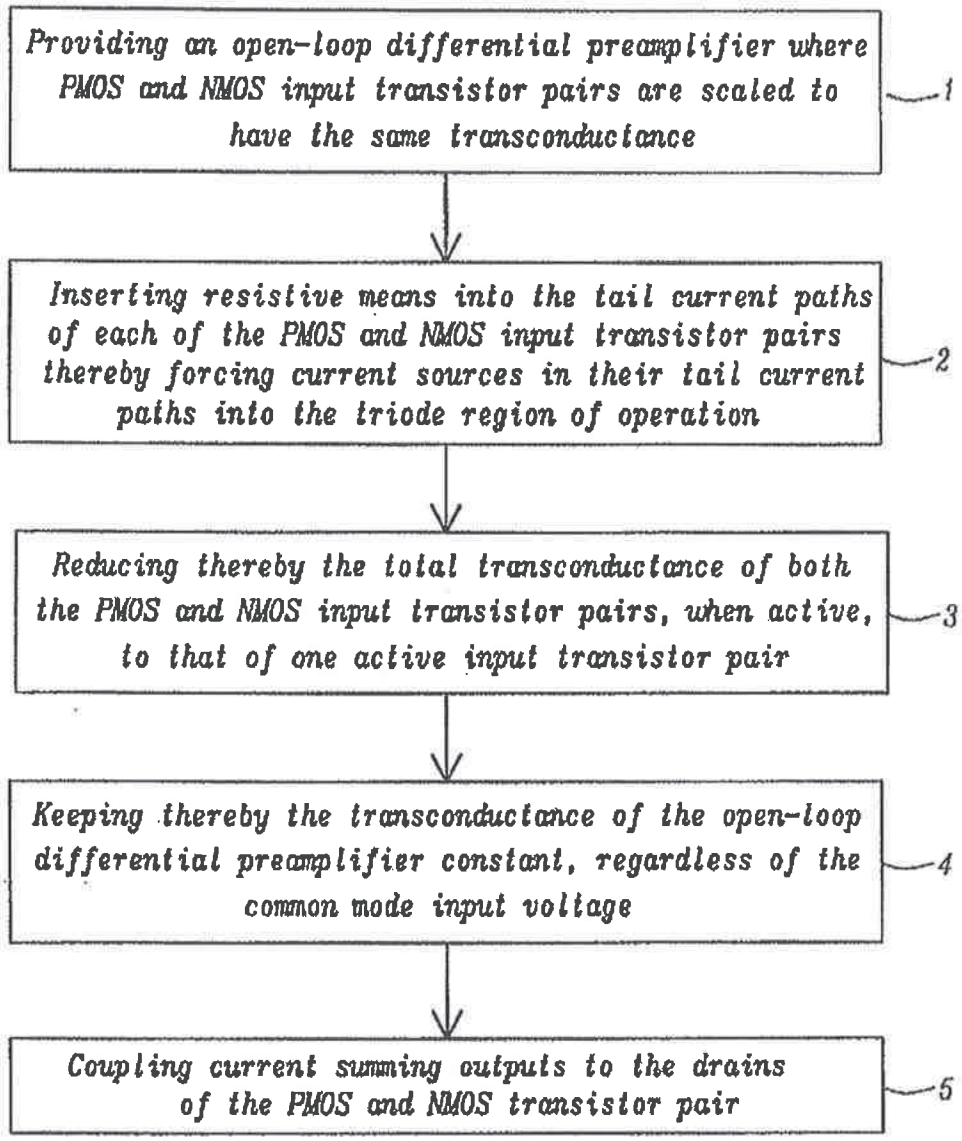
Providing an open-loop differential preamplifier where PMOS and NMOS input transistor pairs are scaled to have the same transconductance
1
Inserting resistive means into the tail current paths of each of the PMOS and NMOS input transistor pairs thereby forcing current sources in their tail current paths into the triode region of operation
2
Reducing thereby the total transconductance of both the PMOS and NMOS input transistor pairs, when active, to that of one active input transistor pair
3
Keeping thereby the transconductance of the open-loop differential preamplifier constant, regardless of the common mode input voltage
4
Coupling current summing outputs to the drains of the PMOS and NMOS transistor pair
5

FIG. 4

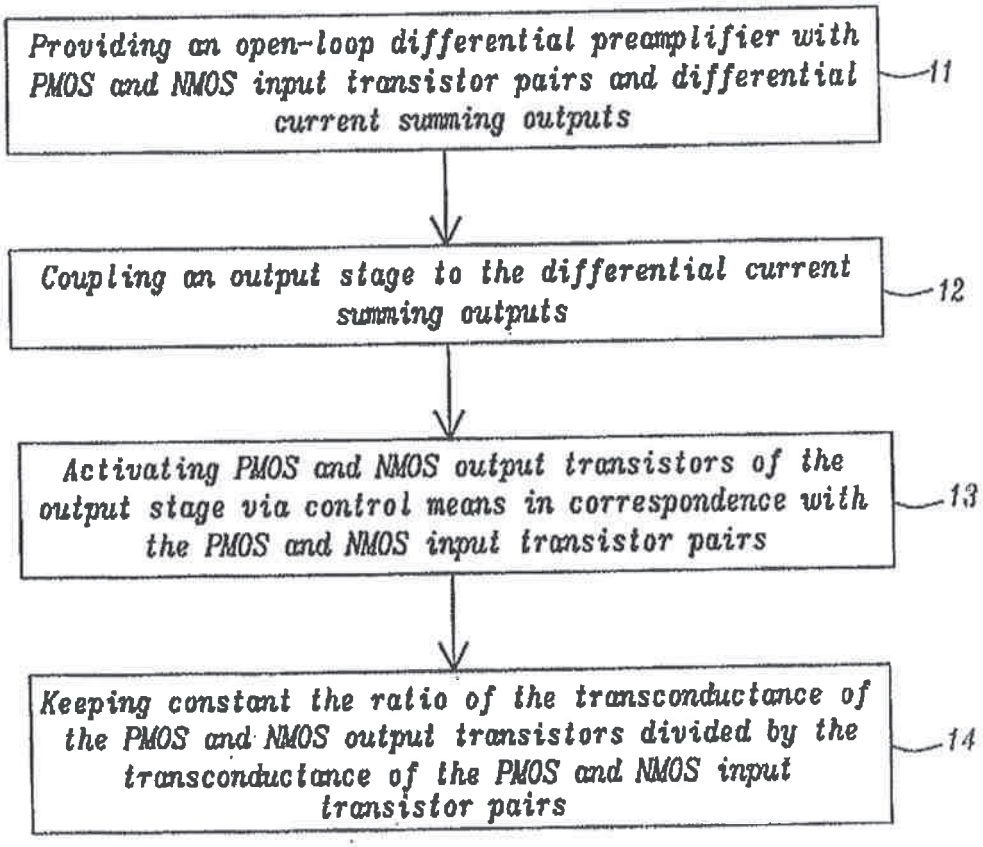
Providing an open-loop differential preamplifier with PMOS and NMOS input transistor pairs and differential current summing outputs
11
Coupling an output stage to the differential current summing outputs
12
Activating PMOS and NMOS output transistors of the output stage via control means in correspondence with the PMOS and NMOS input transistor pairs
13
Keeping constant the ratio of the transconductance of the PMOS and NMOS output transistors divided by the transconductance of the PMOS and NMOS input transistor pairs
14

FIG. 5