

A METHOD OF DRIVING AN ACTIVE MATRIX PANEL OF
A LIQUID CRYSTAL DISPLAY DEVICE

This invention relates to a method of driving an active matrix panel of a liquid crystal display device, utilising thin film transistors.

Liquid crystal displays have been used for small displays for instance in a timepiece, but it is now desired to use a liquid
5 crystal display for a large display device such as a computer terminal or a pocket TV where the liquid crystal display needs to have a large capacity. In a conventional generalised AC amplitude selected multiplexing driving method, the limit of driving duty is $1/30 - 1/50$ and it is difficult to realise a large capacity
10 driving duty of, for instance, $1/500$. In order to improve the driving duty, it has been suggested to use a transistor such as a thin film transistor (TFT) or an active element such as a metal-insulator-metal (MIM) element (strictly speaking, MIM is not active but in this specification it is defined to be an active element)
15 for writing and holding data in every picture element of the display device.

According to the present invention there is provided a circuit for driving an active matrix panel of a liquid crystal display device in which a video signal suitable for a cathode ray tube is used
20 to write into an element of the device via a transistor which during a selected period is turned ON by a gate line, the polarity of the level of the video signal being inverted alternately every field

and written into the element from a data line, and the level of the video signal in the element is held during a non-selected period during which the transistor is turned OFF, the transistor being constructed as a thin film transistor and the voltage applied to the gate of the transistor during the non-selected period being biased from zero level and set within the range of the voltage level of the power source for driving the video signal.

Advantageously, the level of the video signal is non-symmetrical about a common electric potential.

Preferably, the gate voltage applied to the gate of the transistor during the non-selected period is different during alternate positive and negative fields.

This invention will now be illustrated, merely by way of example, with reference to the accompanying drawings, in which:-

Figure 1 shows an $n \times m$ matrix of a liquid crystal display device;

Figure 2 shows the structure of part of a matrix such as that shown in Figure 1;

Figure 3 shows waveforms of signals applied to a matrix such as that shown in Figures 1 and 2 in a preferred method according to the present invention;

Figure 4 shows voltage-current characteristics of two types of transistors;

Figure 5 shows waveforms of a video signal and of gate signals which may be used in the preferred method;

Figure 6 shows further voltage-current characteristics of a transistor of the type used in the preferred method;

Figure 7 is a block diagram of a circuit which may be operated in accordance with the preferred method;

5 Figures 8 and 9 are graphs showing effects of using the preferred method;

Figure 10 shows a waveform of a video signal used in a further preferred method according to the present invention; and

10 Figure 11 shows waveforms used in a yet further preferred embodiment according to the present invention.

Figure 1 shows an active matrix in which picture elements are arranged in an $n \times m$ matrix. Picture elements in a cell are selected by selecting signals on m gate lines G_1 to G_m and data signals are then written into the selected picture elements via
15 n data lines D_1 to D_n and held there.

Figure 2 shows the structure of part of an active matrix using TFT receiving data from a data line D_i . m picture elements P_{i1} - P_{im} are arranged in a column connected to the data line D_i as shown in Figure 2. A transistor Tr of a picture element is turned
20 ON by a selecting signal on a corresponding gate line and display data on a data line is then written into a picture element via the transistor Tr . After writing data, the transistor Tr is turned OFF again and the written data is held until the next time the transistor is selected. Each picture element includes a liquid
25 crystal display device which is represented by a resistance R_L and a capacitance C_L connected to the transistor Tr . The data line D_i

is connected to a data driver 3. In the data driver 3, a video signal VS is sampled by a transistor 2 in synchronism with a selecting signal Si produced by a shift register 1 and held in a capacitor Csi on the data line Di. This driving method is known
5 as a point-at-a-time method.

Figure 3 shows waveforms applied to picture elements in a point-at-a-time driving method in a preferred embodiment of the invention. According to Figure 3(a), one frame is divided into two fields where a negative video signal VS1 in an odd number field and a positive video signal VS2 in an even number field are applied
10 to a data line Di. Video signals VS vary according to the level of the grey scale of the image to be formed and are inverted alternately in the two fields about a level VCOM within the range of GND to VDD. Figures 3(b) and (c) show scanning signals of data
15 lines G1 and Gm which are applied to the gate of a transistor Tr. In the case of an N type TFT, +VDG is applied to the gate when selecting a picture element Pil-Pim and GND when the picture element is not selected. Accordingly, the voltage between the gate and source of the transistor during an odd field term is relatively
20 low compared with that during an even field term since a negative video signal is applied to the source of the transistor in the odd field. Figure ³4(d) shows a waveform Vc which is applied to a picture element in each field. This voltage is written into the picture element and kept therein during a non-selected period. Waveform Vc1
25 is written into a cell Pil and waveform Vcm into a cell Pim as shown

in Figure 2.

Figure 4 shows V-I characteristics of two types of transistors (drain current I_D to gate-source voltage V_{GS}). The characteristic curve B indicates a conventional transistor composed of a silicon monocrystal substrate. The curve T shows a thin film transistor composed of a polycrystalline or amorphous thin film.

Curve B has a favourable characteristic as the drain current I_D rises steeply with an increase in the gate-source voltage V_{GS} in the positive region, and the leak current I_D is extremely small and constant in the zero or negative region. However, if a conventional transistor is used for an active matrix display, it is disadvantageous as the liquid crystal materials used must be of the guest-host type or dynamic scattering type since a monocrystalline silicon substrate is opaque. If a twisted nematic type liquid crystal is used, then a transparent substrate is required in order to produce the highest quality display. A thin film transistor may be provided on a glass substrate or an SiO_2 quartz substrate and transistors using a silicon thin film such as polycrystal-silicon or amorphous silicon have been developed. However, the TFT has a disadvantageous characteristic curve T as shown in Figure 4. As this Figure shows, the drain current increases only gradually in the positive region and leakage current varies in dependence upon the negative bias voltage V_{GS} and is relatively large even at the minimum point in the negative region. Therefore, the use of this type of transistor for driving liquid crystal devices in the manner shown in Figure 3 has the following

disadvantages:

(1) During a non-selected period, electric charge in each picture element leaks away to a data line via the transistor, or charge on a data line flows into the picture element since the leakage level is relatively large in the OFF state of the transistor. Thus, the quality of contrast in the display is deteriorated.

(2) The range R shown in Figure 4 is the operating range of the transistor during a non-selected period. The leakage current in the even field, is, of course, relatively large compared with that in the odd field since the maximum amplitude of the video signal in the even field approaches VDD. Furthermore, in the final scanning line of the even field, leakage current accumulates where the polarity of the video signal of the data line is inverted in the next field, since the potential difference between the picture element and the data line reaches a maximum value and the voltage between the source and the drain is also at a maximum. In Figure 4, TA, TB and TC show variations in characteristic curve T in dependence on the different values of the voltage between the source and drain (TA, TB and TC corresponding to voltage differences of 2V, 4V and 8V, respectively). The effective voltage applied to the picture element in the lower end portion decreases and this causes the display to be non-uniform.

(3) A gate voltage VG has to be relatively large in order to obtain the same level of drain current compared with that of a monocrystal substrate transistor. This means that VDG has to be larger and sometimes exceed the break-down voltage of the driver integrated

circuit or increases the power consumption.

This embodiment seeks to eliminate the above disadvantages and produce a high quality display.

This embodiment provides means for biasing the voltage level
5 of the gate to some degree during the non-selected periods within the voltage range of a power source of the data line driver integrated circuit. In prior art arrangements, the potential level during non-selected periods is set to be the zero level (GND level) of the data line driver integrated circuit thereof.

10 Figure 5 shows the waveform of a video signal (a) and of a gate signal, where waveform (b) is that used in the prior art, and (c), (d), or (e) may be used in the preferred embodiment of this invention.

Video signal (a) is set to be a waveform symmetrical about
15 a common level VCOM in each field. The source voltage of the driver circuit of the data lines is set to be within the range GND to VDD. The level of onset voltage applied to a gate line during a non-selected period is set to be around VCOM as shown in Figure 5(c). As a result, the operating range R of the transistor during a non-
20 selected period is shifted to the range R'1 which is centred around the zero level, as shown in Figure 6. This bias shift contributes towards a decrease in leakage current. Furthermore, the dependency of leakage current on source drain voltage described before can be avoided by biasing the non-selected level of the gate voltage.
25 By this means, the accumulation of leakage current at the final

line of the even field and deterioration in image contrast from the upper portion to the lower portion of a field can be avoided. Thus, an image of uniform quality over an entire field can be obtained. Also, the amplitude of the gate voltage is $V_{DG} - V_{COM}$ which is lower by the amount V_{COM} than that used in the prior art, but produces the same level of ON current.

As shown in Figure 6(c), (d), and (e), there are differences between V-I characteristics, particularly in relation to minimum points of drain current, due to variations in conditions during the manufacturing process by which the transistors are made. R'1 is the operating range of a transistor having the characteristic curve c'. R'2 is the operating range of a transistor having the characteristic curve e'. R'3 is the operating range of a transistor having a characteristic curve of d'. Thus, there is a need for compensation to reduce these differences. If, for example, the non-selected level of gate voltage is biased by +VGB (or -VGB) about V_{COM} as shown in Figure 5(d) or (e), the minimum point of the drain current is located in the positive region (or negative region for -VGB) as shown by characteristics d' and e'. This biasing can contribute further to the decrease of leakage current.

Figure 7 shows a block diagram of a driving circuit for driving an active matrix in the manner described above. In Figure 7, a driver 111 for data lines and a driver 112 for gate lines are connected to a panel 113 comprising an $n \times m$ matrix substrate. In the above construction, the driver 111 has a driving output of

VD1 - VDN, and the driver 112 has a driving output of VG1 - VGM.
A power circuit 110 generates a power voltage, VDD and GND being
applied to a sample and hold circuit of driver 111 for data lines
and to a shift register. The amplitude of video signals VS is within
5 the range of VDD - GND. The power circuit 110 also generates voltage
levels for the gate lines, VCOM being the non-selected level and
VDG the selected level. VCOM is also the potential of the common
electrode on the opposite side of the active matrix panel.

Figure 8 is a graph demonstrating the effects of using the
10 driving method described above. In Figure 8, the average root-
mean-square value VCR of every picture element is plotted against
the bias value VGB for a video signal of specified level applied
to one picture element and stored there for 16msec. The root-mean-
square value VCR is taken relative to a minimum at the time when
15 VGB is equal to zero as in a conventional method. In the described
driving method, VGB is set to be around the value of VCOM and this
corresponds to a maximum of the root-mean-square value VCR as shown
in Figure 8 and produces an image display of high quality.

In Figure 9, VGM is the value of gate-source voltage VGS which
20 produces the minimum value of current having TFT characteristics.
Figure 9 shows the range of non-selected levels of VGB against VGM.
VGB is the value which minimises the decrease in the root-mean-
square value VCR so providing good contrast in the liquid crystal
display. As shown in Figure 9, it is necessary to adjust the non-
25 selected level of VGB in accordance with VGM depending on TFT
characteristics.

Figure 10 shows a waveform of a video signal which may be used in another embodiment of a driving method according to this invention. In this case, the characteristic T of TFT is non-symmetrical with respect of VGS, so the voltage level for driving a data line is set to be non-symmetrical with respect to V'COM. This arrangement can be considered in two ways. One is that a level is set so that only the amplitude or the bias of the video signal VS is non-symmetrical with respect to V'COM in each field by controlling the gain of the amplifier or controlling the TC output level of the amplifier. The other is that the level is set so that the power source electrical potentials are non-symmetrical with respect to VCOM.

It is more suitable that the data line is set to be non-symmetrical in accordance with the characteristics of the TFT. It is also possible for the non-selected level of the gate to be set to be biased by $\pm V_{GB}$ with respect to V'COM.

Figure 11 shows a signal wave which is used in a yet further embodiment of a method according to the present invention. In this embodiment, the non-selected level of the gate voltage is changed every field as the polarity of the video signal is inverted. This can reduce the range of variation of VGS (gate-source voltage) according to the variation of level of the video signal by approximately one-half. As a result, a root-mean-square value of a picture element is more suitable. In this embodiment, a non-selected level of the gate voltage is VCOM in an odd field and +VDS in an even field.

The method described above produces the following effects and thereby enables a liquid crystal television having a high quality display to be produced.

5 (1) As the most suitable root-mean-square value of a picture element is provided, a display corresponding to the original video signal can be obtained. Therefore, the most suitable display contrast can be offered.

10 (2) The decrease in the root-mean-square value of a picture element in the side of the last scanning line, accompanied with an increase in the OFF current with a negative bias between gate and source can be prevented. Accordingly, a uniform voltage can be written into the picture element in any scanning line and a uniform root-mean-square value of the picture elements can be obtained in any scanning line thereby eliminating unevenness in the display.

15 (3) As the amplitude of the gate line voltage can be reduced, the driver integrated circuit can be designed more easily and power consumption may be reduced.

The method of driving an active matrix panel of a liquid crystal display device described herein also forms the subject matter of
20 British Patent Application No. 8308763 (Serial No. 2121584).



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CLAIMS

1. A method of driving an active matrix panel of a liquid crystal display device in which a video signal suitable for a cathode ray tube is used to write into an element of the device via a transistor which during a selected period is turned ON by a gate
5 line, the polarity of the level of the video signal being inverted alternately every field and written into the element from a data line, and the level of video signal in the element is held during a non-selected period during which the transistor is turned OFF, the transistor being constructed as a thin film transistor and the
10 voltage applied to the gate of the transistor during the non-selected period being biased from zero level and set within the range of the voltage level of the power source for driving the video signal.
 2. A method according to claim 1, in which the level of the video signal is non-symmetrical about a common electric potential.
 - 15 3. A method according to claim 1 or 2, in which the gate voltage applied to the gate of the transistor during the non-selected period is different during alternate positive and negative fields.
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