Description

This invention relates, in general, to microprocessors, and more particularly, to an architecture for a CMOS microprocessor.

The microprocessor has been catapulted into one of the most significant developments in the electronics field over the last decade. One of the reasons for this fast growth is the fact the technological advances into large scale integration have made the microprocessor the most effective, most reliable, simplest, and least expensive way of accomplishing complex electronic functions today. It is not surprising, therefore, that the microprocessor, or in a larger sense the microcomputer is dominating the technological development thinking for most equipment currently in the planning stages. The microcomputer is such a powerful performer that the vast majority of all possible applications probably could be served by any one of the dozens of different models available. Yet, for each application there probably is one microcomputer system which serves that purpose best. Despite occasional claims to the contrary, there is no such thing as a truly universal circuit, especially, not from the standpoint of cost-effectiveness. While one microcomputer system may come close to serving the bulk of all potential applications, it is likely that it will be over qualified for some, and under qualified for others. An over qualified system of course is not very cost effective. A microprocessor having CMOS transistors achieves the lowest possible power consumption. A CMOS microprocessor is known, for example, from IEE Transactions on Electron Devices, Volume ED-25, No. 8, August 1978, pages 952—959.

A microprocessor architecture employing a segmented bus and double incrementer structure using dual port register cells is known from European Patent Application No. 0,011,374, which falls under Article 54(3) of the European Patent Convention.

A microprocessor in accordance with the precharacterising portion of claim 1 is known from U.S. Patent No. 4030079.

Accordingly, it is an object of the present invention to provide a low cost, low power microprocessor having CMOS transistors and yet being capable of operating at speeds comparable to NMOS microprocessors.

Another object of the present invention is to provide a CMOS microprocessor having a common incrementer for a plurality of registers and using dual port storage cells in the registers which results in a reduction of chip area.

The invention as claimed is intended to achieve the above objects.

Brief Description of the Drawings

FIG. 1 illustrates, in block diagram form, the present invention in one form thereof;

FIG. 2 shows a portion of the incrementer register capable of incrementing one bit;

FIG. 3 illustrates in schematic and logic block form the interconnection scheme of one of the register cells with the buses; and

FIG. 4 shows some timing relationships helpful in better understanding the operation of the invention.

Detailed Description of the Drawings

Referring first to FIG. 1, there is illustrated an 8 bit fully static microprocessor containing RAM, timer, and input/output (I/O). The microprocessor has an ALU 11 having an input A, and input B, and a summation output. The summation output is coupled to an 8 bit data bus 12. Data bus 12 couples information to input A. Information is carried to input B by an 8 bit transfer bus 18. An accumulator 14 is coupled to both transfer bus 18 and data bus 12. Accumulator 14 is an 8 bit general purpose register used for arithmetic calculations and data manipulations. An 8 bit index register 16 is coupled between transfer bus 18 and data bus 12. Index register 16 is used during an index mode of addressing and provides an 8 bit address which may be added as an offset to create a new effective address. Index register 16 is also used for calculations and data manipulation during read/modify/write instructions, and as a temporary storage register when not in use for addressing purposes. A transmission gate 17 is used to couple data bus 12 to transfer bus 18. A condition code register 13 is coupled to internal data bus 50 and receives an input from ALU 11. Condition code register 13 is a 5 bit register and contains flags which reflects the results of ALU 11 operations. A first bit contained in condition code register 13 is a carry bit and is set when a carry or a borrow out of ALU 11 occurs during an arithmetic operation. The carry bit can also be modified by certain branch instructions. A second bit in condition code register 13 is a zero bit and is set whenever the result of the last arithmetic, logical, or data manipulation is zero. A third bit is a negative bit which indicates that the result of the last arithmetic, logical, or data manipulation is negative. A fourth bit is a mask interrupt bit and when set, disables both external and timer interrupts. Clearing the interrupt mask bit enables both of the interrupts. Both the timer and external interrupts are latched so that no interrupts are lost because of the interrupt mask bit being set. A fifth bit is a half carry bit, and is set if a carry occurs between bits 3 and 4 of the ALU during an add or an add with carry instruction.

An 8 bit address bus 19 is coupled to data bus 12 by transmission gate 26. Address bus 19 carries the lower 8 bits of an address. The microprocessor of FIG. 1 is capable of addressing up to 8K bytes of external memory with a multiplexed address/data bus. Address 19 is coupled to an output buffer 29 and to an incrementer 21. Buffer 29 provides buffered outputs on line 31 which is the 8 bit lower order output address bus. Incrementer 21 is an 8 bit incrementer which can decrement as well as increment. Incrementer 21 is coupled to three registers by line 28. The three registers are an address store register 22, a

program counter register 23, and a stack pointer 24. Address store 22 is an 8 bit register which is used to store a lower order effective address such as generated from a branch instruction. Program counter 23 is an 8 bit register which contains the lower 8 bits of a thirteen bit word which is used to point to the next instruction to be executed by the microprocessor. Stack pointer 24 is a 6 bit stack pointer which contains the address of the next free location on a push down/pop up stack. The stack pointer decrements during pushs and increments during pulls. Stack pointer 24 is used to store the location of the return address on subroutine calls and to store the location of the machine state during interrupts. In a preferred embodiment stack pointer 24 is an 8 bit register with the two most significant bits permanently set to a predetermined state.

The outputs of registers 22, 23, and 24 are connected to address bus 19. Program counter 23 also provides an output to data bus 12 via line 27. When one of register 22, 23, or 24 is desired to be modified its contents are transferred by address bus 19 to incrementer 21, where incrementer 21 can increment or decrement the contents, and the contents are then carried by line 28 back to any desired register. This arrangement of incrementer 21 with registers 22, 23 and 24 permit one common incrementer/ decrementer for three registers with one of the registers, the program counter, also being directly coupled to data bus 12. As mentioned hereinbefore, address bus 19 is coupled to data bus 12 by transmission gate 26.

It should be noted that although the buses are illustrated by one line that they are multiple lines with each different line carrying a different data bit.

The higher five bits of the address word is provided on line 42 by output buffer 41. Output buffer 41 is coupled to a 5 bit address bus 37. It should be noted that in a preferred embodiment, the lower eight bits of the address are multiplexed to external devices while the upper five bits are directly provided on interface pins. Address bus 37 is also coupled to an incrementer/decrementer 38 which is similar to incrementer 21 but only handles five bits. An address store register 32 is coupled from the output of incrementer 38 to address bus 37. Address store 32 contains the high bits of the address while address store 22 contains the lower eight bits of the address. A 5 bit program counter 33 is coupled between the output of incrementer 38 and address bus 37. A 5 bit temporary register 34 is coupled from the output of incrementer 38 to address bus 37. Program counter 33 also provides an output 36 to temporary register 34, which allows the contents of program counter 33 to be directly transferred into temporary register 34. This transfer between registers of course results in faster operation. The output of incrementer 38 is carried by a 5 bit bus or line 39 to registers 32, 33, and 34. Temporary register 34 is directly coupled to data bus 12 by interconnect bus 43. A bit code generator 44 is also connected to data bus 12 which allows any one of the bit lines of data bus 12 to be modified upon command.

An 8 bit internal data bus 50 is coupled by transmission gate 57 to data bus 12, by a transmission gate 58 to transfer bus 18, and receives information from data bus 12 by buffer/driver 55 and transmission gate 59. Buffer/driver 55 and transmission gate 59 are connected in series. As will be seen hereinafter, the registers are compact, fully static, and are not required to provide static current drive since the drive is provided by buffer 55. By having buffers/drivers 29, 41, and 55 the registers do not require large current drivers and therefore the entire microprocessor can be made smaller in size. An 8 bit I/O port 47 and an 8 bit I/O port 48 are coupled to internal data bus 50. I/O ports 47 and 48 contain data direction registers which control whether the individual interface pins associated with the I/O ports are serving as an input or an output for the microprocessor. Also coupled to internal data bus 50 is a random access memory (RAM) 49 which stores 8 bit words. In a preferred embodiment, RAM 49 stores 112 bytes. RAM 49 could be used for, among other things, a stack to store the contents of the registers during an interrupt.

Timer 51 is coupled to internal data bus 50 and has a single 8 bit counter with a 7 bit prescaler as its timer. The 8 bit counter is preset under program control and then decrements towards zero. When a zero crossing is detected the timer interrupt request bit of timer 51 is set, then, if a timer interrupt mask and the interrupt mask bit of condition code register 13 are both cleared the microprocessor receives an interrupt. The microprocessor now stores the appropriate registers on the stack, which is located in RAM 49, and then fetches the interrupt address vectors and begins servicing the interrupt. The prescaler of timer 51 is a 7 bit counter used to extend the maximum length of the timer. Timer 51 also provides an output to input/output logic 53. Input/output logic 53 provides an output to instruction decode and control logic 54. Input/output logic 53 receives and processes a reset and an interrupt request input. An 8 bit instruction register 52 is coupled from internal data bus 50 to instruction decode and control logic 54. Control logic 54 provides decoded instruction outputs and the necessary controls on output lines 56. The outputs on line 56 are used throughout the microprocessor to control the functioning and operation of the microprocessor, a few of such being transmission gates 17, 57, 58, and 59 and bit code generator 44. It is possible for the microprocessor to be a microcomputer simply by the addition of a read only memory (ROM) coupled to internal data bus 50.

Referring now to FIG. 2, there is illustrated a one bit portion of an incrementer/decrementer circuit such as will be found in incrementer 21 and incrementer 38. Also shown is an output bus latch and a cell typical of the cells used in the registers. An incrementer/decrementer circuit 110 receives a control signal at input 111. The control signal is an increment/decrement command which con-

trols N channel transistors 113 and 114. The increment/decrement command is coupled from input 111 to a gate electrode of transistor 114, and is inverted by inverter 112 and coupled to a gate electrode of transistor 113. Transistors 113 and 114 serve as controllable means for coupling inputs from inputs 126 and 127, respectively, to a source electrode of N channel transistor 118. N channel transistor 118 has its gate electrode connected to a gate electrode of a P channel transistor 117. The gate electrodes of transistors 117 and 118 are coupled to an input 116 which is a carry input. Transistors 117 and 118 are connected in series between a voltage terminal V_{DD} and a node formed between transistors 113 and 114. A node which is formed between transistors 117 and 118 is coupled to an input of inverter 121. Inverter 121 provides an output on output line 120 which is a carry/borrow output. The output of inverter 121 is also connected to a gate electrode of a P channel transistor 119. P channel transistor 119 is coupled from voltage terminal V_{DD} to the input of inverter 121 and forms a feedback means around inverter 121. Transistor 119 is only made conductive when the output of inverter 121 is a logic level low. A logic level low on the gate electrode of transistor 119 causes transistor 119 to conduct and maintain a logic level high at the input of inverter 121 thereby latching inverter 121 in a state to produce a logic level low output. Transistors 117, 118, 119, and 121 form a carry/borrow generator having controllable means 113 and 114 for coupling data bits or their complements from lines 126 and 127.

A P channel transistor 128 is connected in series with an N channel transistor 123 between voltage terminal V_{DD} and data input line 126. An output node is formed between transistors 123 and 128 and is connected to increment/decrement output 132. An N channel transistor 122 is coupled between output 132 and carry input 116. Transistor 122 has its gate electrode coupled to data input 126. A P channel transistor 129 is coupled in series with an N channel transistor 124 between voltage terminal V_{DD} and data input 127. An output node is formed between transistors 124 and 129 and is coupled to increment/decrement output 131. An N channel transistor 125 is coupled between output 131 and carry input 116. Transistor 125 has its gate electrode coupled to input 127. In a preferred embodiment, transistors 128 and 129 are P channel transistors, however, it will be noted that other suitable load devices could be substituted for transistors 128 and 129.

Data input 127 is a complement of data input 126. Increment/decrement outputs 131 and 132 are also complements of each other. Increment/decrement output 131 will be a logic level high when both inputs 116 and 127 are logic levels low or logic levels high. When output 131 is a logic level high then output 132 will be a logic level low. Increment/decrement output 132 will be a logic level high when both inputs 116 and 126 are both logic level lows or are both logic level highs. Circuit 110 is an incrementer when increment/decrement input 111 is held at a logic level high and is a decrementer when input 111 is held at a logic level low.

The circuits 110 would be interconnected so that the carry input 116 of one would receive the carry output 120 of the preceding circuit. The outputs 131 and 132 would each go to a respective storage cell of registers which are to be incremented or decremented. Examples of such registers are address storage register 22, 32, program counter register 23, 33, and stack pointer 24 (all of FIG. 1).

Output 131 is shown coupled to a pair of back-to-back inverters 148 and 149 by an N channel transistor 151. Inverters 148 and 149 form a latch or storage location of a typical static register. Transistor 151 has its gate electrode connected to line 156 which could carry a control signal such as an address store load command. Inverters 148 and 149 are also coupled to a bus 146 by an N channel transistor 152. Bus 146 could be an address bus within the microprocessor. Transistor 152 has its gate electrode connected to a line 157 which would carry a control signal such as a bus load command. Output 132 is coupled to inverters 148 and 149 by an N channel transistor 153 which has its gate electrode connected to control line 156. Inverters 148 and 149 are also coupled to a bus 147 by an N channel transistor 154 which is controlled by a control signal on line 157. It should be noted that buses 146 and 147 will carry complementary signals. Transistors 152 and 154 are enabled by the same command signal carried on line 157 and will accordingly couple the register true and its complement output to buses 146 and 147. The true and its complement are stored in the latch formed by inverters 148 and 149. Buses 146 and 147 are coupled to an output latch formed by a cross coupled pair of NAND gates 141 and 142. The output latch formed by logic gates 141 and 142 couples buses 146 and 147 to buses 143 and 144 which would represent the lower order output bus and its complement of line 31 shown in FIG. 1. This arrangement will cause buses 143 and 144 to be static buses. NAND gate 141 has a first input connected to bus 146 and a second input connected to the output from NAND gate 142, which is bus 144. Line 126 is also connected to output bus 144, and as discussed hereinbefore, line 126 serves as an input for increment/decrement circuit 110. NAND gate 141 has its first input connected to bus 147 and its second input connected to the output of NAND gate 141 which is also output bus 143. Line 127 is also connected to output bus 143.

FIG. 3 illustrates a storage cell for a single bit of one of the registers and its associated buses along with the precharge scheme used. The storage cell of the registers are dual access RAM cells and are connected to two buses in most of the cases. A transfer control signal on line 68 loads register cell 60 with the contents of BUS 2. Normally BUS 2 obtains its data from a drive large enough to overwrite the previous contents of register cell 60. When a transfer control signal is

present on line 69, the contents of register cell 60 is transferred to BUS 1 which serves as an output bus. Register cell 60 has back-to-back inverters 61 and 62. It should be noted by now that the bus structure of the micropocessor is such that the bus lines carry the true and well as complement data. When line 68 carries an enabling signal, N channel transistors 63 and 66 are enabled thereby allowing data from BUS 2 into cell 60 and the complement data from $\overline{\text{BUS 2}}$ to be coupled in by transistor 63 to the input of inverter 61. When a transfer control signal is present on line 69, N channel transistors 64 and 67 are enabled thereby allowing output data from inverter 61 to be coupled by transistor 67 to BUS 1 and complement data out of inverter 62 to be coupled by transistor 64 to $\overline{\text{BUS 1}}$. Line 69 is also connected to an input of OR gate 71. A second input for OR gate 71 is connected to line 72 which carries a control input so that the output of OR gate 71 can enable P channel precharge transistors 73 and 74. Transistor 73 has its gate electrode connected to the precharge output of OR gate 71, its source electrode connected to voltage terminal V_{DD}, and its drain electrode connected to BUS 1. Transistor 74 has its gate electrode connected to the precharge output of OR gate 71, its source electrode connected to voltage terminal V_{DD}, and its drain electrode connected to $\overline{\text{BUS 1}}$. On one portion of the clock cycle, BUS 1 and $\overline{\text{BUS 1}}$ will be precharged, and on another portion transfer control signal will enable transistors 64 and 67 so that data can be transferred to BUS 1 and $\overline{\text{BUS 1}}$. The cycle then repeats itself.

A pair of NAND gates 78 and 79 are interconnected to form a latch. Any information transferred to the address or data buses will be latched. The output of NAND gate 78 is connected to one of the inputs of NAND gate 79 and the output of NAND gate 79 is connected to one of the inputs of NAND gate 78. A second input of gate 78 is connected to BUS 1 while a second input of gate 79 is connected to $\overline{\text{BUS 1}}$. NAND gates 78 and 79 form an output latch which provides a true and its complement output for an output bus. Also connected between the second inputs of gates 78 and 79 are two P channel transistors 76 and 77. Transistor 77 has its gate electrode connected to the second input of gtate 78, has a first electrode connected to voltage terminal V_{DD}, and has a second electrode connected to the second input of gate 79. Transistor 76 has its gate electrode connected to the second input of gate 79, has a first electrode connected to voltage terminal V_{DD}, and has a second electrode connected to the second input of gate 78. The purpose of transistor 77 is to place a full voltage amplitude logic "1" level on the second input of gate 79 when the second input to gate 78 is a logic level "0". Gate 76 provides a full voltage amplitude logic level "1" to the second input of gate 78 when the second input to gate 79 is a logic level "0".

FIG. 4 is a timing diagram showing some timing relationships that could be helpful in better understanding the operation of the microprocessor. The top two waveforms, Ø1 and Ø2, are processor clock signals. Next are the timing waveforms useful in following a Load Accumulator from Memory instruction, LDA. Signal LI represents the time to load instruction register 52. Address registers 22 and 32, program counters 23 and 33, and incrementer 21 and 38 are used in LDA. Register to bus transfers occur on Ø1, e.g., ASL → ABL, ASH → ABH and PCL → ABL, PCH → ABH. The incrementers transfer back to the registers during Ø2. The waveform labeled AS → AB represents timing for address storage registers 22 and 32 transfers to address buses 19 and 37 respectively. The INC → PC waveform represents timing for incrementers 21 and 38 transfer to program counters 23 and 33 respectively. The PC → AB waveform represents timing for program counters 23 and 33 transfers to address buses 19 and 37 respectively. The INC → AS waveform represents timing for incrementers 21 and 38 transfers to address storage registers 22 and 32 respectively.

The AS waveform is the address strobe, DS waveform is the data strobe, and MUX BUS is the multiplexed bus which alternates between carrying the effective address and input data. The multiplexed bus would be coupled to internal data bus 50. Waveforms DBI and DB are some of the signals required in transferring data from internal data bus (DBI) 50 to accumulator 14. First, operand data goes to data bus (DB) from the internal data bus (DBI), then to the A input of ALU 11 to be ANDed with highs on input B, and back to accumulator 14 on the following Ø1 pulse. Note that this overlaps the loading of the next instruction and reduces the cycle length, which is possible because data bus 12 is not used for instruction loading, decoding or address transferring. Dotted line 80 indicates the beginning of the next instruction.

By now it should be appreciated that there has been provided a new and improved microprocessor structure which permits transfers between registers such as from program counter 33 to temperary register 34, and from an incrementer to at least three other registers. Data transfers are also permitted from an internal data bus 50 to a transfer bus 18. Transfers from program counter 23 directely to data bus 12 are also possible. The layout of the registers, their cells, and buffer drivers result in a compact, fully static microprocessor. Since the buses are static, the lower order 8 bit temporary register has been eliminated. The arrangement of the buffer/driver easily permits more registers to be added since compact registers are used. The incrementers can easily handle additional registers.

Claims

1. A microprocessor comprising:
a first data bus (12);
a transfer bus (18);
an arithmetic logic unit (11) having a first input coupled to the first data bus (12), a second input

present on line 69, the contents of register cell 60 is transferred to BUS 1 which serves as an output bus. Register cell 60 has back-to-back inverters 61 and 62. It should be noted by now that the bus structure of the micropocessor is such that the bus lines carry the true and well as complement data. When line 68 carries an enabling signal, N channel transistors 63 and 66 are enabled thereby allowing data from BUS 2 into cell 60 and the complement data from $\overline{\text{BUS 2}}$ to be coupled in by transistor 63 to the input of inverter 61. When a transfer control signal is present on line 69, N channel transistors 64 and 67 are enabled thereby allowing output data from inverter 61 to be coupled by transistor 67 to BUS 1 and complement data out of inverter 62 to be coupled by transistor 64 to $\overline{\text{BUS 1}}$. Line 69 is also connected to an input of OR gate 71. A second input for OR gate 71 is connected to line 72 which carries a control input so that the output of OR gate 71 can enable P channel precharge transistors 73 and 74. Transistor 73 has its gate electrode connected to the precharge output of OR gate 71, its source electrode connected to voltage terminal V_{DD}, and its drain electrode connected to BUS 1. Transistor 74 has its gate electrode connected to the precharge output of OR gate 71, its source electrode connected to voltage terminal V_{DD}, and its drain electrode connected to $\overline{\text{BUS 1}}$. On one portion of the clock cycle, BUS 1 and $\overline{\text{BUS 1}}$ will be precharged, and on another portion transfer control signal will enable transistors 64 and 67 so that data can be transferred to BUS 1 and $\overline{\text{BUS 1}}$. The cycle then repeats itself.

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The AS waveform is the address strobe, DS waveform is the data strobe, and MUX BUS is the multiplexed bus which alternates between carrying the effective address and input data. The multiplexed bus would be coupled to internal data bus 50. Waveforms DBI and DB are some of the signals required in transferring data from internal data bus (DBI) 50 to accumulator 14. First, operand data goes to data bus (DB) from the internal data bus (DBI), then to the A input of ALU 11 to be ANDed with highs on input B, and back to accumulator 14 on the following Ø1 pulse. Note that this overlaps the loading of the next instruction and reduces the cycle length, which is possible because data bus 12 is not used for instruction loading, decoding or address transferring. Dotted line 80 indicates the beginning of the next instruction.

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Claims

1. A microprocessor comprising:
a first data bus (12);
a transfer bus (18);
an arithmetic logic unit (11) having a first input coupled to the first data bus (12), a second input

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(12)

coupled to the transfer bus (18), and an output coupled to the first data bus (12);

an index register (16) comprising a plurality of dual port storage cells and having inputs and outputs coupled to the first data bus (12) and to the transfer bus (18);

an accumulator register (14) comprising a plurality of dual port storage cells and having inputs and outputs coupled to the first data bus (12) and to the transfer bus (18);

a first address bus (19);

a first incrementer bus (28);

a first incremeter (21) having an input coupled to the first address bus (19), and an output coupled to the first incrementer bus (28);

a stack pointer register (24) comprising a plurality of dual port storage cells and having an input, and an output coupled to the first address bus (19);

a first program counter register (23) comprising a plurality of dual port storage cells and having an input coupled to the first incrementer bus (28), a first output coupled to the first address bus (19), and a second output coupled to the first data bus (12);

a second address bus (37);

a second incrementer bus (39);

a second incrementer (38) having an input coupled to the second address bus (37), and an output coupled to the second incrementer bus (39);

a second program counter register (33) comprising a plurality of dual port storage cells and having an input coupled to the second incrementer bus (39), and an output coupled to the second address bus (37);

a temporary storage register (34) comprising a plurality of dual port storage cells and having an input coupled to the first data bus (12), and outputs coupled to the second address bus (37) and to the first data bus (12);

a second data bus (50);

a condition code register (13) having an input coupled to the arithmetic logic unit (11), and an output coupled to the second data bus (50);

first switching means (57) for selectively coupling the second data bus (50) to the first data bus (12);

second switching means (59) including driver means (55) for selectively coupling the first data bus (12) to the second data bus (50);

an instruction register (52) having an input coupled to the second data bus (50), and an output; and

instruction decode and control means (54) coupled to the output of the instruction register (52), for controlling the operation of the arithmetic logic unit (11), the registers (13, 14, 16, 22, 23, 24, 32, 33, 34, 52), the incrementers (21, 38), and the switching means (26, 57) in response to the contents of the instruction register (52), characterised in that

the microprocessor is a CMOS microprocessor,

the buses are static buses;

the stack pointer register (24) input is coupled to the first incrementer bus (28),

the temporary storage register (34) has inputs coupled to the second incrementer bus (39) and to an output of the second program counter register (33),

the code condition register (13) has an input coupled to the second data bus (50), and

the microprocessor further comprises:

third switching means (26) for selectively coupling the first address bus (19) to the first data bus (12);

a first address store register (22) comprising a plurality of dual port storage cells and having an input coupled to the first incrementer bus (28), and an output coupled to the first address bus (19);

a second address store register (32) comprising a plurality of dual port storage cells and having an input coupled to the second incrementer bus (39), and an output coupled to the second address bus (37); and

input/output means (47, 48) for control by the instruction decode and control means (54) for selectively coupling the second data bus (50) to devices external of the microprocessor.

2. The microprocessor of claim 1 further including a random access memory (49) coupled to the second data bus (50).

3. The microprocessor of claim 1 further including a first output buffer (29) coupled to the first address bus (19), and a second output buffer (41) coupled to the second address bus (37).

4. The microprocessor of claim 1 further including a bit code generator (44) coupled to the first data bus (12) for setting or resetting selected bits of data carried by the first data bus (12) under control of the instruction decode and control means (54).

5. The microprocessor of claim 1 wherein the switching means (26, 57, 59) comprise transmission gates.

6. The microprocessor of claim 1 further having fourth switching means (58) for selectively coupling the second data bus (50) to the transfer bus (18), and having fifth switching means (17) for selectively coupling the first data bus (12) to the transfer bus (18).

7. The microprocessor of claim 6 wherein the switching means (17, 26, 57, 58, 59) comprise transmission gates.

Revendications

1. Micro-processeur comportant: une première ligne omnibus de données (12), une ligne omnibus de transfert (18), une unité arithmétique et logique (11) comprenant une première entrée reliée à la première ligne omnibus de données (12), une seconde entrée reliée à la ligne omnibus de transfert (18) et une sortie reliée à la première ligne omnibus de données (12); un registre d'index (16) comprenant plusieurs cellules de mémoire à double connexion et avec des entrées et des sorties reliées à la

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première ligne omnibus de données (12) et à la ligne omnibus de transfer (18); un registre accumulateur (14) comprenant plusieurs cellules de mémoire à double connexion et avec des entrées et des sorties reliées à la première ligne omnibus de données (12) et à la ligne omnibus de transfert (18); une première ligne omnibus d'adresse (19); une première ligne omnibus d'incrémenteurs (28), un premier incrémenteur (21) dont une entrée est connectée à la première ligne omnibus d'adresse (19) et dont une sortie est reliée à la première ligne omnibus d'incrémenteur (28); un registre d'indicateur de pile (24) comprenant plusieurs cellules de mémoire à double connexion et avec une entrée et une sortie reliée à la première ligne omnibus d'adresse (19); un premier registre compteur de programme (23) comprenant plusieurs cellules de mémoire à double connexion et avec une entrée reliée à la première ligne omnibus d'incrémenteur (28), une première sortie reliée à la première ligne omnibus d'adresse (19) et une seconde sortie reliée à la première ligne omnibus de données (12); une seconde ligne omnibus d'adresse (37); une seconde ligne omnibus d'incrémenteur (39); un second incrémenteur (38) avec une entrée reliée à la seconde ligne omnibus d'adresse (37) et une sortie reliée à la seconde ligne omnibus d'incrémenteur (39); un second registre compteur de programme (34) comprenant plusieurs cellules de mémoire à double connexion, avec une entrée reliée à la seconde ligne omnibus d'incrémenteur (39) et une sortie reliée à la seconde ligne omnibus d'adresse (37); un registre de mémorisation temporaire (34) comprenant plusieurs cellules de mémoire à double connexion, avec une entrée reliée à la première ligne omnibus de données (12) et des sorties reliées à la seconde ligne omnibus d'adresse (37) et à la première ligne omnibus de données (12); une seconde ligne omnibus de données (50); un registre de code de condition (13) dont une entrée est reliée à l'unité arithmétique et logique (11) et dont une sortie est reliée à la seconde ligne omnibus de données (50); un premier dispositif de commutation (57) destiné à coupler sélectivement la seconde ligne omnibus de données (50) avec la première ligne omnibus de données (12); un second dispositif de commutation (59) comprenant un circuit d'attaque (55) pour coupler sélectivement la première ligne omnibus de données (12) avec la seconde ligne omnibus de données (50); un registre d'instruction (52) dont une entrée est reliée à la seconde ligne omnibus de données (50) et une sortie; et un circuit (54) de décodage de commande d'instruction couplé avec la sortie du registre d'instructions (52) pour commander le fonctionnement de l'unite arithmetique et logique (11), des registres (13, 14, 16, 22, 23, 24, 32, 33, 34, 52), des incrémenteurs (21, 38) et du circuit de commutation (26, 57) en réponse au contenu du registre d'instruction (52), caractérisé en ce que le micro-processeur est un micro-processeur CMOS les lignes omnibus sont des lignes omnibus statiques; l'entrée du registre indicateur de pile (24) est reliée à la première ligne omnibus d'incrémenteur (28), le registre de mémorisation temporaire (34) a des entrées connectées à la seconde ligne omnibus d'incrémenteur (39) et à la sortie du second registre compteur de programme (33), le registre de condition de code (13) comporte une entrée connectée à la seconde ligne omnibus de données (50) et le micro-processeur comporte en outre: un troisième circuit de commutation (26) pour relier sélectivement la première ligne omnibus d'adresse (19) à la première ligne omnibus de données (12); un premier registre de mémorisation d'adresse (22) consistant en plusieurs cellules de mémoire à double connexion, avec une entrée reliée à la première ligne omnibus d'incrémenteur (28) et une sortie reliée à la première ligne omnibus d'adresse (19); un second registre de mémoire d'adresse (32) consistant en plusieurs cellules de mémoire à double connexion, avec une entrée reliée à la seconde ligne omnibus d'incrémenteur (39) et une sortie reliée à la seconde ligne omnibus d'adresse (37); et un circuit d'entrée/sortie (47, 48) pour commander par ledit dispositif de décodage et de commande d'instruction (54) le couplage sélectif de la seconde ligne omnibus de données (50) avec des dispositifs extérieurs au micro-processeur.

2. Micro-processeur selon la revendication 1, comportant en outre une mémoire à accès direct (49) reliée à la seconde ligne omnibus de données (50).

3. Micro-processeur selon la revendication 1, comportant en outre un premier tampon de sortie (29) relié à la première ligne omnibus d'adresse (19) et un second tampon de sortie (41) relié à la seconde ligne omnibus d'adresse (37).

4. Micro-processeur selon la revendication 1, comportant en outre un générateur de code binaire (44) relié à la première ligne omnibus de données (12) pour mettre à "1" ou "0" des bits sélectionnés de données transmis par la première ligne omnibus de données (12) à la commande du dispositif (54) de décodage de commande d'instruction.

5. Micro-processeur selon la revendication 1, dans lequel le circuit de commutation (26, 57, 59) consiste en des portes de transmission.

6. Micro-processeur selon la revendication 1, comportant en outre un quatrième dispositif de commutation (58) destiné à connecteur sélectivement la seconde ligne omnibus de données (50) à la ligne omnibus de transfert (18) et un cinquième dispositif de commutation (17) pour relier sélectivement la première ligne omnibus de données (12) à la ligne omnibus de transfert (18).

7. Micro-processeur selon la revendication 6, dans lequel les dispositifs de commutation (17, 26, 57, 58, 59) consistent en des portes de transmission.

Patentansprüche

1. Ein Mikroprozessor mit folgenden Merkmalen:

einem ersten Datenbus (12);

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einem Übertragungsbus (18);

einer arithmetischen logischen Einheit (11) mit einem ersten Eingang, der an den ersten Datenbus (12) angeschlossen ist, einem zweiten Eingang, der an den Übertragungsbus (18) angeschlossen ist und einem Ausgang, der an den ersten Datenbus (12) angeschlossen ist;

einem Indexregister (16) mit einer Mehrzahl von Speicherzellen mit zwei Toren, deren Eingänge und Ausgänge an den ersten Datenbus (12) und an den Übertragungsbus (18) angeschlossen sind;

einem Akkumulatorregister (14) mit einer Mehrzahl von Speicherzellen mit zwei Toren, deren Eingänge und Ausgänge an den ersten Datenbus und an den Übertragungsbus (18) angeschlossen sind;

einem ersten Adreßbus (19);

einem ersten Inkrementierbus (28);

einem ersten Inkrementierer (21), dessen Eingang an den ersten Adreßbus (19) und dessen Ausgang an den ersten Inkrementierbus (28) angeschlossen ist;

einem Stapelzeigerregister (24) mit einer Mehrzahl von Speicherzellen mit zwei Toren mit einem Eingang und einem Ausgang, der an den ersten Adreßbus (19) angeschlossen ist;

einem ersten Programmzählerregister (23) mit einer Mehrzahl von Speicherzellen mit zwei Toren, deren Eingang an den ersten Inkrementierbus (28) angeschlossen ist, deren erster Ausgang an den ersten Adreßbus (19) angeschlossen ist und deren zweiter Ausgang an den ersten Datenbus (12) angeschlossen ist;

einem zweiten Adreßbus (37);

einem zweiten Inkrementierbus (39);

einem zweiten Inkrementierer (38), dessen Eingang an den zweiten Adreßbus (37) und dessen Ausgang an den zweiten Inkrementierbus (39) angeschlossen ist;

ewinem zweiten Programmzählerregister (33) mit einer Mehrzahl von Speicherzellen mit zwei Toren, dessen Eingang an den zweiten Inkrementierbus (39) und dessen Ausgang an den zweiten Adreßbus (37) angeschlossen ist;

einem zeitweiligen Speicherregister (34) mit einer Mehrzahl von Speicherzellen mit zwei Toren, deren Eingang an den ersten Datenbus (12) und deren Ausgänge an den zweiten Adreßbus (37) und an den ersten Datenbus (12) angeschlossen sind;

einem zweiten Datenbus (50);

einem Zustandskoderegister (13), dessen Eingang an die arithmetische logische Einheit (11) und dessen Ausgang an den zweiten Datenbus (50) angeschlossen ist;

einer ersten Schalteinrichtung (57) zum wahlweise Ankoppeln des zweiten Datenbusses (50) an den ersten Datenbus (12);

einer zweiten Schalteinrichtung (59) mit einer Treibereinrichtung (55) zum wahlweise Ankoppeln des ersten Datenbusses (12) an den zweiten Datenbus (50);

einem Befehlsregister (52) mit einem Eingang, der an den zweiten Datenbus (50) angeschlossen ist, und mit einem Ausgang; und

einer Befehlsdekoder- und Steuereinrichtung (54), die an den Ausgang des Befehlsregisters (52) angeschlossen ist, um den Betrieb der arithmetischen logischen Einheit (11), der Register (13, 14, 16, 22, 23, 24, 32, 33, 34, 52), der Inkrementierer (21, 38) und der Schalteinrichtungen (26, 57) in Reaktion auf den Inhalt des Befehlsregisters (52),

dadurch gekennzeichnet,

daß der Mikroprozessor ein CMOS-Mikroprozessor ist,

daß die Busse statische Busse sind,

daß der Eingang des Stapelzeigerregister (24) an den ersten Inkrementierbus (28) angeschlossen ist,

daß das zeitweilige Speicherregister (34) mit seinen Eingängen an den zweiten Inkrementierbus (39) und an einen Ausgang des zweiten Programmzählerregisters (33) angeschlossen ist,

daß das Codezustandsregister (13) mit seinem Eingang an den zweiten Datenbus (50) angeschlossen ist, und

daß der Mikroprozessor folgende Merkmale aufweist:

eine dritte Schalteinrichtung (26) zum wahlweise Ankoppeln des ersten Adreßbusses (19) an den ersten Datenbus (12);

ein erstes Adreßspeicherregister (22) mit einer Mehrzahl von Speicherzellen mit zwei Toren, dessen Eingang an den ersten Inkrementierbus (28) angeschlossen ist und dessen Ausgang an den ersten Adreßbus (19) angeschlossen ist;

ein zweites Adreßspeicherregister (32) mit einer Mehrzahl von Speicherzellen mit zwei Toren und mit einem Eingang, der an den zweiten Inkrementierbus (39) angeschlossen ist, und mit einem Ausgang, der an den zweiten Adreßdatenbus (37) angeschlossen ist; und

eine Eingangs-/Ausgangs-Einrichtung (47, 48) zum Steuern der Instruktionsdekodier- und Steuer-Einrichtung (54) zum wahlweise Ankoppeln des zweiten Datenbusses (50) an außerhalb des Mikroprozessors liegende Geräte.

2. Der Mikroprozessor nach Anspruch 1, ferner mit einem Speicher (49) mit wahlfreiem Zugriff, der an den zweiten Datenbus (50) angeschlossen ist.

3. Der Mikroprozessor nach Anspruch 1, ferner mit einem ersten Ausgangspuffer (29), der an den ersten Adreßbus (19) angeschlossen ist, und einem zweiten Ausgangspuffer (41), der an den zweiten Adreßbus (37) angeschlossen ist.

4. Der Mikroprozessor nach Anspruch 1, ferner mit einem Bit-Kode-Generator (44), der an den ersten Datenbus (12) angeschlossen ist, um ausgewählte Bits der Daten, die durch den ersten Datenbus (12) unter der Steuerung der Befehlsdekodier- und Steuer-Einrichtung (54) geführt werden, zu setzen oder rückzusetzen.

5. Der Mikroprozessor nach Anspruch 1, bei dem die Schalteinrichtung (26, 57, 59) Übertragungsgatter aufweist.

6. Der Mikroprozessor nach Anspruch 1, ferner mit einer vierten Schaltvorrichtung (58) zum wahlweise Ankoppeln des zweiten Datenbusses (50) an den Übertragungsbus (18), und mit einer fünften Schalteinrichtung (17) zum wahlweise Ankoppeln

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des ersten Datenbusses (12) an den Übertragungsbus (18).

7. Der Mikroprozessor nach Anspruch 6, bei dem die Schalteinrichtung (17, 26, 57, 58, 59) Übertragungsgatter aufweist.

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