

WHAT IS CLAIMED IS:

1. An integrated circuit (IC) device comprising:
 - a substrate;
 - a connection component comprising a cavity defined therethrough, said connection component coupled to said substrate;
 - at least one memory die positioned in said cavity, said at least one memory die electrically coupled to said substrate; and
 - a logic die extending over said at least one memory die and at least a portion of said connection component, said at least one logic die electrically coupled to said connection component and said at least one memory die, wherein said connection component is free of through silicon vias, and wherein said connection component is electrically coupled to said substrate through at least one wire bond.
2. The IC device in accordance with Claim 1, wherein said connection component comprises a redistribution wiring layer comprising at least one wire bonding pad and said substrate comprises at least one substance bonding pad, and said at least one wire bonding pad is electrically coupled to said substrate bonding pad through said at least one wire bond.
3. The IC device in accordance with Claim 1, wherein said at least one memory die comprises an active surface, said active surface faces said substrate and faces away from said logic die.
4. The IC device in accordance with Claim 1, wherein said at least one memory die comprises an active surface, said active surface faces said logic die and faces away from said substrate.
5. The IC device in accordance with Claim 1, wherein said connection component is a passive connection component.
6. The IC device in accordance with Claim 5, wherein said passive connection component comprises at least one passive component embedded therein.

7. The IC device in accordance with Claim 6, wherein said passive component comprises one or more of the following: resistors, capacitors, and inductors.

8. The IC device in accordance with Claim 1, wherein said connection component is an active connection component.

9. The IC device in accordance with Claim 8, wherein said active connection component comprises at least one active electrical component embedded therein.

10. The IC device in accordance with Claim 9, wherein said active electrical component comprises one or more of the following: transistors, signal amplifiers, and signal filters.

11. An integrated circuit (IC) device comprising:

a substrate comprising a first active surface, said first active surface comprising a plurality of substrate bonding pads;

a plurality of connection components coupled to said first active surface, said plurality of connection components arranged to define a cavity between said plurality of connection components, each connection component of said plurality of connection components comprising a second active surface opposite said first active surface, each said second active surface comprising at least one connection component bonding pad;

at least one memory die positioned within said cavity and electrically coupled to said first active surface; and

a logic die coupled to each said second active surface and said at least one memory die, wherein said plurality of connection components are free of through silicon vias, and wherein each said at least one connection component bonding pad is electrically coupled to a substrate bonding pad of said plurality of substrate bonding pads through at least one wire bond.

12. The IC device in accordance with Claim 11, wherein at least one connection component of said plurality of connection components is a passive connection component.

13. The IC device in accordance with Claim 12, wherein said at least one passive connection component comprises at least one passive component embedded therein.

14. The IC device in accordance with Claim 13, wherein said at least one passive component comprises one or more of the following: resistors, capacitors, and inductors.

15. The IC device in accordance with Claim 11, wherein at least one connection component of said plurality of connection components is an active connection component.

16. The IC device in accordance with Claim 15, wherein said active connection component comprises at least one active electrical component embedded therein.

17. The IC device in accordance with Claim 16, wherein said active electrical component comprises one or more of the following: transistors, signal amplifiers, and signal filters.

18. A method of forming an IC device having a 3D package structure, said method comprising:

forming a connection component free of through silicon vias, the connection component including a cavity defined therethrough and a redistribution wiring layer including a connection component bonding pad;

coupling the connection component to a substrate, the substrate including a substrate bonding pad;

coupling at least one memory die to the substrate such that memory die is positioned within the cavity;

extending a logic die over the memory die and at least a portion of the connection component;

electrically coupling the logic die to the memory die and the at least a portion of the connection component; and

electrically coupling the connection component bonding pad to the substrate bonding pad through at least one wire bond.

19. The method in accordance with Claim 18, wherein forming the connection component comprises separately forming a plurality of connection components, each connection component of the plurality of connection components including a connection component bonding pad, and wherein coupling the connection component to a substrate comprises:

positioning the plurality of connection components on the substrate to define a cavity between the plurality of connection components; and

coupling the plurality of connection components to the substrate.

20. The method in accordance with Claim 18, wherein coupling the at least one memory die to the substrate comprises:

electrically coupling a first surface of the memory die to the substrate; and

electrically coupling a second surface of the memory die to the substrate through a plurality of through silicon vias formed in the memory die, the second surface opposite the first surface.