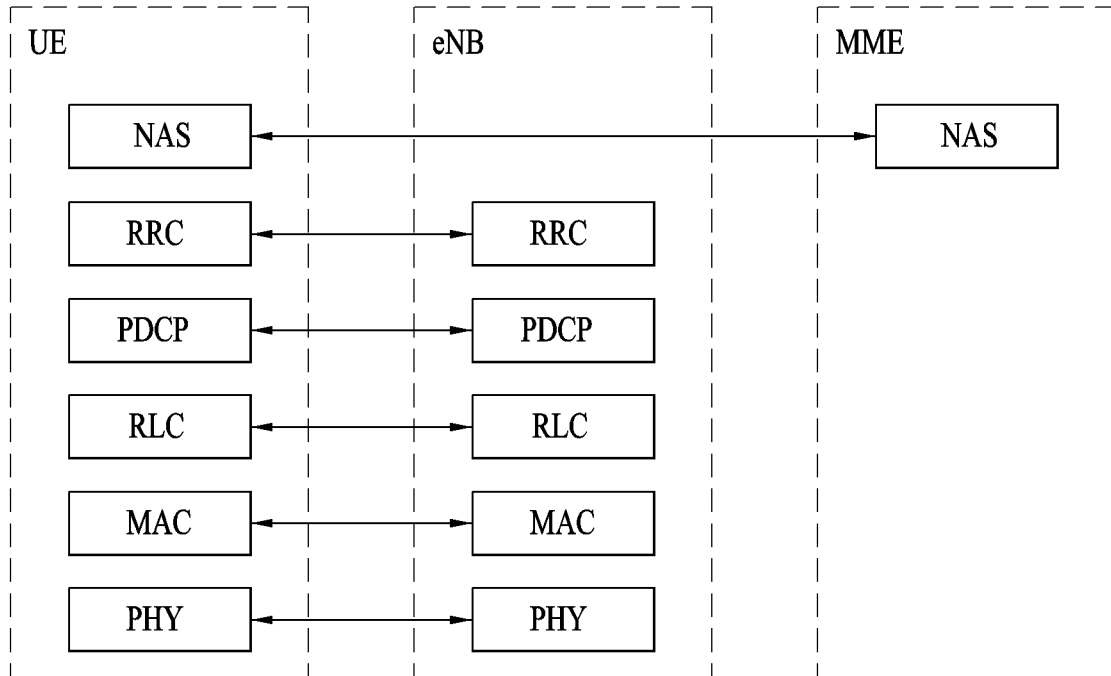
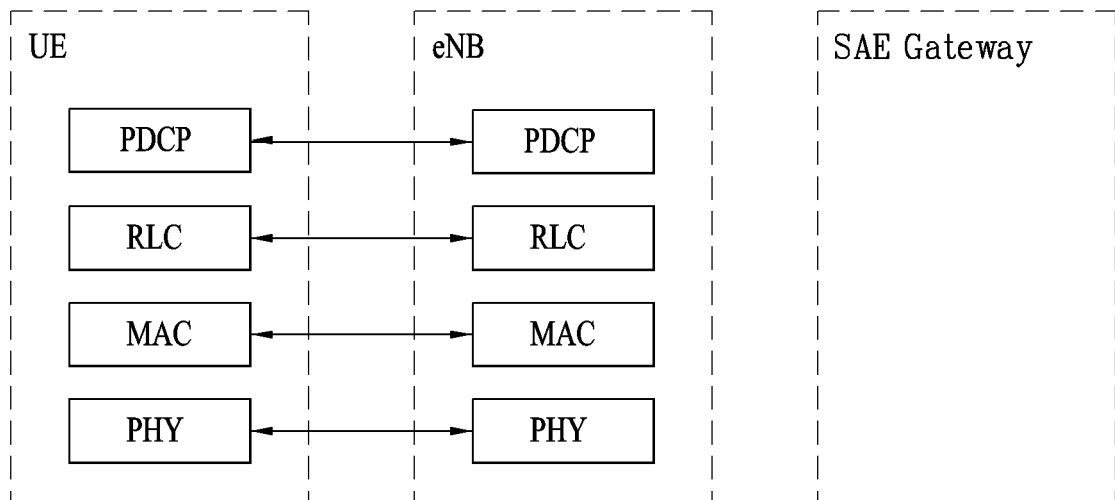


FIG. 1



(A) CONTROL-PLANE PROTOCOL STACK



(B) USER-PLANE PROTOCOL STACK

FIG. 2

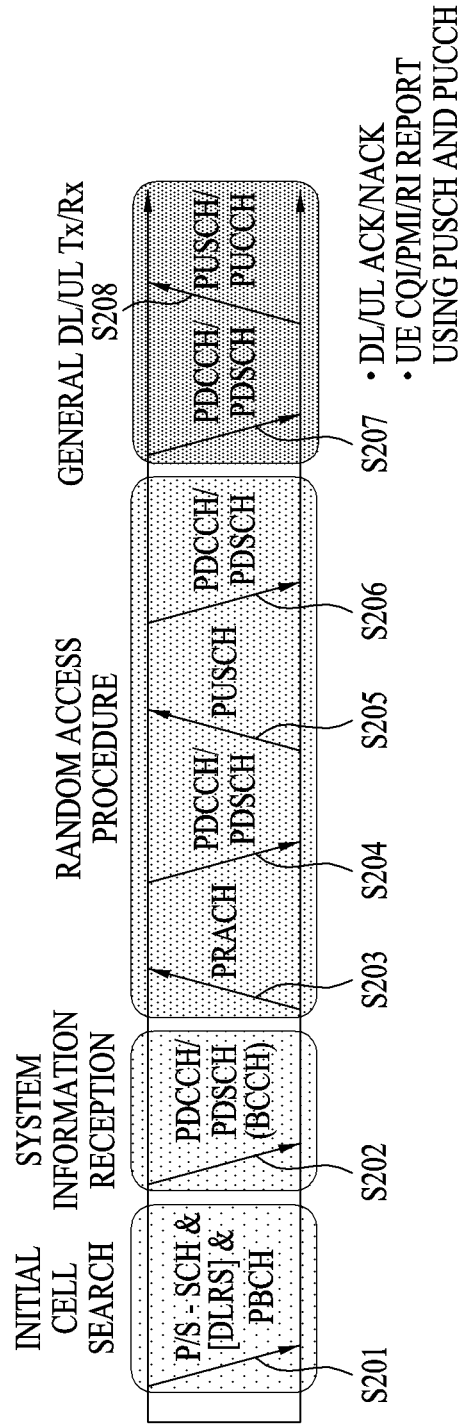


FIG. 3

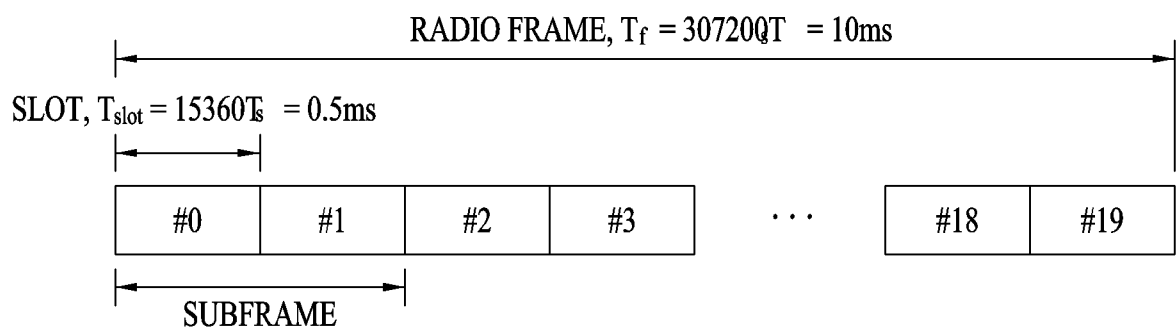


FIG. 4

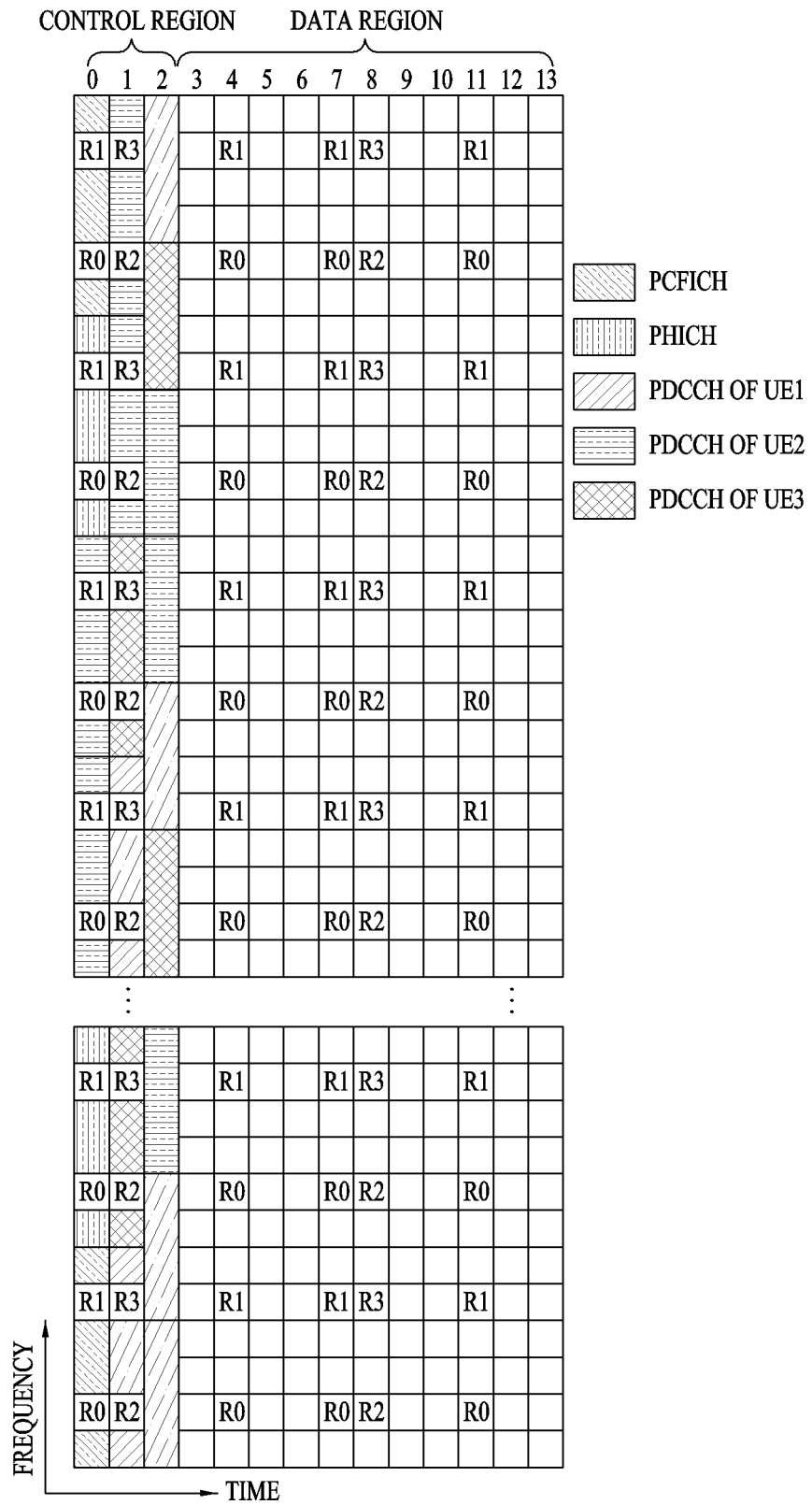
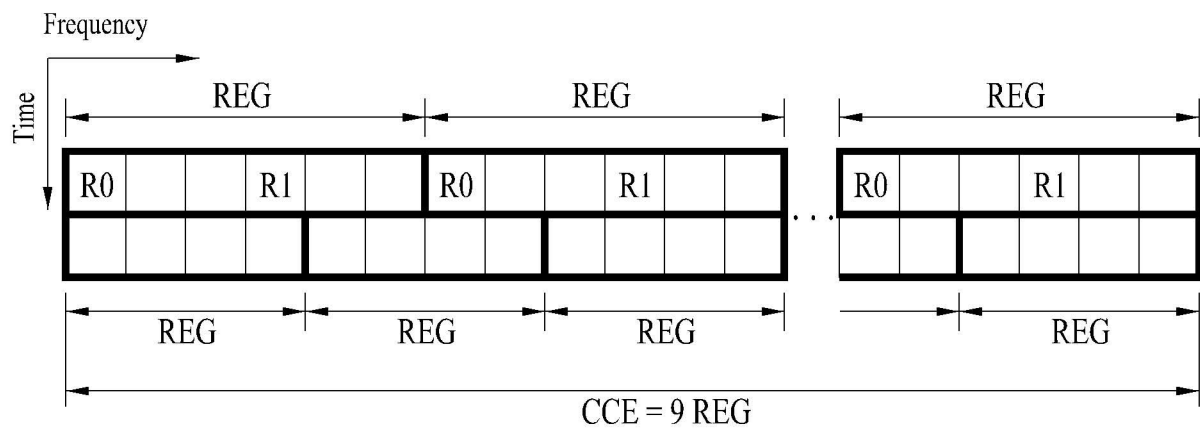
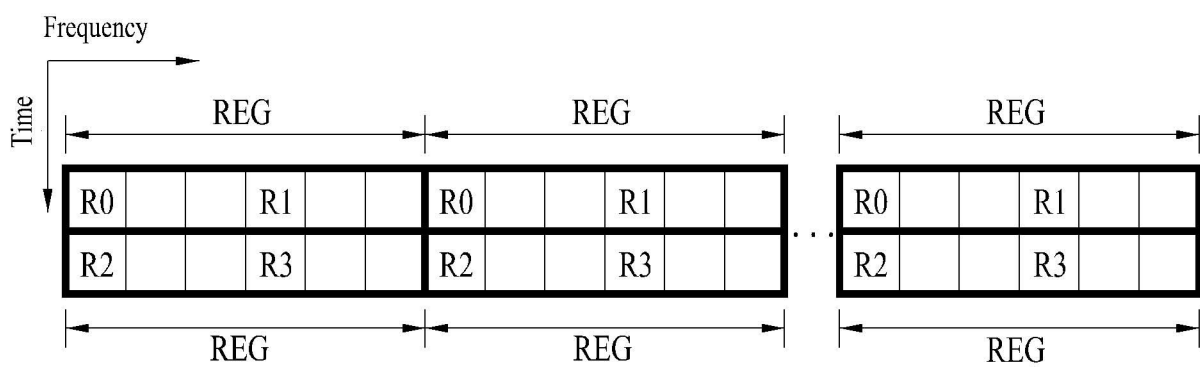


FIG. 5



(a) 1 Tx or 2 Tx



(b) 4 Tx

FIG. 6

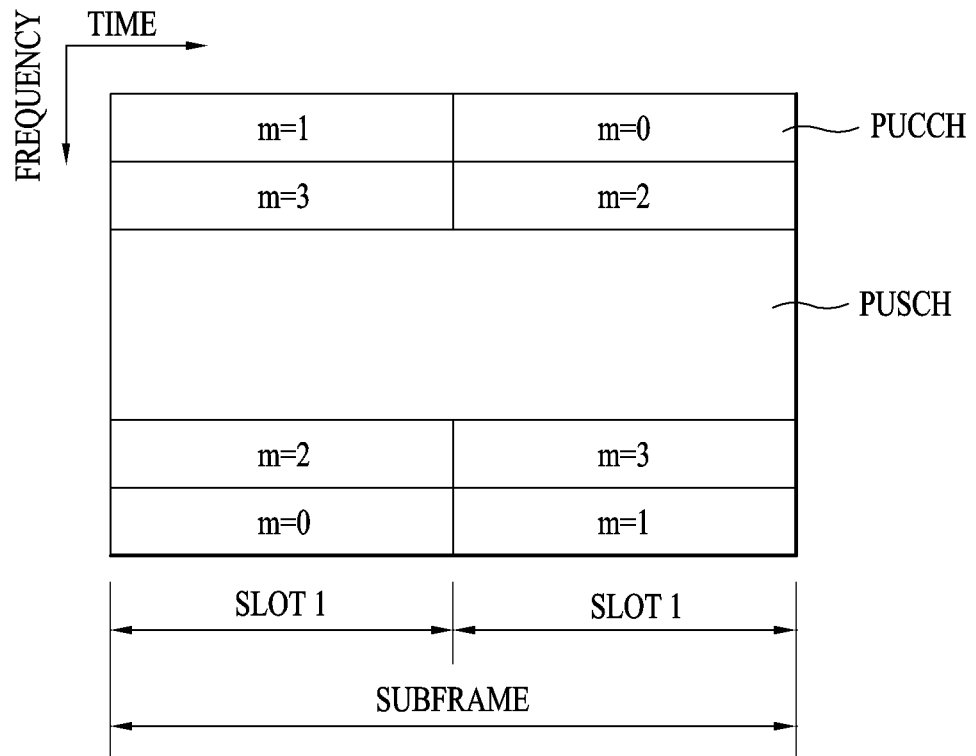


FIG. 7

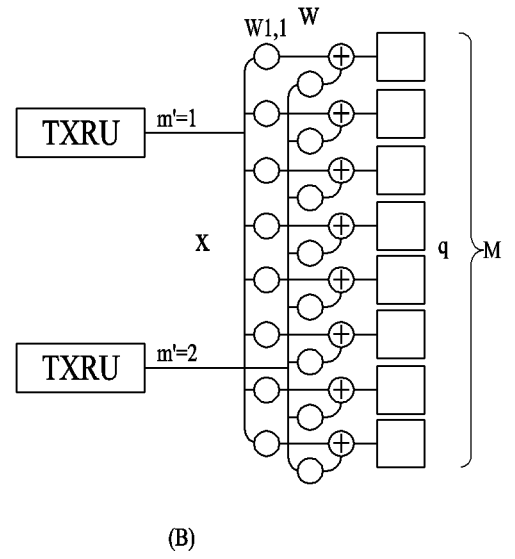
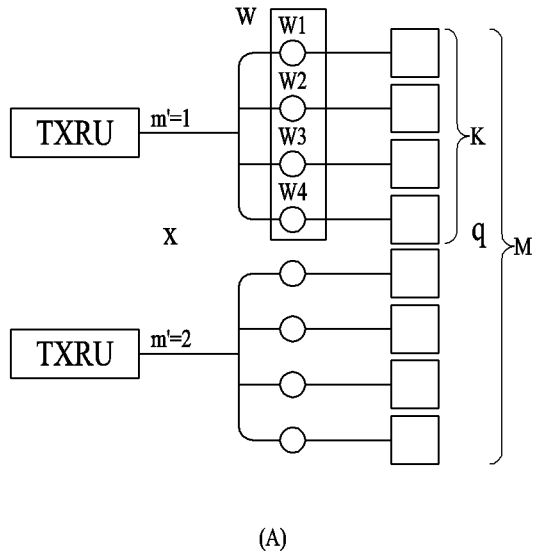
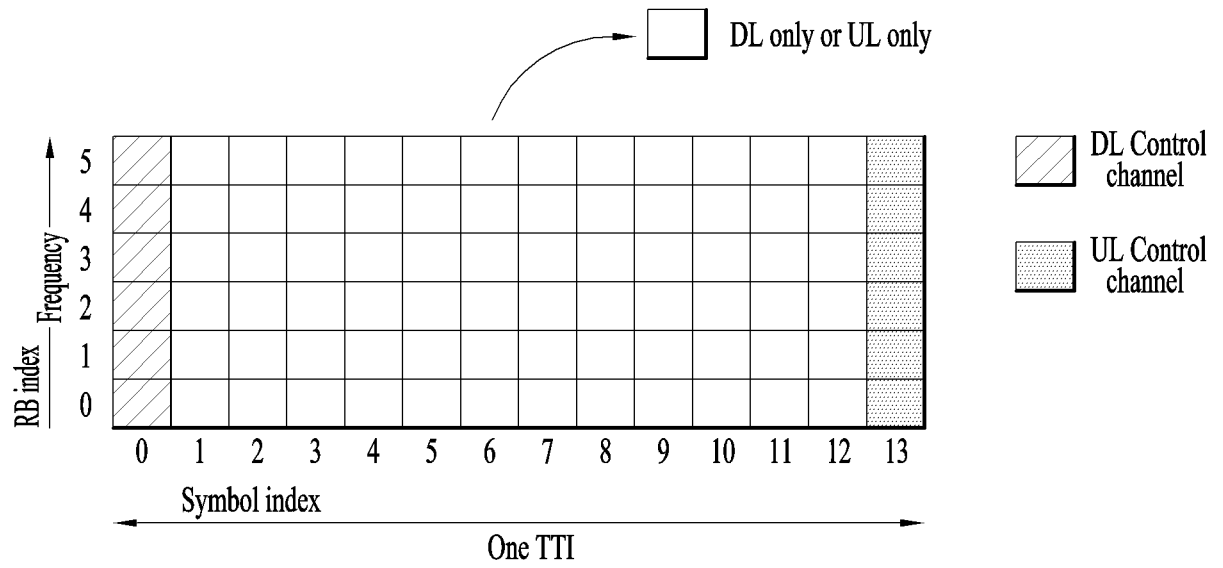
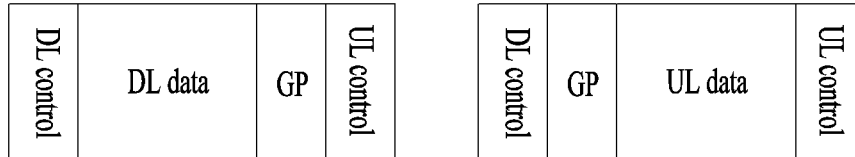


FIG. 8



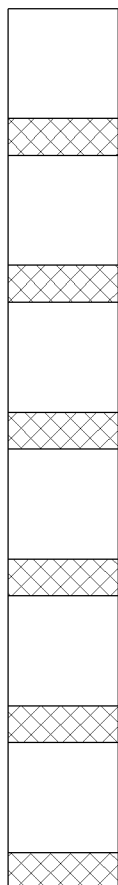
(a)



(b)

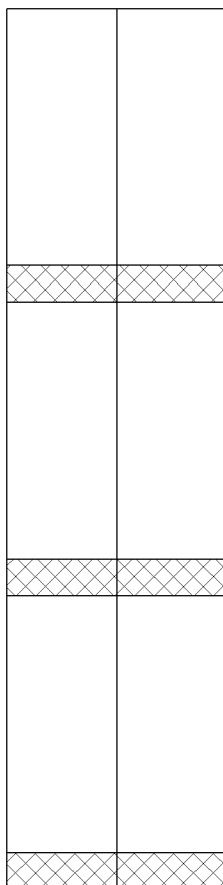
FIG. 9

CORESET
duration : 1



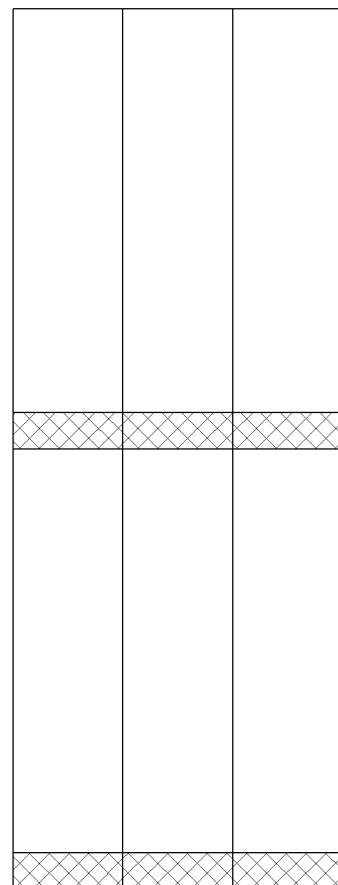
No bundling

CORESET
duration : 2



Bundling size : 2

CORESET
duration : 3



Bundling size : 3

FIG. 10

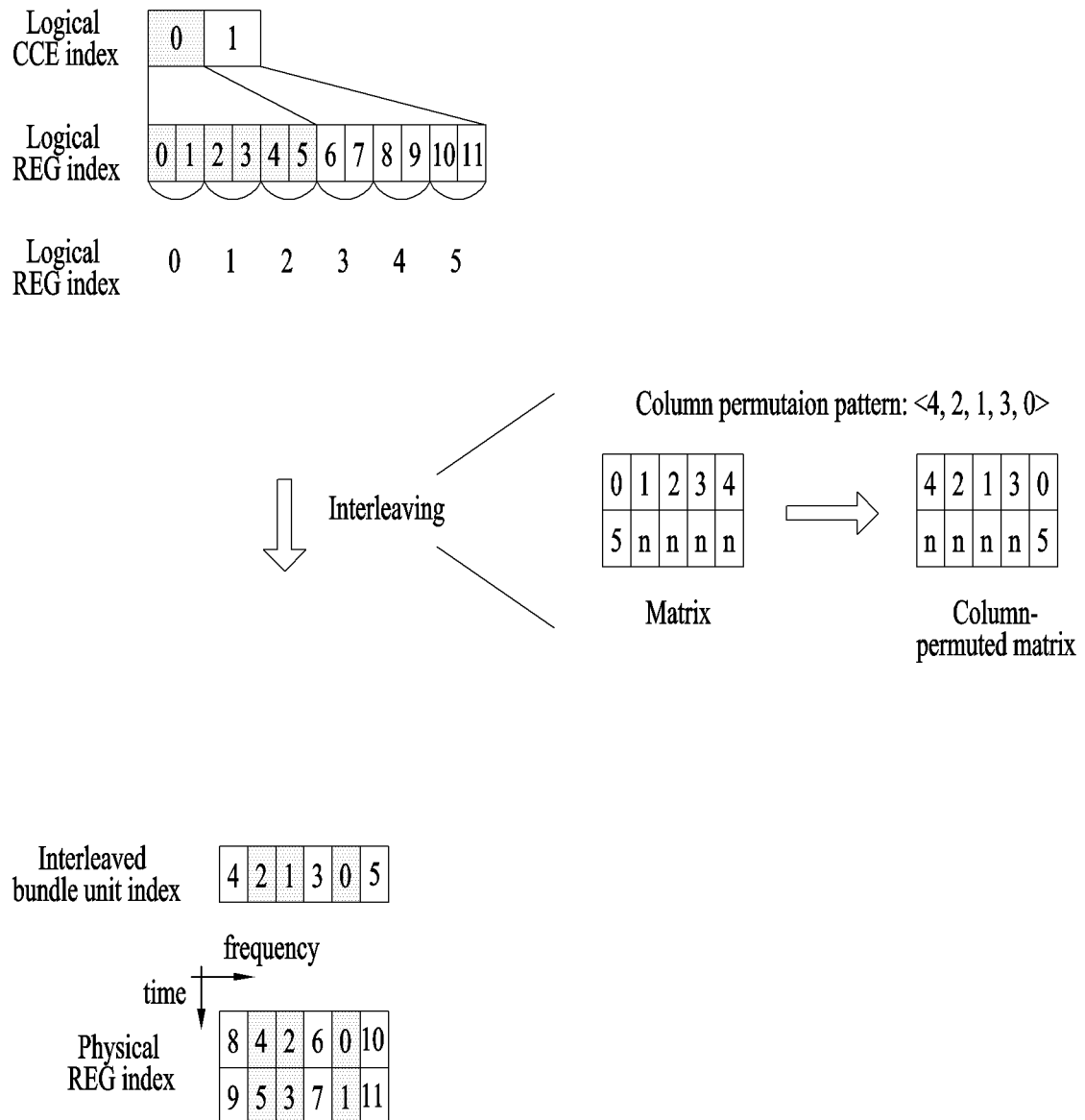


FIG. 11

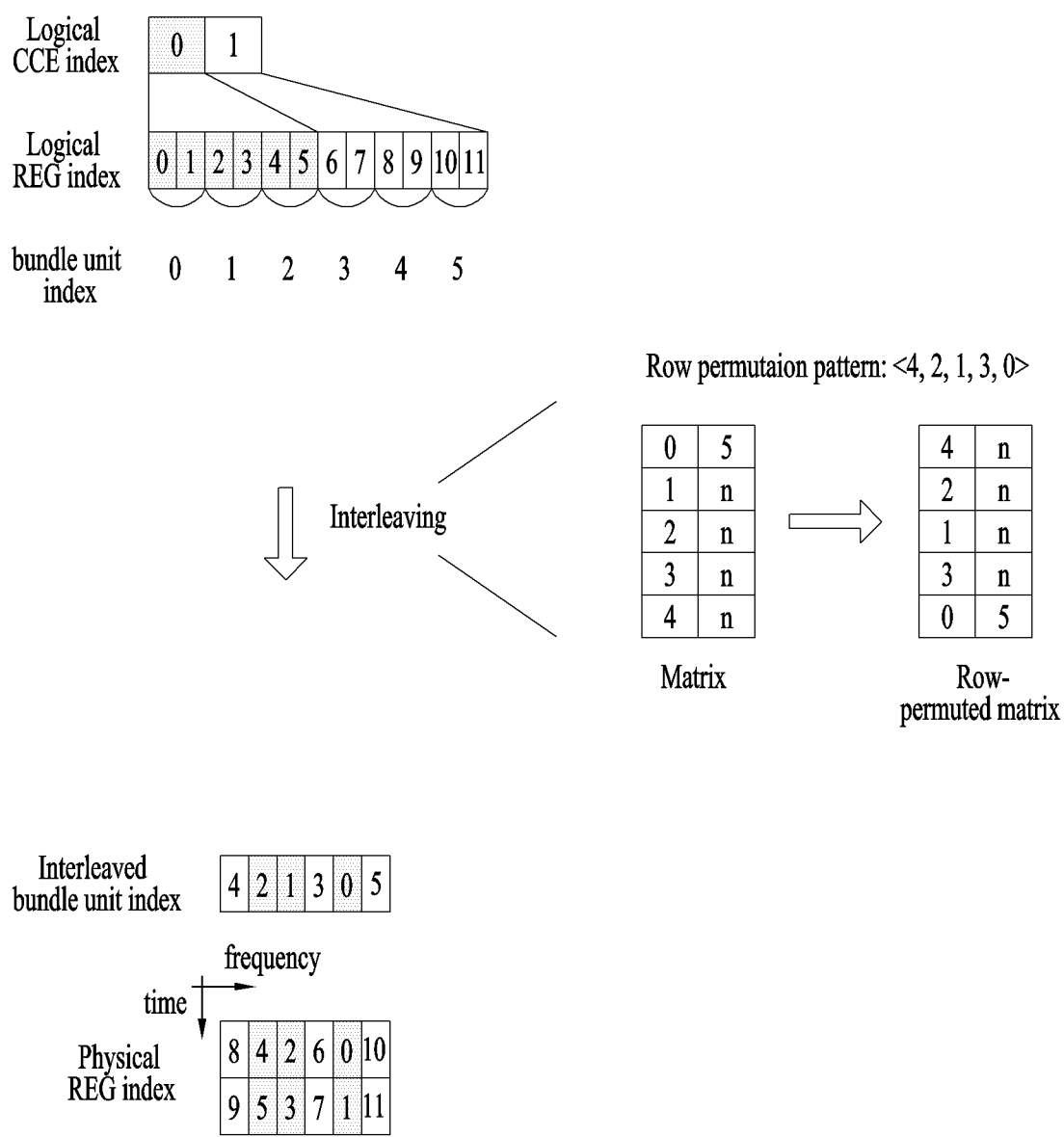


FIG. 12

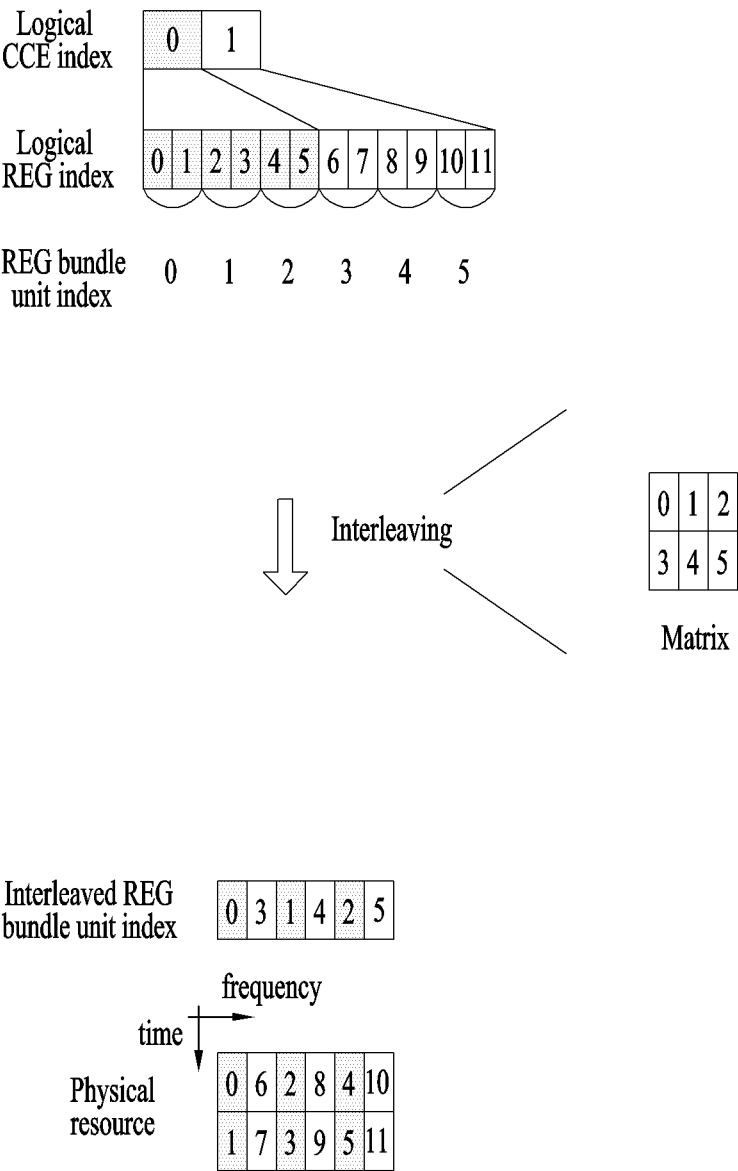


FIG. 13

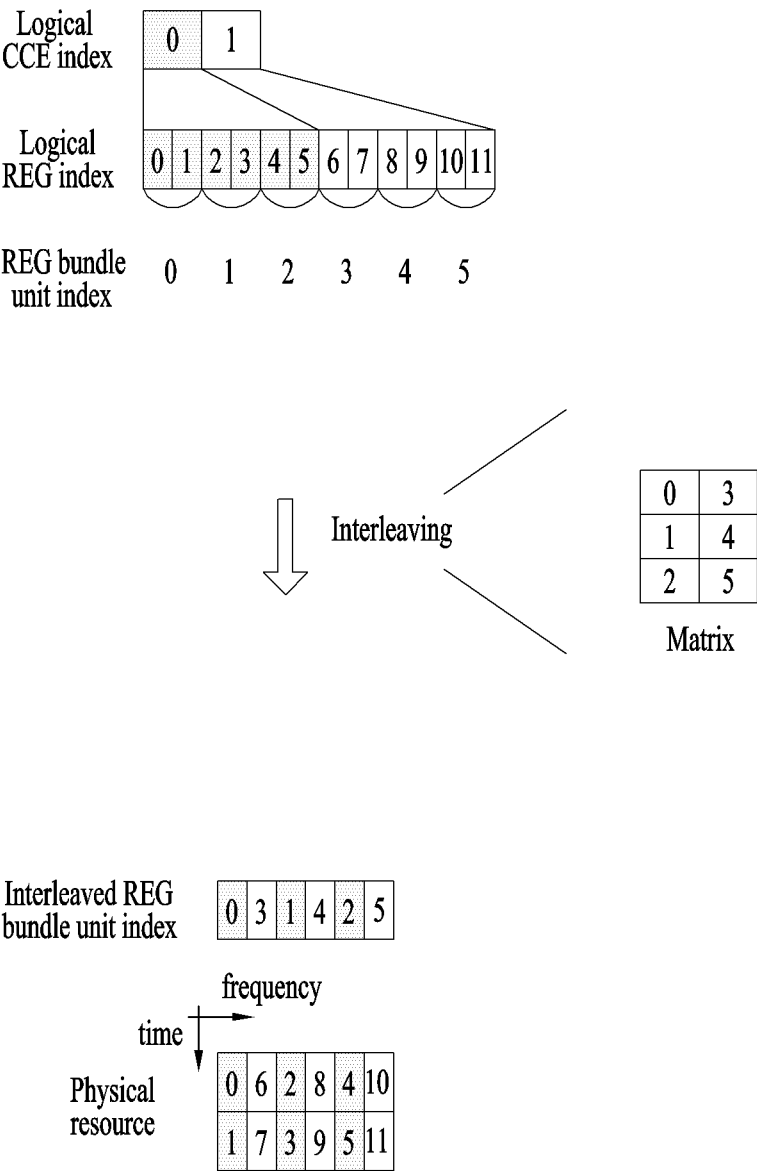
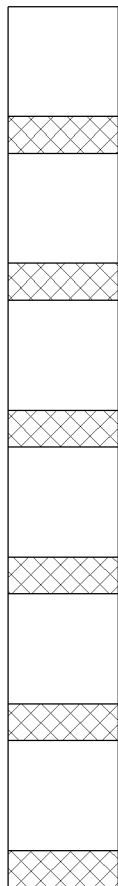


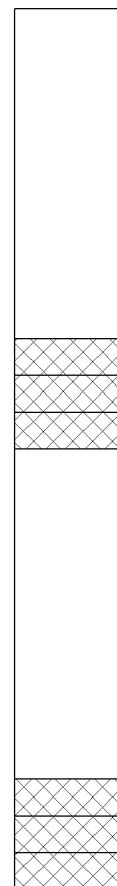
FIG. 14



No bundling



Bundling size : 2



Bundling size : 3

FIG. 15

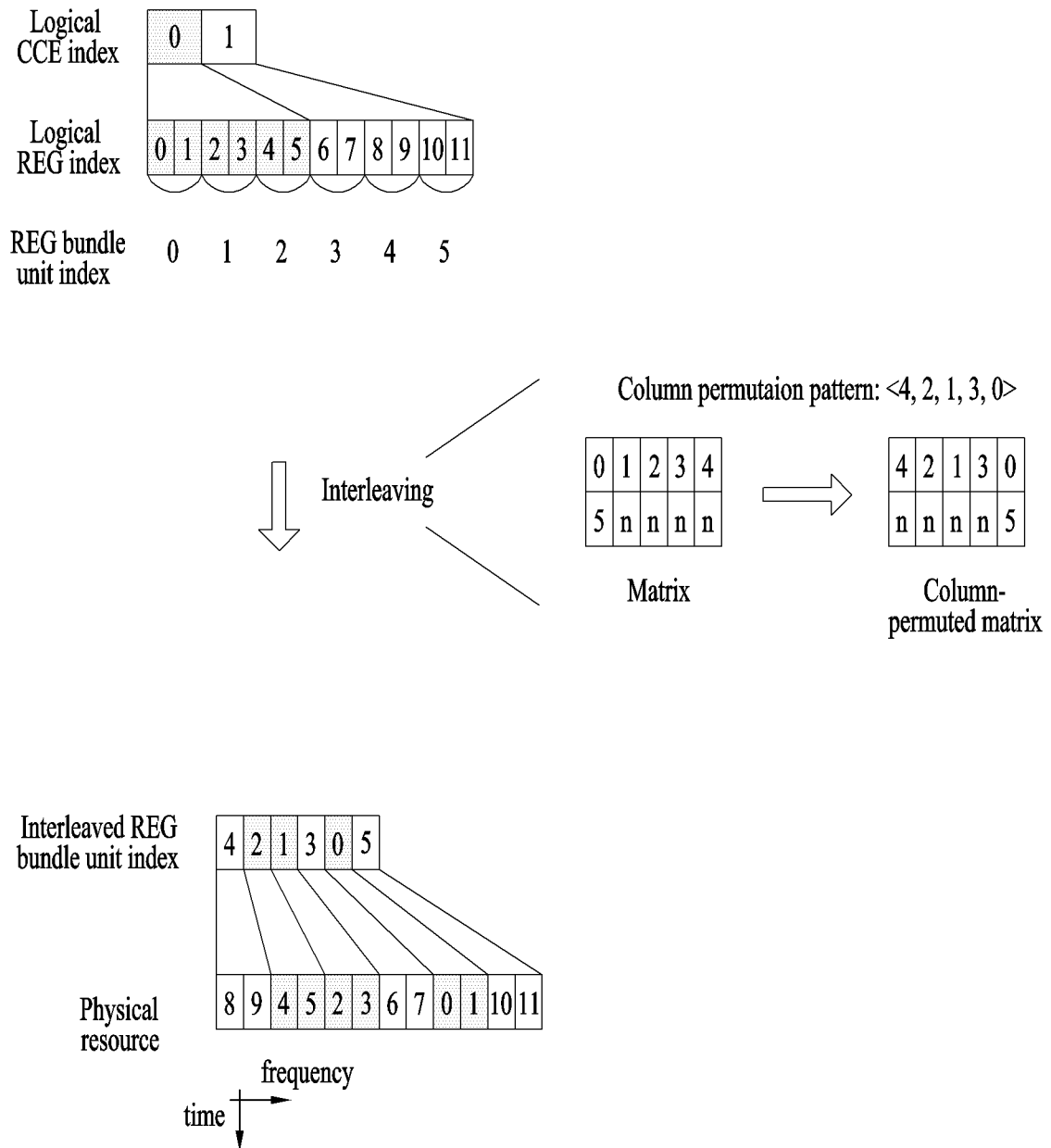


FIG. 16

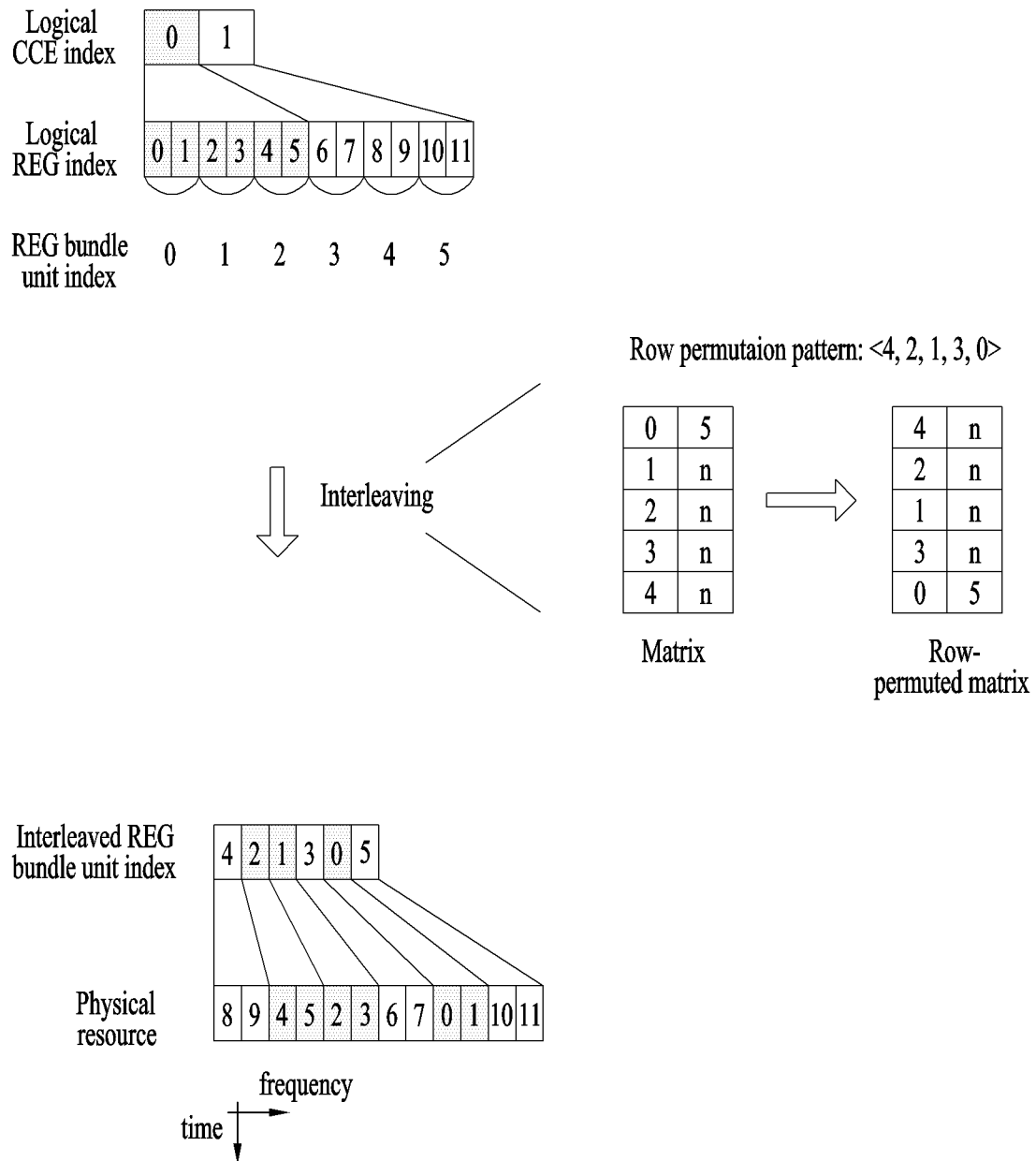


FIG. 17

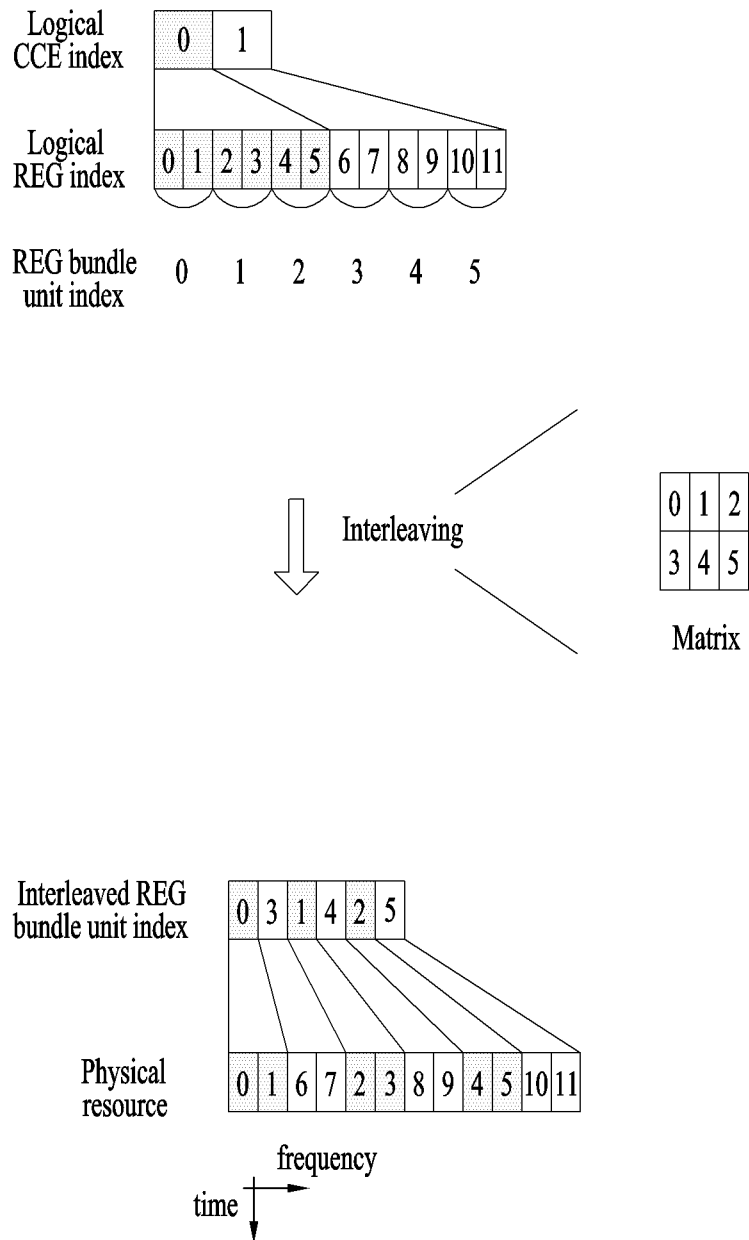


FIG. 18

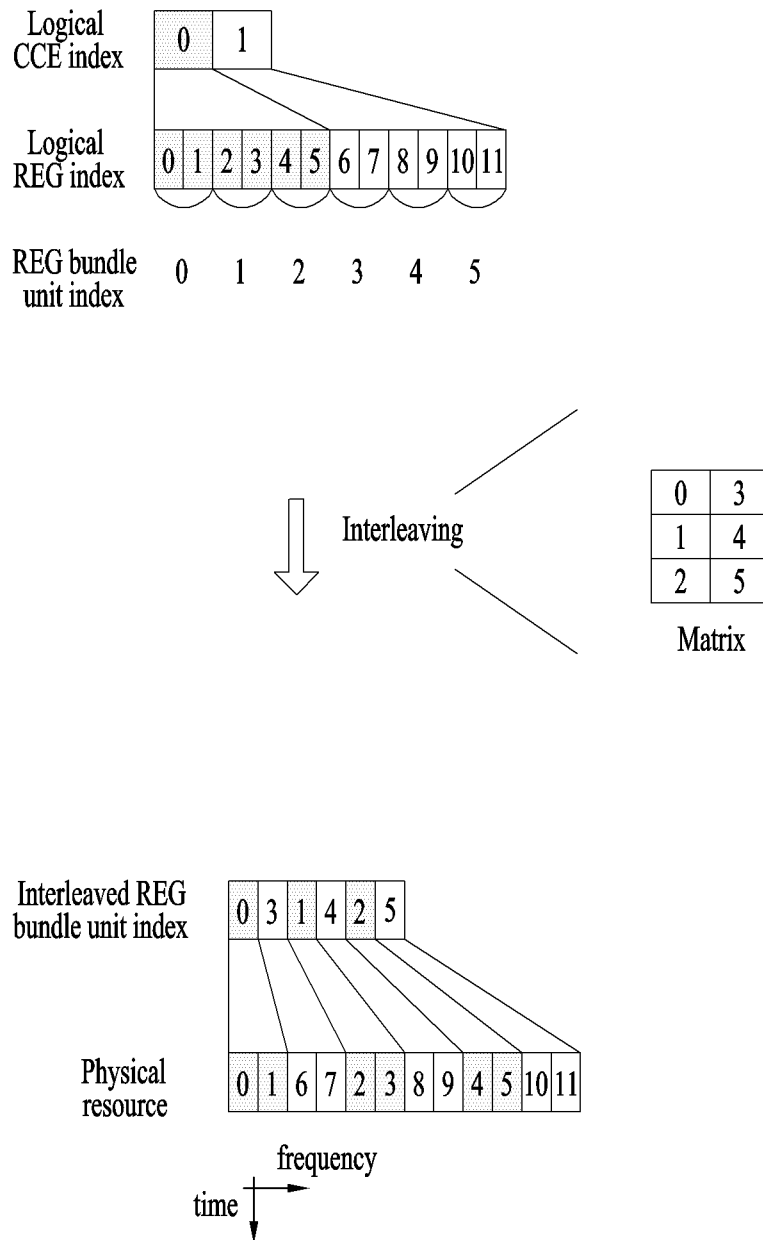


FIG. 19

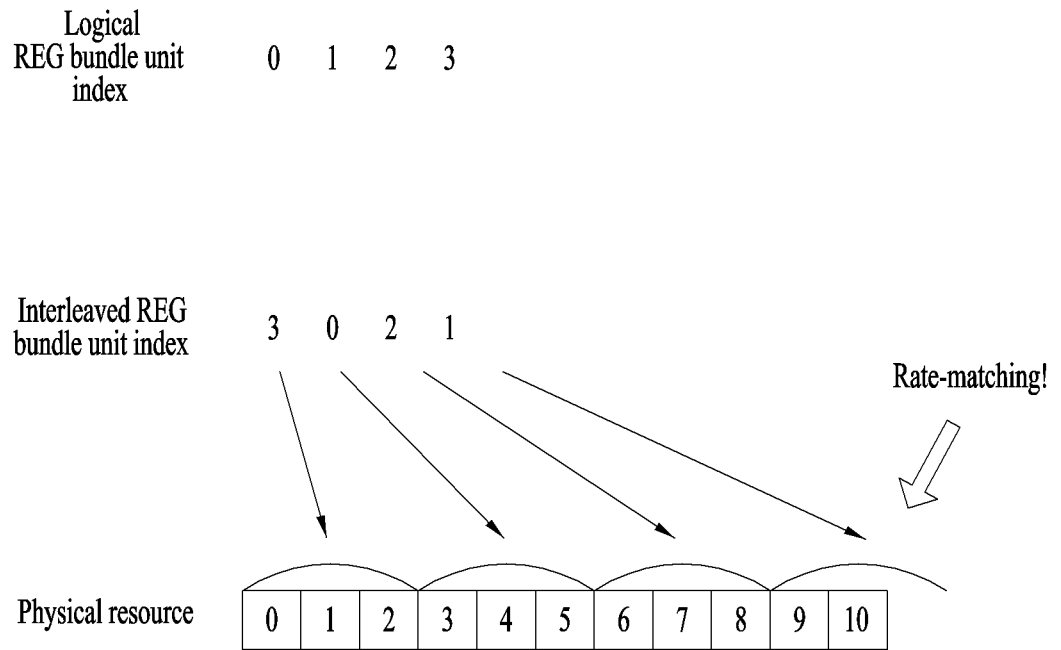


FIG. 20

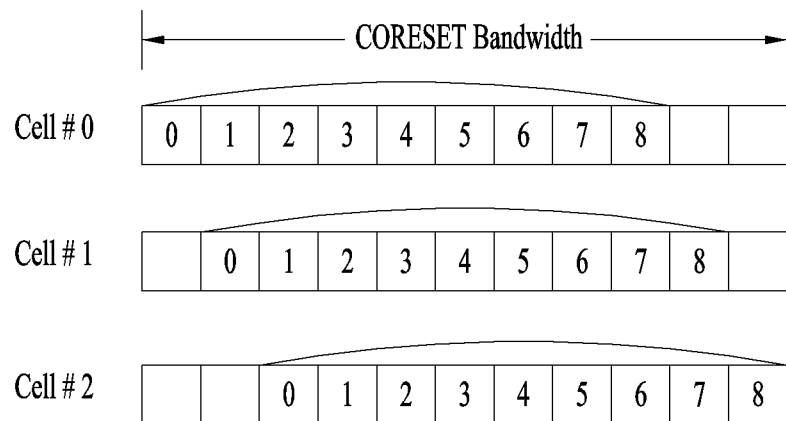


FIG. 21

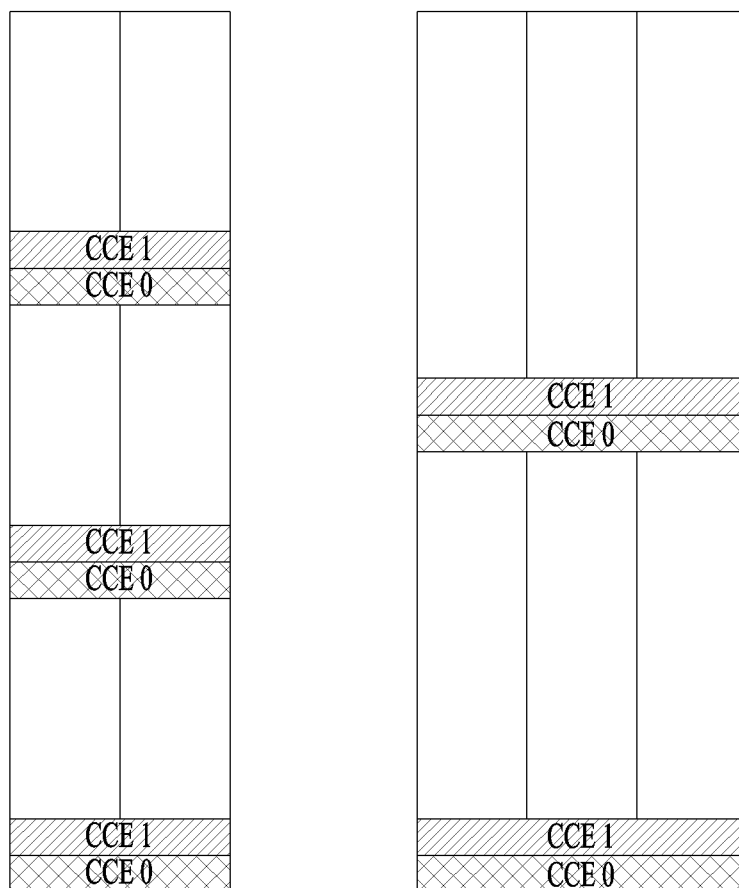


FIG. 22

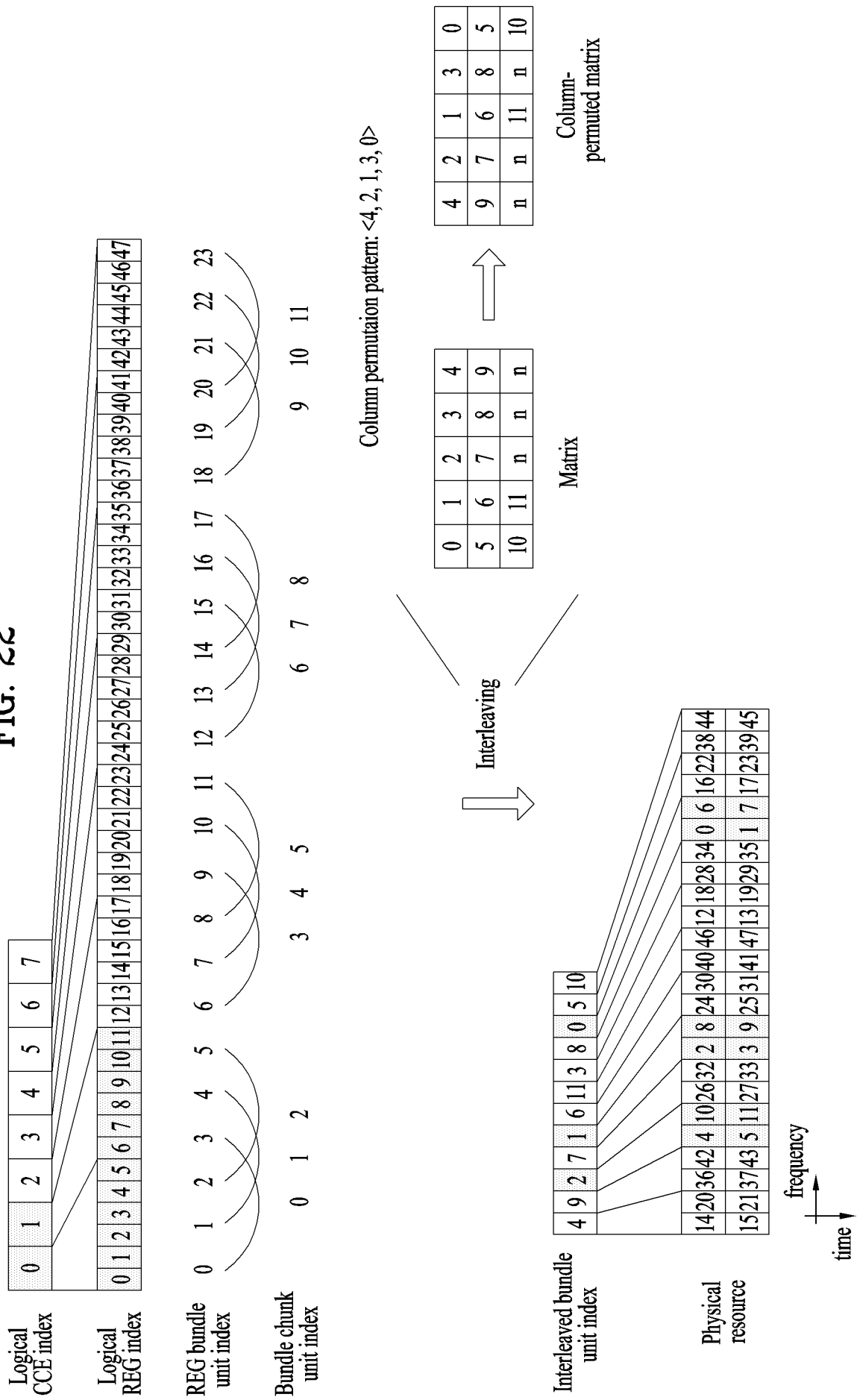


FIG. 23

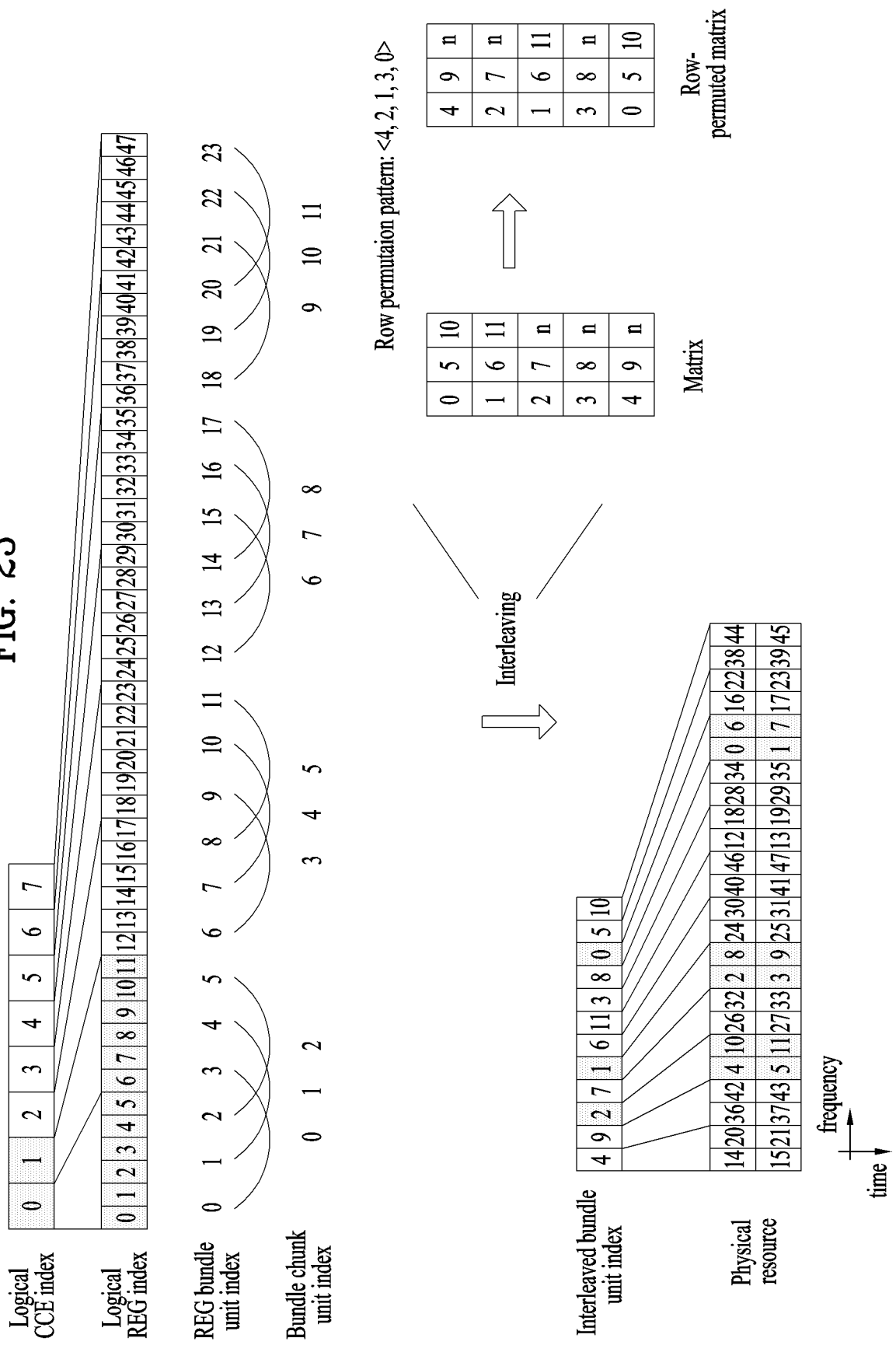


FIG. 24

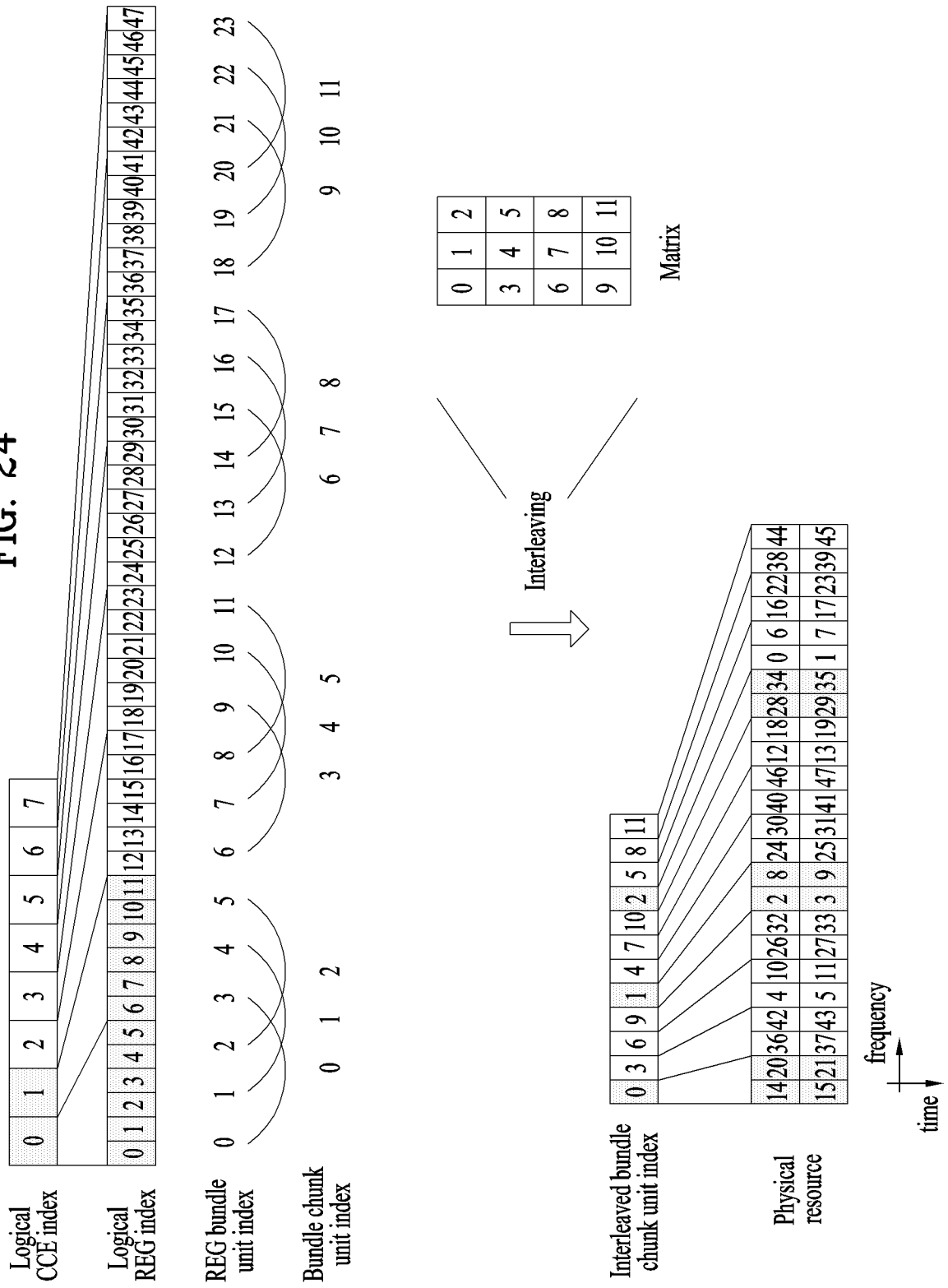


FIG. 25

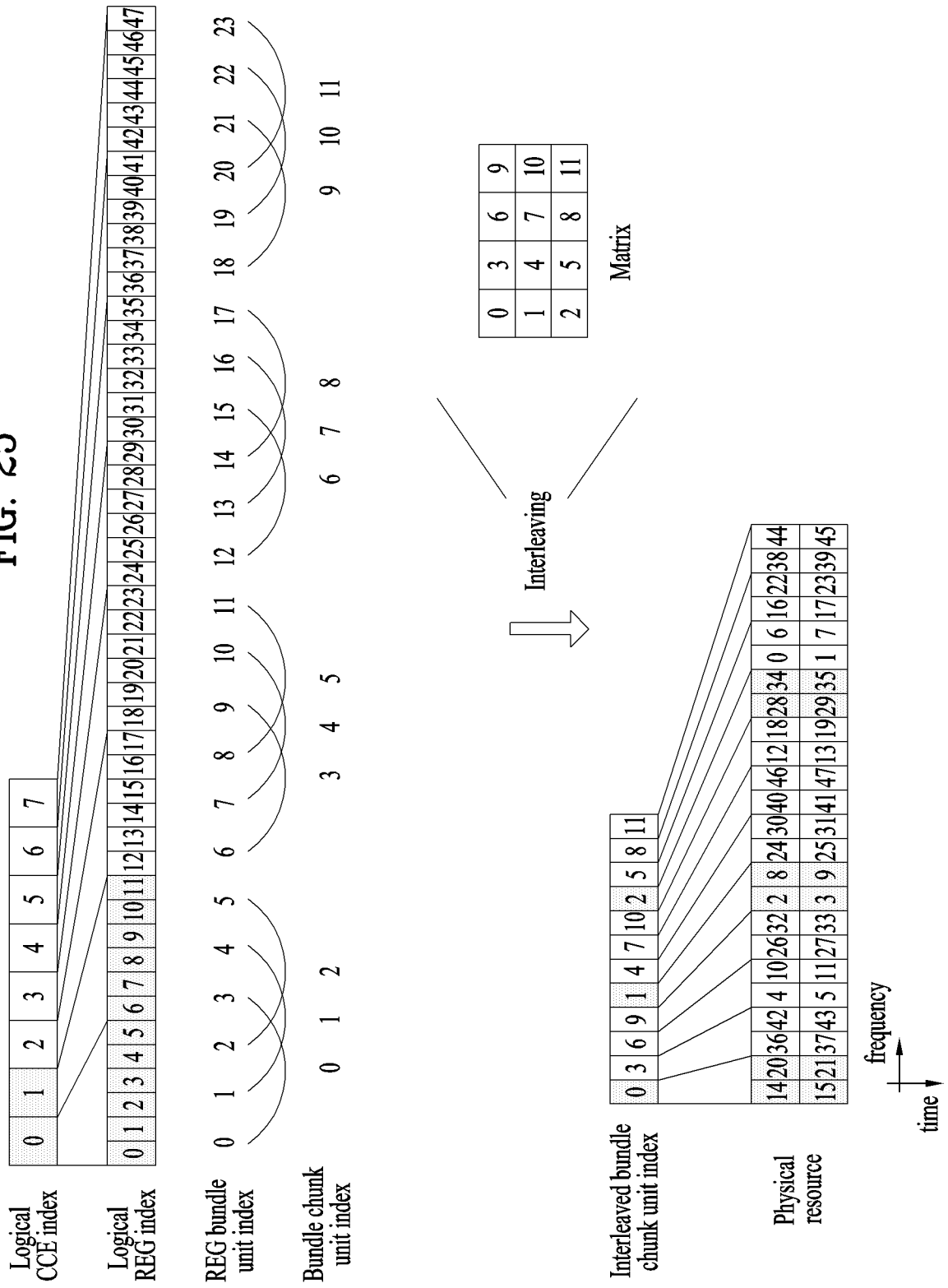


FIG. 26

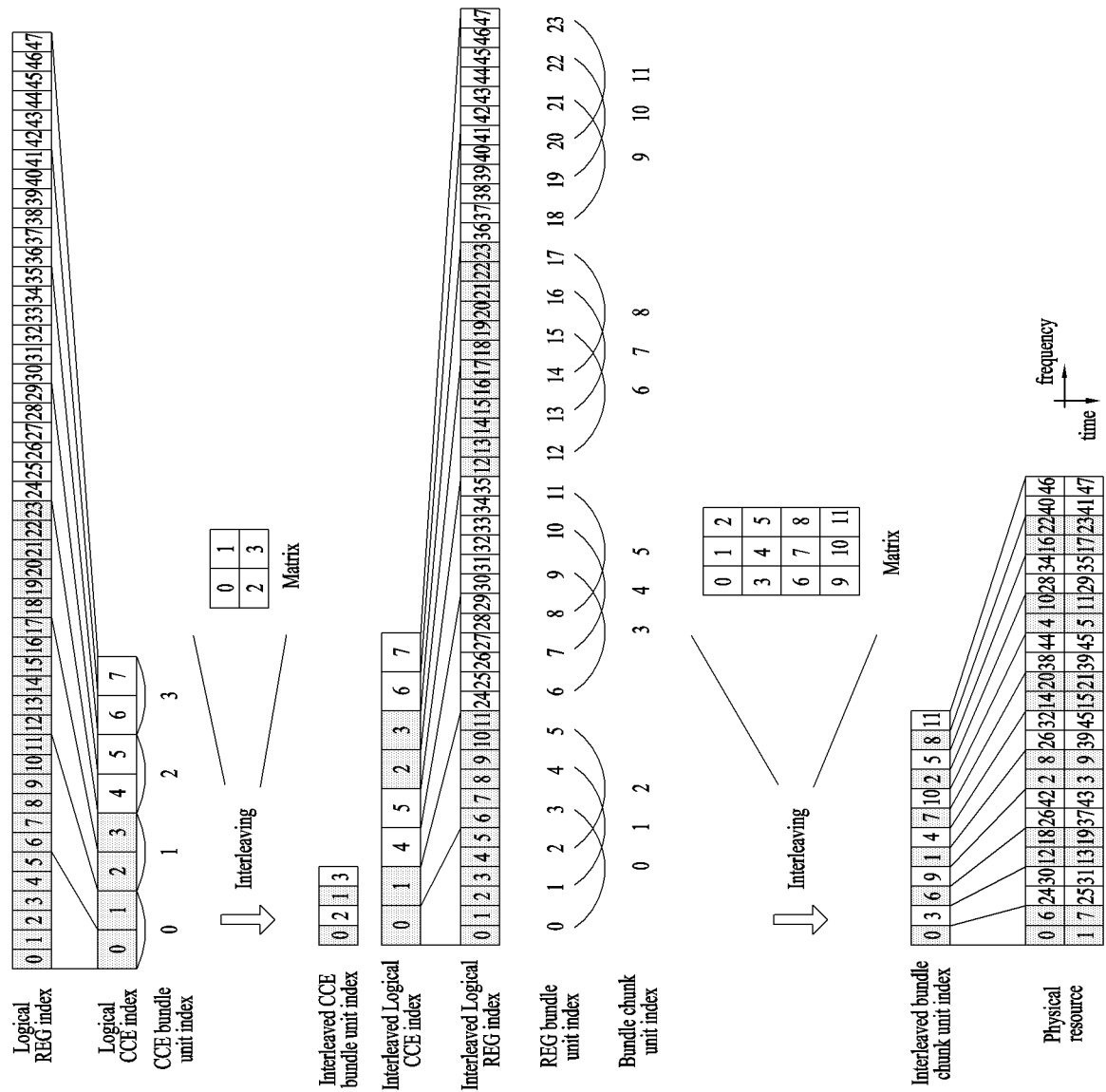


FIG. 27

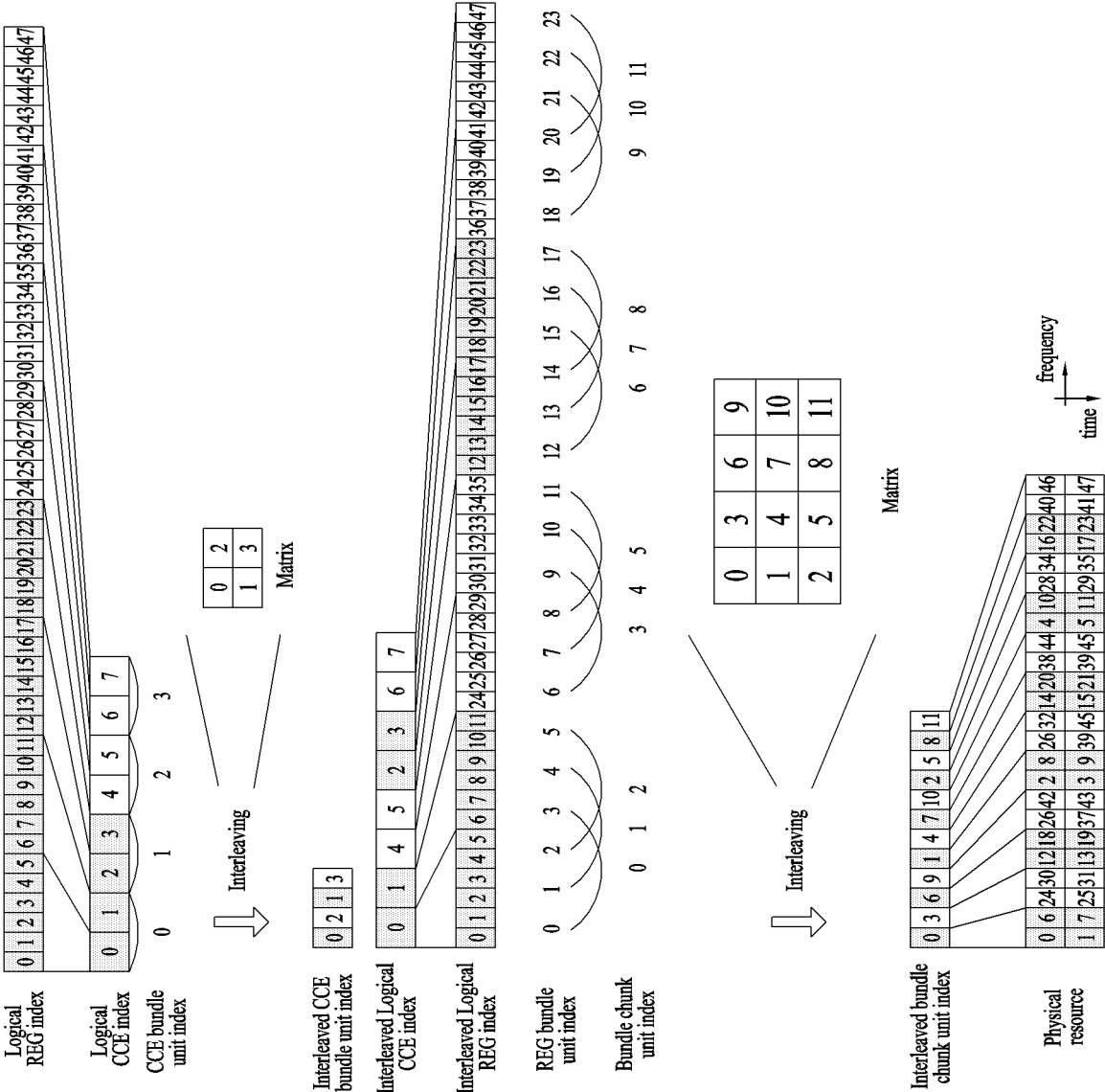


FIG. 28

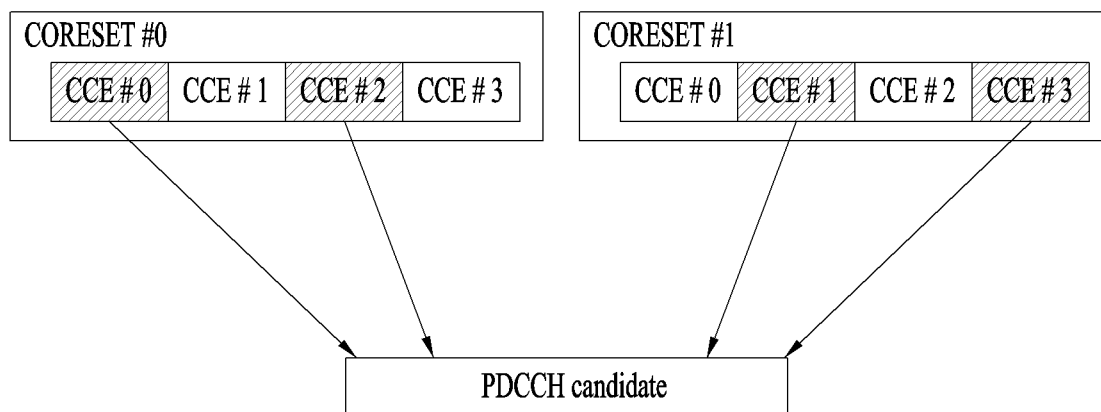


FIG. 29

