

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
4 September 2008 (04.09.2008)

PCT

(10) International Publication Number
WO 2008/106095 A1

(51) International Patent Classification:
G11C 29/00 (2006.01) *G06F 12/02* (2006.01)

(74) Agents: STEFFEY, Charles E. et al.; Schwegman, Lundberg & Woessner, P.A., P.O. Box 2938, Minneapolis, Minnesota 55402 (US).

(21) International Application Number:
PCT/US2008/002475

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(22) International Filing Date:
26 February 2008 (26.02.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/710,794 26 February 2007 (26.02.2007) US

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

(71) Applicant (for all designated States except US): MICRON TECHNOLOGY, INC. [US/US]; 8000 So. Federal Way, Boise, Idaho 83716-9632 (US).

(72) Inventor; and

(75) Inventor/Applicant (for US only): MURRAY, Michael [US/US]; 385 Foxborough Dr., Mountain View, California 94041 (US).

Published:
— with international search report

(54) Title: APPARATUS, METHOD, SYSTEM OF NAND DEFECT MANAGEMENT

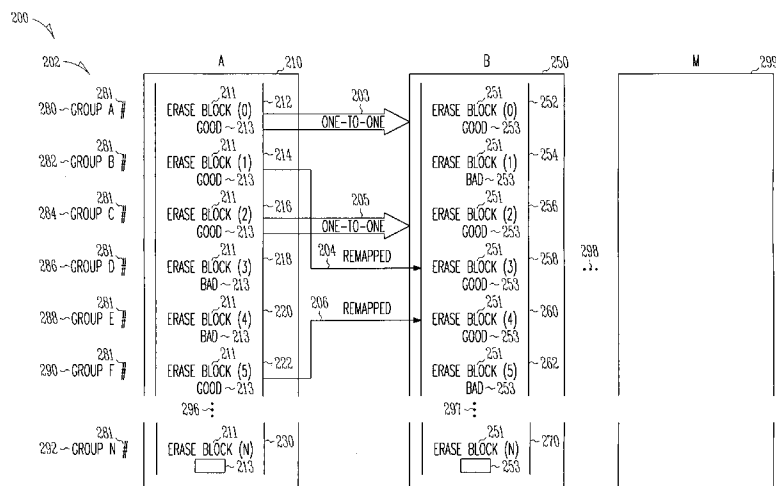


Fig. 2

(57) Abstract: Various embodiments comprise apparatus, methods, and systems that include an apparatus comprising a memory device configurable as a plurality of erase block groups including a base erase block group, wherein each of the plurality of erase block groups comprises a plurality of erase blocks each identified by a matching unique plurality of erase block numbers unique within the plurality of erase blocks and matching across the plurality of erase block groups; and a mapping table coupled to the plurality of erase block groups to store at least one group address number corresponding to one of the matching unique plurality of erase block numbers identifying a non-defective erase block in the base erase block group, and corresponding to several of the matching unique plurality of erase block numbers identifying a single non-defective erase block in each of the plurality of erase block groups other than the base erase block group.