CLAIMS

1. A method for forming a semiconductor structure, comprising:

providing a substrate, wherein the substrate comprises a first area and a second area arranged in sequence in a second direction, and the first area comprises active layers arranged at intervals in a third direction;

forming an initial gate structure located on a surface of each of the active layers in the first area;

etching the initial gate structures to form comb-shaped gate structures stacked in the third direction, wherein each of the comb-shaped gate structures at least comprises first gate structures arranged at intervals in a first direction, the first direction, the second direction and the third direction are perpendicular to one another, and the first direction and the second direction are parallel to a surface of the substrate; and

forming bit line structures extending in the third direction and capacitor structures extending in the second direction in the second area, wherein each of the bit line structures and each of the capacitor structures are respectively connected to one corresponding first gate structure.

2. The method of claim 1, wherein each of the comb-shaped gate structures further comprises a second gate structure, connected to all the first gate structures located on the same layer.

3. The method of claim 2, wherein a projection of the first gate structures on a surface of the substrate is a U shape.

4. The method of any one of claims 1 to 3, wherein the active layers are formed by:

providing a semiconductor substrate;

forming a stacked structure located in the first area and the second area on a surface of the semiconductor structure, wherein the stacked structure comprises first semiconductor layers and second semiconductor layers stacked alternately;

removing the first semiconductor layers in the first area to expose the second semiconductor layers in the first area;

performing thinning processing on the exposed second semiconductor layers to form initial active layers; and

processing the initial active layers to form the active layers.

5. The method of claim 4, wherein processing the initial active layers to form the active layers comprises:

forming a sacrificial layer and a first isolating layer on a surface of each of the initial active layers in sequence, wherein the first isolating layer fills between two adjacent ones of the sacrificial layers;

removing each of the initial active layers with a first length along the second direction to form a first space; and

removing each of the sacrificial layers with a second length along the second direction to expose part of each of the initial active layers and form a second space, wherein the second space comprises the first space, the second length is greater than the first length, and the exposed part of each of the initial active layers forms the active layer.

6. The method of claim 5, wherein forming the initial gate structure located on the surface of each of the active layers in the first area comprises:

forming a gate dielectric layer and a gate conductive layer on a surface of the active layer in sequence, wherein the gate conductive layer fills up the second space.

7. The method of claim 6, after forming the comb-shaped gate structures, the method for forming the semiconductor structure further comprises:

forming word line stairs stacked in sequence in the third direction,

wherein each layer of word lines in the word line stairs is electrically connected to the corresponding second gate structures, arranged in the first direction of each of the comb-shaped gate structures.

8. The method of claim 7, wherein the comb-shaped gate structures are formed by:

simultaneously removing part of the initial gate structures and part of stacked structure in the second area to form L-shaped grooves and isolating grooves arranged alternately in the first direction, and the remaining initial gate structures form the comb-shaped gate structures,

wherein a dimension of the isolating grooves in the second direction is greater than a dimension of the L-shaped grooves in the second direction, and each of the active layers is divided into a plurality of active structures arranged in the first direction by the isolating grooves.

9. The method of claim 8, wherein the stacked structures located on two sides in the first direction of the L-shaped groove have different sizes in the second direction; and forming bit line structures extending in the third direction and capacitor structures extending in the second direction in the second area comprises:

filling an isolating material in the L-shaped grooves and the isolating grooves to form a second isolating layer;

removing the second isolating layer and the first semiconductor layers located in the second area, wherein the remaining second semiconductor layers form first active pillars and second active pillars arranged alternately in the first direction, and each of the first active pillars comprises a first sub-pillar and a second sub-pillar;

forming each of the capacitor structures on a surface of the second sub-pillar; and

forming each of the bit line structures on a surface of the second active pillar.

10. The method of claim 9, further comprising:

forming a supporting layer on a surface of the first sub-pillar before forming the capacitor structures, wherein the supporting layer fills between two adjacent ones of the first sub-pillars.

11. The method of claim 10, wherein forming each of the capacitor structures on the surface of the second sub-pillar comprises:

forming a first electrode layer, a dielectric layer and a second electrode layer on the surface of the second sub-pillar in sequence to form the capacitor structure.

12. A semiconductor structure, least comprising:

a semiconductor substrate, the semiconductor substrate comprising a first area and a second area arranged in sequence in a second direction;

active structures located on a surface of the semiconductor substrate, the active structures being arranged in an array along a first direction and a third direction;

a comb-shaped gate structure, located on a surface of each of the active structures in the first area, and the comb-shaped gate structure at least comprising first gate structures arranged at intervals in the first direction;

bit line structures, extending in the third direction; and

capacitor structures, extending in the second direction,

wherein the bit line structures and the capacitor structures are located on the second area and are connected to the first gate structures, and the first direction, the second direction and the third direction are perpendicular to one another, and the first direction and the second direction are parallel to the surface of the semiconductor substrate.

13. The semiconductor structure of claim 12, wherein the comb-shaped gate structure further comprises: a second gate structure, connected to the first gate structures located on the same layer.

14. The semiconductor structure of claim 13, wherein each of the active structure comprises a first active pillar and a second active pillar located on the second area and arranged in the first direction, and a channel pillar located on the first area; and

the first active pillar and the second active pillar are connected to the channel pillar.

15. The semiconductor structure of claim 14, wherein the first gate structures cover a first surface and a second surface, in the third direction, of the channel pillar; and

each of the first gate structures comprises a gate dielectric layer and a gate conductive layer that are stacked.

16. The semiconductor structure of claim 15, wherein a projection of the channel pillar on the substrate of the semiconductor is a U shape.

17. The semiconductor structure of any one of claims 14 to 16, wherein each of the capacitor structures is formed on the first active pillar; and each of the bit line structures is formed on the second active pillar; and

a L-shaped groove is formed between the first active pillar and the second active pillar of a same active structure.

18. The semiconductor structure of claim 17, wherein an isolating groove is formed between two adjacent ones of the active structures in the first direction; and

a dimension of the isolating groove in the second direction is greater than a dimension of the L-shaped groove in the second direction.

19. The semiconductor structure of claim 13, further comprising: word line stairs, wherein

the word line stairs are stacked in sequence in the third direction; and each layer of word lines in the word line stairs are connected to a plurality of second gate structures, arranged in the first direction, of the comb-shaped gate structure.

20. A layout structure, comprising the semiconductor structures of any one of claims 12 to 19 arranged at intervals in the second direction, wherein

each of the semiconductor structure comprises memory cells arranged in an array in the first direction and the third direction, wherein each of the memory cells comprises a first gate structure and a capacitor structure; and

two adjacent ones of the memory cells are centrosymmetric in the second direction, and projection regions of the capacitor structures of the two adjacent memory cells in the second direction are at least partially overlapped in the first direction,

wherein two adjacent ones of the memory cells in the first direction have a same outlay or are axisymmetric.