What is claimed is:

1. An apparatus comprising:

first memory cells located in a first device level of a memory device;

second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.

2. The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and

a conductive material extending through the first and second memory elements.

10. The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory

element and the second additional conductive material are located in a second device level of the memory device.

11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

22. A method comprising:

forming a first non-volatile memory cell including a first memory element having a ring shape;

forming a non-volatile second memory cell including a second memory element having a ring shape; and

forming a conductive material extending through the first and second memory elements.

23. The method of claim 22, wherein forming the first memory cell comprises forming a first cavity in a first conductive material, wherein the first memory element is formed in the first cavity, wherein forming the second memory cell comprises forming a second cavity in a second conductive material, and wherein the second memory element is formed in the second cavity.

24. The method of claim 23, wherein the first cavity is substantially aligned over the second cavity.

25. The method of claim 22, further comprising:

forming a data line over a substrate, wherein the data line is located between the substrate and the first and second memory cells.

26. The method of claim 22, further comprising:

forming a data line over a substrate, wherein the first and second memory cells are located between the substrate and the data line.

27. A method comprising:

forming conductive material layers and dielectric material layers such that the conductive material layers are electrically isolated from each other by the dielectric material layers;

forming cavities in each of the conductive material layers; and

forming a memory element in each of the cavities.

28. The method of claim 27, wherein each of the conductive material layers is between two of the dielectric material layers and at least one of the conductive material layers is between two of the conductive material layers.

29. The method of claim 27, wherein the memory element comprises polysilicon.

30. The method of claim 27, wherein the memory element comprises a dielectric material.

31. The method of claim 27, wherein forming the cavities includes:

forming initial cavities in the conductive material layers; and

enlarging a size of the initial cavities to form the cavities in each of the conductive material layers.

32. The method of claim 31, further comprising:

forming openings through the conductive material layers and the dielectric material layers to form the initial cavities.

33. The method of claim 32, wherein second cavities are formed in each of the dielectric material layers when the openings are formed, and a size of the second cavities remains substantially unchanged when the size of the initial cavities is enlarged.

34. The method of claim 33, wherein each of the second cavities and each of the initial cavities has a substantially same diameter.

What is claimed is:

1. An apparatus comprising:

a substrate of a memory device;

a plurality of first memory cells located in a first device level of the memory device over the substrate;

a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and

data lines configured to be selectively coupled to a common source and the memory cells through conductive material.

2. The apparatus of claim 1, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction,

the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

5. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

6. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells

during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

8. An apparatus comprising:

a plurality of first memory cells located in a first device level of a memory device;

a plurality of second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;

a common source; and

data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

9. An apparatus comprising:

a substrate of a memory device;

a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

10. The apparatus of claim 9, wherein the first and second memory elements comprise polysilicon.

11. The apparatus of claim 9, wherein the first and second memory elements comprise a dielectric material.

12. The apparatus of claim 11, wherein the dielectric material comprises silicon nitride.

13. The apparatus of claim 9, further comprising dielectric material between the first and second conductive materials.

14. The apparatus of claim 9, further comprising:

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

15. An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element;

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric;

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.