CLAIMS

1. A semiconductor device comprising:

a first Vertical Field Effect Transistor (VFET), wherein the first VFET has a first source/drain epi, and wherein at least one liner is between the first source/drain epi and a first contact; and

and

a second VFET, wherein the second VFET has a second source/drain epi, and at least two liners are between the second source/drain epi and a second contact, and wherein the number of liners above the second VFET is greater than the number of liners above the first VFET; wherein

a top surface of the first source/drain epi is below a top surface of the second source/drain epi.

2. The structure of claim 1, wherein

the at least one liner between the first source/drain epi and the first contact comprises a single liner between the first source/drain epi and a first contact; and

the at least two liners between the second source/drain epi and the second contact comprise two liners are between the second source/drain epi and a second contact.

3. The structure of either of the preceding claims, wherein the first VFET comprises a pFET, and wherein the second VFET comprises an nFET.

4. The structure of any of the preceding claims, wherein the at least two liners comprise a liner for a pFET located above a titanium liner.

5. The structure of any of the preceding claims, wherein the at least one liner comprises a liner for a pFET.

6. The structure of any of claim 4 or claim 5 dependent upon claim 4, wherein the titanium liner comprises a p-type dopant.

7. A method of forming a semiconductor device comprising:

forming a first Vertical Field Effect Transistor (VFET) having a first source/drain epi, and a second VFET having a second source/drain epi;

performing a first ion implantation on the second source/drain epi forming an implanted source/drain epi;

performing a selective deposition of a first liner metal on the implanted source/drain epi;

performing a second ion implantation, wherein the second ion implantation is a blanket ion implantation, and wherein the first liner metal blocks implantation into the second source/drain epi.

8. The method of claim 7, wherein the first VFET comprises a pFET, and wherein the second VFET comprises an nFET.

9. The method of either of claims 7 or 8, wherein the first liner metal comprises titanium.

10. The method of any of claims 7 to 9, wherein a top surface of the first source/drain epi is below a top surface of the second source/drain epi.

11. The method of any of claims 7 to 10, wherein the first liner further comprises a p-type dopant.

12. The method of any of claims 7 to 11, further comprising:

forming a cap above first source/drain epi;

wherein the first ion implantation is a blanket ion implantation, and wherein the cap blocks implantation into the first source/drain epi.

13. The method of claim 12, wherein forming the cap comprises:

depositing a dielectric above the first source/drain epi; and

planarizing the dielectric to for the cap, wherein a top surface of the cap is substantially coplanar to a top surface of an ILD surrounding the first FET and the second FET.

14. The method of either of claims 12 or 13, wherein forming the cap is performed prior to forming the second source/drain epi.

15. The method of any of claims 12 to 14, wherein a top surface of the cap is substantially coplanar to a top surface of the second source/drain epi.