CLOCK SKEW MINIMIZATION SYSTEM AND METHOD FOR INTEGRATED CIRCUITS

ABSTRACT

A precise and highly controllable clock-distribution network is provided on one active substrate to distribute clock signals with minimal skew to another active substrate by connecting the substrates together face-to-face using flip-chip technology. Since the clock-distribution substrate is sparse, "quiet busses" are provided on the sparse substrate to facilitate the high-speed transfer of data over relatively long distances. Low-power devices (e.g., DRAM) can be provided on one substrate for use by higher-power logic (e.g., a processor) on another substrate with minimal interconnection distance.

Fig. 6

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