# NEAR CHIP SIZE SEMICONDUCTOR PACKAGE

## BACKGROUND OF THE INVENTION

### FIELD OF THE INVENTION

The present invention relates to packaged semiconductors, semiconductor packages, leadframe assemblies therefor, and more particularly, but not by way of limitation, to semiconductor packages that can accept semiconductor chips of various sizes without having to change the footprint of the semiconductor package.

### HISTORY OF RELATED ART

It is conventional in the electronic industry to encapsulate one or more semiconductor devices, such as integrated circuit dies, or chips, in a semiconductor package. These plastic packages protect a chip from environmental hazards, and provide a method of and apparatus for electrically and mechanically attaching the chip to an intended device. Recently, such semiconductor packages have included metal leadframes for supporting an integrated circuit chip which is bonded to a chip paddle region formed centrally therein. Bond wires which electrically connect pads on the integrated circuit chip to individual leads of the leadframe are then incorporated. A hard plastic encapsulating material, or encapsulant, which covers the bond wire, the integrated circuit chip and other components, forms the exterior of the package.

This Sheet Has Been Replaced

A primary focus in this design is to provide the chip with adequate protection from the external environment in a reliable and effective manner.

As set forth above, the semiconductor package therein described incorporates a leadframe as the central supporting structure of such a package. A portion of the leadframe completely surrounded by the plastic encapsulant is internal to the package. Portions of the leadframe extend internally from the package and are then used to connect the package externally. More information relative to leadframe technology may be found in Chapter 8 of the book Micro Electronics Packaging Handbook, (1989), edited by R. Tummala and E. Rymaszewski, incorporated by reference herein. This book is published by Van Nostrand Reinhold, 115 Fifth Avenue, New York, New York.

Once the integrated circuit chips have been produced and encapsulated in semiconductor packages described above, they may be used in a wide variety of electronic appliances. The variety of electronic devices utilizing semiconductor packages has grown dramatically in recent years. These devices include cellular phones, portable computers, etc. Each of these devices typically include a printed circuit board on which a significant number of such semiconductor packages are secured to provide multiple electronic functions. These electronic appliances are typically manufactured in reduced sizes and at

This Sheet Has Been Replaced



reduced costs, which results in increased consumer demand. Accordingly, not only are semiconductor chips highly integrated, but also semiconductor packages are highly miniaturized with an increased level of package mounting density.

According to such miniaturization tendencies, semiconductor packages, which transmit electrical signals from semiconductor chips to printed circuit boards and support the semiconductor chips on the printed circuit boards, have been designed to have a small size. By way of example only, such semiconductor packages may have a size on the order of 1x1mm to 10x10 mm. Examples of such semiconductor packages are referred to as MLF (micro leadframe) type semiconductor packages and MLP (micro leadframe package) type semiconductor packages. Both MLF type semiconductor packages and MLP type semiconductor packages are generally manufactured in the same manner.

One specific problem with the prior art is that chip sizes differ and/or increases due to different computing requirements of different products. With existing packaging design, fitting these larger chips means the packages must be made bigger. Bigger packages have larger footprint (the locations where the leads physically and electrically connect to printed circuit boards). The larger

This Sheet Has Been Replaced



footprint forces the printed circuit boards to be redesigned for proper electrical connection. This redesign takes time and money. Thus, a semiconductor package that can fit circuit chips of different sizes without changing the semiconductor package=s footprint is needed.

## SUMMARY OF THE INVENTION

The present invention relates to semiconductor packages that can accept semiconductor chips of various sizes without having to change the footprint of the carrier package. More particularly, one aspect of the present invention comprises a leadframe, a semiconductor chip attached to the leadframe, electrical connectors electrically connecting the semiconductor to the leadframe, and a sealing material. The leadframe has a plurality of leads, with each one of the plurality of leads having an upper side, a lower exposed side, and a laterally exposed side. The upper side of each one of the plurality of leads define a generally co-planar surface for supporting the semiconductor chip. Because the semiconductor chip rests on the co-planar and unobstructed surface defined by the upper side of the leads, semiconductors of different sizes can be attached to the semiconductor package without having to change the footprint of the semiconductor package. Finally, after sealing material

This Sheet Has Been Replaced



encapsulates the components of the semiconductor package in a spacial relationship, the lower exposed side and the lateral exposed side of the plurality of leads are exposed to the outside surface of the semiconductor package.

Another aspect of the present invention is a leadframe that comprises a plurality of leads and a tie bar connecting to the plurality of leads. Each one of the plurality of leads has an upper side and a lower exposed side, with the upper side of each one of the plurality of leads forming a generally co-planar surface with the upper side of at least some of the leads. Further, when the tie bars are trimmed off the leadframe, they leave a lateral surface of the plurality of leads exposed to the lateral side of the semiconductor package.

## BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the method and apparatus of the present invention may be had by reference to the following detailed description when taken in conjunction with the accompanying drawings wherein:

FIGURE 1 is a perspective cut-away view of a prior art semiconductor carrier package;

FIGURE 2 is a perspective cut-away view of another prior art semiconductor carrier package;

This Sheet Has Been Replaced



FIGURE 3 is a perspective cut-away view of a first embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 4 is a perspective view of a leadframe of a first embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 5 is a perspective cut-away view of a second embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 6 is a perspective view of a leadframe of a second embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 7 is a perspective cut-away view of a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention;

FIGURE 8 is a perspective cut-away view of a fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention; and

This Sheet Has Been Replaced



FIGURE 9 is a perspective view of a leadframe of a fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

This Sheet Has Been Replaced



Referring first to FIGURE 1, there is shown a perspective cut-away view of a first prior art semiconductor package 50. Semiconductor package 50 is described below to provide a better context for understanding the semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 50 includes a leadframe 51 (partially shown in Figure 1) having a paddle 52 and a plurality of leads 53. Leads 53 are located on opposing sides of semiconductor package 50, are generally AZ@ shaped, and are spaced parallel and apart from each other. Paddle 52 rests below a horizontal plane defined by the top surface of the top side 57 of leads 53. A semiconductor chip 54 is attached to paddle 52 through any method known in the art of semiconductor chip packaging, such as by using the eutectic method or by epoxy adhesive. (Attaching a semiconductor chip to a paddle by the eutectic method or by using an epoxy adhesive will be explained in further detail below, in the discussion of embodiments of the semiconductor packages constructed in accordance with the principles of the present invention.) At least a part of semiconductor chip 54 rests below a plane defined by the top side 57 of leads 53. A plurality of connecting pads 56 are located on semiconductor chip 54. A plurality of wires 55 electrically connect semiconductor chip 54 (through connecting pads 54) to leads 53. Bottom side

This Sheet Has Been Replaced



58 of leads 53 physically and electrically connect the semiconductor package 50 to a printed circuit board (not shown). The above components are affixed in a spacial relationship and are protected from the outside environment by sealing material 59.

If another semiconductor chip that is larger than semiconductor chip 54 is placed in semiconductor package 50, that larger semiconductor chip will touch and be obstructed by leads 53 because a part of the larger semiconductor chip rests below the plane defined by the top side 57 of leads 53. In order to fit this larger semiconductor chip into semiconductor package 50, leads 53 of semiconductor package 50 must be moved farther apart from the lateral centerline of semiconductor package 50, thus changing the footprint of semiconductor package 50. A change in semiconductor package 50's footprint forces a redesign of the printed circuit board to be physically and electrically attached to semiconductor package 50. The redesign is necessary because the physical directions of the electrical contact points of the printed circuit board no longer fits the new larger semiconductor package 50. Redesigning the printed circuit board is undesirable because it incurs additional monetary costs and time delays.

This Sheet Has Been Replaced



Referring now to FIGURE 2, there is shown a perspective cut-away view of a second prior art semiconductor package 60. Again, semiconductor package 60 is described below to provide a better context for understanding the semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 60 has a leadframe 61 (shown partially) having a plurality of leads 62 lined up lengthwise along the two longer sides of semiconductor package 60. Leads 62 are spaced parallel and apart from each other. Each lead in the plurality of leads 62 has an upper part 63 and a lower part 64. A semiconductor chip 65 is placed on top of lower part 64 of leads 62. A plurality of connecting pads 67 are located on semiconductor chip 65 for connection to a plurality of wires 66. Wires 66 electrically connect semiconductor chip 65 to leads 62.

This Sheet Has Been Replaced



If another semiconductor chip that is larger than semiconductor chip 65 is placed in semiconductor package 60, that larger semiconductor chip will touch and be obstructed by leads 62. Thus, in order to fit a larger semiconductor chip into semiconductor package 60, leads 62 must be moved outward. Moving leads 62 outward changes the footprint of semiconductor package 60, thereby forcing a redesign of the printed circuit board. Again, redesigning the printed circuit board is underdesirable because the redesigning process incurs additional monetary costs and time delays.

Referring now to FIGURE 3, there is shown a perspective cut-away view of semiconductor package 70 that is a first embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 70 generally consists of a leadframe 71 (FIGURE 4), a semiconductor chip 74, a plurality of wires 75, and sealing material 76. A more detailed description of semiconductor package 70 appears below.

Referring now to FIGURE 4, there is shown a detailed perspective view of a leadframe 71 of the first embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Leadframe 71 is made of an electrically conductive material such as, for example, copper. Leadframe 71 has a paddle 72 surrounded by a plurality of

This Sheet Has Been Replaced



leads 73. Leads 73 and paddle 72 are connected to each other via a tie bar 71a located on the outer perimeter of leadframe 71. Leads 73 do not touch paddle 72 and are placed parallel and apart from each other. Each one of the leads 73 has a notch 77 at the end near paddle 72. Notch 77 increases the locking strength between leads 73 and sealing material 76 so that leads 73 are less likely to become detached from semiconductor package 70. The bottom of each one of leads 73, after packaging, is exposed to the outside of semiconductor package 70 for electrically and physically connecting semiconductor package 70 to a printed circuit board. To minimize corrosion, the bottom of leads 73 are coated or electroplated with tin, gold, or other comparable corrosion-minimizing material. Paddle 72 is attached to leadframe 71 through a plurality of connectors 78. The top side of leads 73 and paddle 72 rest in the same horizontal plane to allow semiconductor chip 74 to be placed on top of both paddle 72 and a portion of leads 73. The bottom of paddle 72 may or may not be exposed to the outer bottom surface of semiconductor 70.

Referring back to FIGURE 3, there is shown a perspective cut-away view of semiconductor package 70. Having described leadframe 71 in detail above, additional components of semiconductor package 70 will now be discussed. Semiconductor chip 74 is attached to the top of both paddle 72 and

This Sheet Has Been Replaced



leads 73. Semiconductor chip 74 is attached to paddle 72 and leads 73 by using the eutectic method (discussed below), an epoxy adhesive (discussed below), or any other adhesive means or technique known in the art of semiconductor chip attachment. Because the top surface of paddle 72 and leads 73 rest in the same horizontal plane, the size of semiconductor chip 74 can vary so that semiconductor chip 74 may rest only on paddle 72 or extend over and rest on top of leads 73. This configuration of paddle 72 in relation to leads 73 allows semiconductor chips of different sizes to fit in semiconductor package 70 without changing the footprint of semiconductor package 70.

The eutectic semiconductor chip attachment method mentioned above will now be described in more detail. The eutectic method is named for the phenomenon that takes place when two materials melt together (alloy) at a much lower temperature than either one of the materials separately. For semiconductor chip attachment, the eutectic materials are gold and silicon. The top side of paddle 72 is first deposited or plated with a layer of gold. Then, both the gold and the bottom side of semiconductor chip 74 (made of silicon) are heated until the gold and the silicon each forms a generally thin liquid layer. The semiconductor chip 74 is then placed on the paddle 72, and semiconductor chip 74 and paddle 72 are forced together through an abrasive

This Sheet Has Been Replaced



action called Ascrubbing.@ Scrubbing, in the presence of heat, forms the gold-silicon eutectic layer. Finally, paddle 72 and semiconductor chip 74 are cooled. The eutectic semiconductor chip attachment method described above can be performed manually or by an automated machine.

Alternatively, semiconductor chip 74 can be attached to paddle 72 by using an epoxy adhesive. The epoxy adhesive can, but does not necessarily have to be, silver filled for used with copper lead flames or silver filled polyamide for alloy 22 metal frames. The epoxy adhesive semiconductor chip attachment process starts by depositing the epoxy adhesive on paddle 72 using, for example, a needle or through screen printing. The semiconductor chip 74, held by a vacuum wand, is placed over the paddle and then forced into the epoxy adhesive so a thin layer of epoxy adhesive is formed between the semiconductor chip 74 and paddle 72. Finally, the semiconductor chip 74 and the leadframe 71 are cured in an oven to set the epoxy bond.

Referring still to FIGURE 3, semiconductor package 70 will now continue to be described. A plurality of connecting pads 79 are located on semiconductor chip 74 for electrical connection. A plurality of wires 75 electrically connect each connecting pad of connecting pads 79 to each lead of leads 73. (Wire bonding methods will be discussed in more detail below.)

This Sheet Has Been Replaced



Wires 75 can be made of any electrically conductive material such as, for example, gold, silver, aluminum, or an alloy thereof. Both the lateral side and the bottom side of each one the of leads 73 exposed to the outside of semiconductor package 70 are coated or electroplated with corrosion-minimizing material such as, for example, tin or gold. All the components described above are encased (with the exception of the bottom and one lateral side of each lead of leads 73) in sealing material 76. Sealing material 76 may be epoxy resin or other materials or combination of materials. Semiconductor package 70 is electrically and physically attached to a printed circuit board (not shown) through any method known in the art of semiconductor package attachment such as, for example, soldering leads 73 to the printed circuit board.

As mentioned above, two methods by which wires 75 can be attached (or Abonded@) to connecting pads 79 and leads 73 are described below. The two wire bonding techniques are gold wire bonding and aluminum wire bonding. Note these methods are presented for illustrative purposes only and should not limit the precise packaging method to be used with packaging the semiconductor package constructed in accordance with the principles of the present invention. The bonding methods described below can be performed either manually or mechanically. While there is one general aluminum bonding

This Sheet Has Been Replaced



method, there are two general gold bonding techniques: the thermocompression technique and the thermosonic technique. Both techniques will be described below.

The thermocompression gold wire bonding technique will now be described. Thermocompression bonding starts with feeding the wire out of a thin tube called a Acapillary.@ The capillary is placed over a connecting pad of connecting pads 79 and an electrical spark or small flame melts the tip of the gold wire into a ball. The capillary then moves downward and attaches the melted ball to the connecting pad. After this connection is made, the capillary feeds out more wire as the capillary travels to and is positioned over one lead of leads 73. The capillary then travels downwards and is positioned directly on top of the lead. The wire is then pressed onto the lead while a spark or flame melts the wire simultaneously, bonding the wire and forming another melted ball for attaching to the next connecting pad.

The thermosonic gold wire bonding technique is similar to the thermocompression bonding technique described above, except the thermosonic technique can take place at a lower temperature. Rather than melting the gold wire like the thermocompression technique, a pulse of ultrasonic energy is sent

This Sheet Has Been Replaced

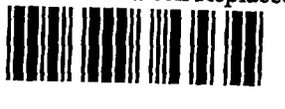


through the capillary and into the wire, thus providing the heat and friction to form the bond.

Wires 75 can also be bonded to the connecting pads 79 and the leads 73 using aluminum wire bonding techniques. Aluminum bonding is generally similar to gold wire bonding, except it can take place at a lower temperature. To bond an aluminum wire to a connecting pad and a lead, the capillary is first positioned over a connecting pad. A wedge then forces the wire onto the connection pad while a pulse of ultrasonic energy is sent down to the wedge, bonding the aluminum wire to the connecting pad. The capillary then feeds out more wire as it travels to and is positioned directly on top of the lead. The wedge then forces the wire onto the lead and a pulse of ultrasonic energy bonds the aluminum wire to the lead. The wire is cut, and the process is repeated.

Referring now to FIGURE 5, there is shown semiconductor package 80, which is a second embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 80 has a plurality of leads 81, a semiconductor chip 82, a plurality of wires 83, and sealing material 84. Semiconductor package 80 differs from semiconductor package 70 in that semiconductor package 80 lacks a paddle. Semiconductor package 80 will be discussed in more detail below.

This Sheet Has Been Replaced



Referring to FIGURE 6, there is shown a perspective view of leadframe 85 of the second embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Leadframe 85 will now be described in further detail. Leads 81 are connected to each other via a tie bar 85a located on the outer perimeter of leadframe 85. Leadframe 85 and leads 81 are made of an electrically conductive material such as, for example, copper. Leads 81 are placed parallel and apart from each other and on opposite sides of leadframe 85. Each one of leads 81 has an inwardly extending member 86 located generally perpendicularly to an upwardly extending member 87. Inwardly extending member 86 extends towards the middle of semiconductor package 80 to support semiconductor chip 82 (shown in FIGURE 5).

Referring back to FIGURE 5, additional components of semiconductor package 80 will now be described. Leads 81 are shown after the trimming process. (The trimming process will be described in more detail later below.) Semiconductor chip 82 is attached to leads 81 by using any semiconductor chip attaching processing known in the art of semiconductor packaging such as, for example, the eutectic method or with epoxy adhesives. Semiconductor chip 82 can be of different sizes because inwardly extending member 86 of each one of leads 81 has a long upper surface for attaching semiconductor chips of various

This Sheet Has Been Replaced



sizes without having to move the location of leads 81 resulting in a change to the footprint of semiconductor package 80. A plurality of connecting pads 88 are located on top of semiconductor chip 82. A plurality of wires 83 electrically connect semiconductor chip 82 (via connecting pads 88) to leads 81. Wires 83 are made of an electrically conductive material such as, for example, gold, silver, or aluminum. Sealing material 84 secures leads 81, semiconductor chip 82, and the plurality of wires 83 in a spacial relationship. The bottom and one side of each one of the leads 81 rest flush with the outer surfaces of semiconductor package 80 and are exposed to the outside of semiconductor package 80 for electrical and physical connection to a printed circuit board. The electrical and physical connection may, but do not necessarily have to be, achieved through soldering semiconductor package 80 to the printed circuit board (not shown). The exposed surfaces of leads 81 are electroplated with corrosion-minimizing material such as, for example, tin or gold.

Referring now to FIGURE 7, there is shown a perspective cut-away view of semiconductor package 90, which is a third embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 90 is similar in construction (including the construction

This Sheet Has Been Replaced



of the leadframe) to semiconductor package 80. Semiconductor package 90 differs from semiconductor package 80 in that semiconductor chip 91 is flipped upside down and then attached to the plurality of leads 92 via a plurality of solder balls 93. Solder balls 93 are made of an electrically conductive material and allow a direct physical and electrical connection between semiconductor chip 91 and leads 92. Using solder balls 93 to attach semiconductor chip 91 to lead 92 bypasses the use of wires to electrically connect semiconductor chip 91 to leads 92. The advantage of using solder balls 93 instead of wires to connect semiconductor chip 91 to leads 92 is that using solder balls 93 minimizes the chance of wires breaking or becoming disconnected and causing a failure of the entire semiconductor package 90. The semiconductor chip 91 and the plurality of leads 92 are secured in a spacial relationship and are protected from the outside environment by sealing material 94. Sealing material 94 may be, for example, epoxy resin. The bottom and one side of each one of the plurality of leads 92 are exposed to the outside of sealing material 94 and rest flush with the bottom and the sides of semiconductor package 90. The exposed bottom and one side of each one of the plurality of leads 92 are electroplated with corrosion-minimizing material such as, for example, tin or gold.

This Sheet Has Been Replaced



Referring now to FIGURE 8, there is shown a perspective cut-away view of semiconductor package 100, which is a fourth embodiment of a semiconductor package constructed in accordance with the principles of the present invention. Semiconductor package 100 generally has a plurality of leads 101, a semiconductor chip 102, a plurality of wires 103, and sealing material 104. Semiconductor package 100 will be described in more detail below.

Referring now to FIGURE 9, there is shown a perspective view of a leadframe 105 of semiconductor package 100 prior to the packaging process. Leadframe 105 will now be described first in further detail. Leadframe 105 has a plurality of leads 101 placed generally parallel and apart from each other and along the length of semiconductor package 100. Leads 101 are connected to each other via a tie bar 105a located on the outer perimeter of leadframe 105. An equal number of leads 101 may, but does not necessarily have to, rest on each side of semiconductor package 100. Each lead of leads 101 has a notch 106 on the underside of each lead. Notch 106 allows for better locking strength between leads 101 and sealing material 104. Better locking strength minimizes the chance of a lead of leads 101 from becoming detached from semiconductor package 100. Each one of the leads 101 also has an inwardly extending

This Sheet Has Been Replaced



member 107 extending towards the centerline of semiconductor package 100. The top of all leads 101 rest in one horizontal plane so that semiconductor chip 102 of various sizes can be supported by leads 101.

Referring back to FIGURE 8, there is shown a perspective cut-away view of semiconductor package 100, after the packaging process has been completed, with the plurality of leads 101 trimmed to their desired lengths. Additional components of semiconductor package 100 will now be described below. The bottom of semiconductor chip 102 is attached to leads 101 through any method known in the art of semiconductor chip attachment such as, for example, the eutectic method or with epoxy adhesives. Semiconductor chip 102 can be of any size because the top of leads 101, which provide the supporting surface for semiconductor chip 102, rest in one horizontal plane. A plurality of connecting pads 108 are located on top of semiconductor chip 102. A plurality of wires 103 electrically connect semiconductor chip 102, through connecting pads 108, to leads 101. Semiconductor chip 102, leadframe 105, and wires 103 are secured in a spacial relationship using sealing material 104. Sealing material 104 can be, for example, epoxy resin. Sealing material 104 also protects semiconductor chip 102 from damage. The bottom and one side of each one of the plurality of leads 101 rest flush with and are exposed to the

This Sheet Has Been Replaced



bottom and side surfaces of semiconductor package 100 without being encased in sealing material 104. The bottom and one side of each one of the plurality of leads 101 are protected from corrosion by being electroplated with a corrosion-minimizing material such as, for example, tin or gold.

The following applications are all being filed on the same date as the present application and all are incorporated by reference as if wholly rewritten entirely herein, including any additional matter incorporated by reference therein:

| Attorney Docket No. | Title of Application | First Named Inventor |
|---|---|---|
| 45475-00015 | Semiconductor Package Having Increased Solder Joint Strength | Kil Chin Lee |
| 45475-00016 | Clamp and Heat Block Assembly for Wire Bonding a Semiconductor Package Assembly | Young Suk Chung |
| 45475-00019 | Semiconductor Package | Sean Timothy Crowley |
| 45475-00020 | Stackable Semiconductor Package and Method for Manufacturing Same | Sean Timothy Crowley |
| 45475-00021 | Stackable Semiconductor Package and Method for Manufacturing Same | Jun Young Yang |

This Sheet Has Been Replaced



| | | |
|---|---|---|
| 45475-00024 | Method of and Apparatus for Manufacturing Semiconductor Packages | Hyung Ju Lee |
| 45475-00028 | Semiconductor Package Having Improved Adhesiveness and Ground Bonding | Sung Sik Jang |
| 45475-00029 | Semiconductor Package Leadframe Assembly and Method of Manufacture | Young Suk Chung |

Although a preferred embodiment of the method and apparatus of the present invention has been illustrated in the accompanying drawings and described in the foregoing detailed description, it will be understood that the invention is not limited to the embodiment disclosed, but is capable of numerous rearrangements, modifications, and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.

This Sheet Has Been Replaced



WHAT IS CLAIMED IS:

1. A packaged semiconductor, comprising:

a leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side, a lower exposed side, and a laterally exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least two groups of a plurality of leads;

a semiconductor chip placed above the generally co-planar surface defined by the upper side of said first group of said at least some of said plurality of leads;

a plurality of electrical connectors electrically connecting said semiconductor chip to a second group of said at least two groups of a plurality of leads; and

sealing material encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors, said lower exposed side and said laterally exposed side of at least one of said plurality of leads resting flush with a bottom surface of said semiconductor package and a side surface of said semiconductor package.

This Sheet Has Been Replaced




2. The semiconductor package of claim 1 wherein said leadframe has a paddle for supporting said semiconductor chip, said paddle having a top side and a bottom side, said top side located in the generally co-planar surface of said leadframe.

3. The semiconductor package of claim 2 wherein said semiconductor chip is eutectically attached to said paddle.

4. The semiconductor package of claim 2 further comprising an epoxy adhesive for attaching said semiconductor chip to said paddle.

5. The semiconductor package of claim 1 wherein said electrical connectors comprise a plurality of wires.

6. The semiconductor package of claim 6 wherein said plurality of wires are selected from a material in the group consisting of: gold, silver, aluminum, or a combination thereof.

7. The semiconductor package of claim 1 wherein said electrical connectors are a plurality of solder balls.

This Sheet Has Been Replaced



* C L M S *

8. The semiconductor package of claim 1 wherein said sealing material is epoxy.

9. The semiconductor package of claim 1 wherein said semiconductor chip is eutectically attached to said plurality of leads.

10. The semiconductor package of claim 1 further comprising an epoxy adhesive for attaching said semiconductor chip to said plurality of leads.

11. The semiconductor package of claim 1 wherein said leadframe is made of copper.

12. The semiconductor package of claim 1 wherein said lower exposed side is plated with a corrosion-minimizing material.

13. The semiconductor package of claim 12 wherein said corrosion-minimizing material is selected from the group comprised of tin, silver, or a combination thereof.

This Sheet Has Been Replaced




14. The semiconductor package of claim 1 wherein said laterally exposed side is plated with a corrosion-minimizing material.

15. The semiconductor package of claim 14 wherein said corrosion-minimizing material is selected from the group consisting of tin or gold.

16. A leadframe, comprising:

a plurality of leads, each one of said plurality of leads has an upper side and a lower exposed side, said upper side of said each one of said plurality of leads forming a generally co-planar surface with said upper side of at least some of said plurality of leads, each one of said plurality of leads has an outwardly extending portion; and

a tie bar connected to said outwardly extending portion of said plurality of leads configured so that when said tie bar is trimmed off said leadframe during the semiconductor packaging process, said trimming off of said plurality of leads leaves a laterally exposed surface of said plurality of leads.

17. The leadframe of claim 16 further comprising a paddle, said paddle having a top side located in said generally co-planar surface.

This Sheet Has Been Replaced



18. The leadframe of claim 16 wherein said leadframe is copper.

19. A semiconductor package, comprising:

a leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side, a lower exposed side, and a laterally exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least two groups of a plurality of leads, said generally co-planar surface of said leadframe for attaching to a semiconductor chip;

a plurality of electrical connectors electrically connecting said semiconductor chip to a second group of said at least two groups of a plurality of leads; and

sealing material encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors, said lower exposed side and said laterally exposed side of said plurality of leads resting flush with a bottom surface of said semiconductor package and a side surface of said semiconductor package.

This Sheet Has Been Replaced

* C L M S *

20. A method for manufacturing a packaged semiconductor, comprising the steps:

attaching a semiconductor chip to a leadframe, said leadframe comprising at least two groups of a plurality of leads wherein each one of said plurality of leads has an upper side and a lower exposed side, the upper side of said each one of said plurality of leads defining a generally co-planar surface with the upper side of a first group of said at least two groups of a plurality of leads, said semiconductor chip attached to the generally co-planar surface defined by the upper side of said first group of said at least some of said plurality of leads;

electrically connecting a plurality of electrical connectors on said semiconductor chip to a second group of said at least two groups of a plurality of leads;

encapsulating said leadframe, said semiconductor chip, and said plurality of electrical connectors with a sealing material, said lower exposed side resting flush with a bottom surface of said semiconductor package; and

trimming off excess encapsulant and a portion of said leadframe to expose a lateral side of said plurality of leads, said lateral side of at least one

This Sheet Has Been Replaced

lead of said plurality of leads resting flush with a side surface of said semiconductor package.

This Sheet Has Been Replaced