

PATENT SPECIFICATION

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(54) INTERCONNECTION OF ELECTRICAL DEVICES

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the provision of circuit connections to electronic apparatus with particular reference to microelectronics.

In microelectronics, it is important to provide a high density of conductive paths in relatively small spaces. Advantageously such conductive paths are provided in layers overlying a supporting substrate and there arises a necessity for the conductive paths in different layers to overlap or cross over one another while maintaining electrical isolation.

Typical is the problem of providing a number of interconnections, either d-c or capacitive, to different circuit elements in a monolithic integrated circuit. Closely related is the problem of making separate connections to two closely spaced regions where it is found desirable to have one connection overlap the edge of the other connection although maintaining electrical isolation therefrom.

A popular method for achieving a desired interconnection pattern in the integrated circuit art involves first forming a continuous conductive layer over the semiconductive wafer, typically electrically isolated therefrom over most of the surface

by an intermediate insulating layer but making connection thereto at selected regions by openings or thickness reductions in the insulating layer. Portions of the conductive layer are then selectively removed to form the first conductive pattern or first level of metallization. Then, after providing an insulating layer over this conductive pattern with appropriate openings or regions of reduced thickness in the insulation where connection to the wafer or the first pattern is desired, a second continuous conductive layer is deposited and selected portions thereof are thereafter removed to form the second conductive pattern or second level of metallization.

Interconnection patterns formed in this way too often exhibit defects localized at the regions where the one of the two conductive patterns crosses over the other.

According to this invention there is provided a process for making an electrically conductive pattern on a substrate, comprising forming on the substrate a conductive layer of non-uniform material, the nonuniformity being such that in a suitable etching medium the rate of etching in a direction parallel to the plane of the layer is greater than the rate of etching in a direction normal to said plane, providing an etch resistant mask over the conductive layer in order to define the required pattern, etching the unmasked part of the conductive layer in the etching medium and forming an insulating layer over at least part of the pattern.

An advantage of the invention is that the conductor edges are free of abrupt discontinuities whereby a more uniform layer of insulating material may be formed thereover before deposition thereover of a

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second conductive pattern. In the preferred embodiment, this is achieved by utilizing for the first conductive pattern a conductor which will exhibit an anisotropic etch rate. Another advantage of the invention is that the incidence of defects is reduced at regions where one conductive pattern crosses another conductive pattern.

Embodiments of the invention will now be described with reference to the accompanying drawing in which:

FIG. 1 illustrates the relatively abrupt discontinuities at the edges of a conductive pattern when the usual prior art process is employed;

FIG. 2 illustrates the more gradual transition in thickness at the edges of a conductive pattern when a process in accordance with the invention is employed; and

FIG. 3A through 3C illustrates an exemplary process in accordance with the invention for providing two levels of conductive patterns on a semiconductive wafer substrate.

With reference now to the drawing, FIG. 1 shows the essentially rectangular cross section of a conductor 11 of the conductive pattern formed on an electrical element in the form of a substrate 12 when the prior art practice is employed for forming the pattern. There is shown the photoresist mask 13 used to localize the removal of the unwanted portion of the original uniform conductive layer during etching. Typically some under-cutting during etching occurs but the angle θ is at least 45° . This angle is still quite large and when an insulating layer is deposited over the edge portions there tends to be created defects in the insulating layer at such regions.

To minimize such defects it is proposed to achieve a more pronouncedly trapezoidal cross section of the conductive pattern 11A on the substrate 12A as shown in FIG. 2. In particular, advantageously provision is made to achieve an angle θ with the mask 13A which is no greater than about 30° so that a more uniform insulating layer can be deposited over the edge portions.

Moreover, the removal of abrupt edge portions is advantageous even when the insulating layer used to provide isolation from an overlying second conductive pattern is formed as a genetic layer formed by conversion in situ of a skin portion of the first conductive layer. In this case the principal advantage arises from the fact that there is made possible a more uniform deposition of the photoresist material normally used in forming contact holes in the insulating layer.

As may be appreciated from FIG. 2, this desired cross section of the conductor can be obtained by providing greater undercutting of the mask, as would be

achieved by providing that the etch rate be faster in the plane of the layer than in its thickness dimension. In order to provide such a gradient or anisotropy in etch rate the conductor can be made non-uniform in any one of a variety of ways. For example, the conductor 11A may be made to etch faster on top than on the bottom as a result of a composition gradient. Such a composition gradient can be realized by coevaporation of two metals such that the resulting alloy has a gradient in the relative compositions of the two metals with thickness, the less etch-resistant metal forming a larger part of the composition at the top than at the bottom. Alternatively the conductor 11A may comprise a conductive polycrystalline semiconductor and the anisotropy in etch rate achieved by a profile in crystalline disorder produced either by ionic bombardment or deposition conditions, use being made of the fact that the more disordered material can be made to etch faster than more ordered material.

An illustrative example of one embodiment of the present invention will be discussed in connection with FIG. 3A through 3C which show successive stages in the formation of a portion of an interconnection pattern of a monolithic silicon integrated circuit. For better exposition, the drawing is not to scale. In FIG. 3A there is shown a silicon wafer 21 which normally includes therein a plurality of circuit elements (not individually shown), which are largely isolated from one another internally by known p-n junction isolation techniques and which are to be interconnected primarily by conductive films on the surface of the wafer. In particular, various openings are provided in the oxide-coating 22 to permit a conductive layer 23 on the surface to make d-c electrical connection to the wafer at such regions. Alternatively, if a capacitive electrical connection is to be made, the insulating layer is merely thinned at regions where such connection is desired. There then remains the problem of interconnecting the regions in a desired fashion to interconnect thereby the circuit elements. In the interest of simplicity, there is being described herein in detail only this portion of the fabrication. There is a variety of techniques now being practiced commercially which can provide an oxide-coated silicon wafer of the kind shown in FIG. 3A which includes on a common surface a plurality of regions which need to be interconnected.

The conductive layer 23 is chosen to etch anisotropically, and in particular to etch in the direction of the plane of the layer faster than in the direction normal thereto. The conductive layer may be formed by codepositing two metals, the ratio of the two

changing with time during the deposition to provide a composition gradient with thickness in the layer deposited. As an illustrative example, the layer may be composed of copper and gold, and the material initially deposited being predominately gold, and the proportions of the two shifted with time till the final material deposited will be predominantly copper. There is then used an etch which etches faster the greater the copper content. As another example, the conductive layer deposited may be of polycrystalline silicon doped to be highly conductive, the deposition conditions being such that the material initially deposited is relatively well ordered but that with increasing time the amount of disorder in the material deposited increases. This can be achieved for example by decreasing with time the temperature of the substrate as the silicon is being deposited. Alternately, a uniform polycrystalline layer may be deposited and the disorder introduced to the top of the layer by ion bombardment. As another alternative, the layer may be highly conductive p-type silicon whose doping is higher the nearer the surface.

After formation of the conductive layer, there needs to be removed the excess material to define the desired first conductive pattern. This can be done in the manner now used in the integrated circuit art and typically involves photolithographic techniques the end product of which is the formation of an etch-resistant mask over the conductive layer conforming to the conductive pattern desired for this first level of metallization.

Next the masked wafer is exposed to an etchant which will etch in the desired anisotropic fashion the conductive layer and leave on the surface the desired first conductive pattern 24 as shown in FIG. 3B.

For the example involving the binary composition layer of copper and gold described above, an aqueous solution of ferric chloride or an aqueous solution of 70 percent nitric acid is a suitable etchant. For the example described involving disordered polycrystalline silicon, a suitable etchant comprises a mixture which by volume is three parts a 48 percent aqueous solution of hydrofluoric acid, five parts a 70 percent aqueous solution of nitric acid, 3 parts of glacial acetic acid and 2 parts of a 3 percent aqueous solution of mercurous nitrate. Actually, there is known from use in metallurgical studies a large number of etchants which etch damaged material faster than ordered material. Moreover, an etchant for etching p-type silicon anisotropically is described in a paper entitled "A Water-Amine Complexing Agent System for Etching Silicon", appearing at

pages 956-970 of the September 1967 issue of the *J. Electrochem. Soc. Solid State Science*.

The etching is continued until the oxide layer is reached at the exposed portions of the conductive layer. The anisotropic etching will result in appreciable undercutting of the mask to provide tapered edges to the conductor remaining unetched forming the first conductive pattern. As shown in FIG. 2, the cross section of the conductor will have a pronouncedly trapezoidal shape although there will be some rounding at the corners.

Thereafter, the mask is removed in the normal fashion, and a layer of insulating material, which typically may be silicon dioxide is deposited over the surface of the wafer to cover the conductive pattern and to permit formation of a second conductive pattern insulated from the first. It can be appreciated that the use of tapered edges for the conductor forming the first conductive pattern permits this layer of insulating material to be deposited more uniformly over the conductor.

In some cases, it may be advantageous to form the insulating layer by conversion in situ of a top portion of the conductive pattern. For example, if the first pattern formed is of silicon, heating in an oxidizing atmosphere in the usual manner can be used to form an insulating layer thereover. In this instance, the tapered edge will prove advantageous in the subsequent processing. In particular, it will facilitate subsequent uniform deposition of the photoresist layer normally used to control the shaping of the insulating layer over the first layer of metallization and again serve to reduce the likelihood of defects in the overlap of the crossover region.

There then needs to be formed the second level of conductive pattern desired.

First, if this pattern is to make electrical connection to the semiconductive wafer, either direct or capacitively, appropriate openings or thinning of the insulating layers over the wafer are first provided at the regions desired for connection. This advantageously can be done by the usual photolithographic techniques and so will not be described in detail.

After the appropriate openings have been provided, there is deposited advantageously a continuous conductive layer. If the desired interconnection pattern necessitates yet another conductor overlapping or crossing over the second pattern, the material forming the second pattern can also with advantage have anisotropic etching properties. However, if it will be unnecessary to form additional crossing or overlapping patterns, this second conductive pattern can be formed in con-

ventional manner using normal materials. Thereafter, in any case photolithographic techniques are used to remove excess material from this second continuous layer to leave behind the desired conductive pattern 25, insulated from the first conductive pattern 24 by an insulating layer 26, as seen in FIG. 3C. In the interest of simplicity, the full extent of insulating layer 26 is not shown.

The invention also has applicability to the formation of a conductive path which does not completely cross over an underlying conductor but merely overlaps, although maintaining electrical isolation. This situation arises typically where it is advantageous to make separate connections either direct or capacitive to two closely spaced regions of a semiconductive wafer as arises for example in some forms of insulated gate field effect transistors or charge coupled devices.

It should be evident that the basic principles of the invention can be extended to any form of microcircuit involving multilayer interconnection patterns, such as thin- and thick-film circuits involving simply resistances and capacitances, and functional circuits such as charge-coupled devices involving primarily capacitive connections to a semiconductive wafer. The invention even may have applicability to magnetic microcircuits when the need arises for multilayer interconnections.

WHAT WE CLAIM IS:—

1. A process for making an electrically conductive pattern on a substrate, comprising forming on the substrate a conductive layer of non-uniform material, the nonuniformity being such that in a suitable

etching medium the rate of etching in a direction parallel to the plane of the layer is greater than the rate of etching in a direction normal to said plane, providing an etch resistant mask over the conductive layer in order to define the required pattern, etching the unmasked part of the conductive layer over at least part of the pattern.

2. A process according to claim 1, wherein in order to provide said non-uniformity said material is a conductive binary alloy whose composition varies according to position in the conductive layer in order to provide the anisotropic etching rate.

3. A process according to claim 1, wherein in order to provide said non-uniformity said material is polycrystalline and the lattice disorder thereof varies according to position in the conductive layer in order to provide the anisotropic etching rate.

4. A process according to claim 1, wherein the substrate is an oxide coated silicon crystal and the conductive layer is of polycrystalline silicon.

5. A process for making an electrically conducting pattern on a substrate, substantially as herein before described with reference to FIGS. 2 and FIGS. 3a, 3b and 3c of the drawings.

6. A substrate with an electrical conductor pattern prepared by the process according to any one of the preceding claims.

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