ABSTRACT

A METHOD TO FABRICATE A SUB-QUARTER-MICRON MOSFET WITH LIGHTLY DOPED SOURCE/DRAIN REGIONS

A new method of fabricating a MOSFET device is described. A semiconductor substrate is provided and isolation areas are formed isolating active areas in the substrate. An oxide layer is provided overlying both the substrate and isolation area and is patterned and etched to expose two areas within an isolated active area of the substrate. Selective epitaxial growth (SEG) using intrinsic silicon is performed to fill the exposed substrate areas formed in the previous etch step. The oxide layer region in the active area between the two epitaxially grown silicon regions is then etched, exposing the substrate. This is followed by a gate oxide growth and a polysilicon deposition. Planarization is then performed on the surface to expose the two epitaxially grown silicon regions. A second oxide is grown consuming some of the polysilicon gate and the epitaxially grown silicon. This consumption occurs at a higher rate at the upper surface and thus shapes the gate and epitaxially grown silicon into trapezoids with the base being wider than the top. The oxide is then etched leaving V-shaped trenches between the polysilicon and epitaxially grown silicon. A low-angle implantation is performed creating the source/drain extensions in the substrate below the V-shaped trenches. A third oxide is deposited filling the V-shaped groove and overlying the surface of the wafer. A second planarization is performed exposing the top of the epitaxially grown silicon regions and the polysilicon gate. A second implantation is performed to dope the polysilicon gate and epitaxially grown silicon regions. The doped portions of the epitaxially grown silicon form the source /drain electrodes of the MOSFET. This is then followed by a salicidation step for metalization and annealing of the second implantation completing the MOSFET device.

(FIGURE 7 IS SUGGESTED FOR PUBLICATION)