

The present invention relates to a method for the evaluation of signals of an incremental transducer. An incremental transducer is a device which is used for the digital control of positioning elements. It consists e.g. of a pulse generator in the form of a disc, on which there are made in tangential direction at identical angular distances optically or mechanically scannable marks, which on movement of the disc, e.g. by rotation, emit pulses in cooperation with sensors. In order to detect the direction of movement of the disc, two sensors are used which are arranged offset in such a way that there are created at two outputs of the incremental transducer two pulse trains phase-displaced by 90 degrees. The direction of movement may in this way be recognized from the phase position of the two output signals. The pulses of one of the two outputs serve for the step-wise adjustment of a positioning element, which according to the direction of movement of the incremental transducer emits a control voltage variable step-wise to higher or lower values. The output pulses are evaluated in such a way that e.g. each positive edge varies a control value by one step upwards or downwards. In the case of simply constructed incremental transducers there is the disadvantage that the generated pulses exhibit at their edges disturbance which is known by the term "contact bounce". This means that at each positive edge of such disturbing pulses the positioning element is advanced by one step, that therefore with a uniform movement of the incremental transducer various step widths may result, that e.g. a plurality of steps are evaluated forwards and backwards, although only a single pulse was to have been generated and the incremental transducer is moved in only one direction.

In US patent specification 4 308 500 a circuit is described which is used for the decoding of signals of an incremental transducer. It is intended with said circuit also to detect and eliminate disturbance. It is intended to achieve with said circuit that the output pulses of the incremental transducer become effective only if the signal is set for the direction of rotation in a stable manner. To this end the strobe signals are delayed. This takes place with the aid of time lag elements. Such a circuit, however, is suitable only for cutting out disturbance at higher frequencies. An arrangement or a method for removing disturbing pulses which occur in the region of the edges of the output pulses is not however involved there.

The aim of the invention is to debounce in the case of a simply constructed incremental transducer the generated very noisy switching edges of the pulses, in order thereby to ensure an unambiguous evaluation of the signals. This aim is achieved by the invention stated in the patent claim. Further developments of the invention follow from the sub-claims.

The invention will be explained below with reference to an exemplifying embodiment.

Fig. 1 shows pulse diagrams of an incremental transducer which forms the basis of the invention.

- Fig. 2 shows a block circuit diagram by way of explanation of the invention.
- Fig. 3 shows a detail of the block circuit diagram according to Fig. 2.
- Fig. 4 shows a flow chart by way of explanation of the method.

In Fig. 1 there is represented a pulse diagram which shows the signals at the outputs A and B of the incremental transducer. Since, according to the assumption on which the invention is based, an incremental transducer is involved whose output signals are affected by bounce, said signals are disturbed in particular in the regions T of the edges. Said bounce complicates decoding, or else makes it impossible, unless special measures are taken. The measures to be used for this purpose are however expensive. In order to avoid such an expenditure, the method described below is applied.

The block circuit diagram according to Fig. 2 serves as an explanation of the method. It should be pointed out that the timing of the steps of the method may easily be carried out by a microprocessor, whereby the cost of materials drops dramatically, since the program required for this is stored, as will be shown later with the aid of Fig. 4.

In Fig. 2 there is labelled as 1 an incremental transducer, to whose outputs A and B there are applied the signals a and b according to Fig. 1. The signal pattern according to Fig. 1 occurs only if the incremental transducer is operated by means of the handle 1', i.e. if the incremental transducer 1 is set. Otherwise there occur statically at the outputs A and B any combinations 0 and 1. An incremental transducer emits to the outputs A and B, depending on the direction of rotation R or L, the following combinations: e.g. in the one operating direction the sequence: 00:01:11:10:00... and in the other operating direction the sequence: 00:10:11:01:00... . It will be seen from this example that the order of the output signals a and b always obeys the following scheme irrespective of the operating direction: $a = b = 0$, $a \neq b$, $a = b = 1$, $a \neq b$, $a = b = 0 \dots$. If said order is not adhered to, this is an indication that the signal pattern at one or both of the outputs A, B is disturbed. Said criterion is utilized in the procedure described below.

The signal conditions a and b occurring at the outputs A and B vary with a frequency which depends on the nature of the operation of the incremental transducer 1, e.g. on the angular speed of the handle 1'. Said signal conditions are passed to an intermediate storage means 2, which is triggered with a clock frequency from a clock generator 3. The clock frequency must moreover be at least four times as big as the highest signal frequency generated by the incremental transducer 1. By rapid operation of the incremental transducer the latter may emit e.g. a frequency of 5 kHz, so that the frequency of the clock generator should come to at least 20 kHz. The signal conditions

$a(n)$, $b(n)$ read out from the intermediate storage means 2 are compared in a comparison stage 5 with the signal conditions $a(n-1)$, $b(n-1)$ of a previous enquiry, which have been stored in a storage means 4. Whether and when the previous signal conditions $a(n-1)$ and $b(n-1)$ are stored in the storage means 4 is determined by a comparison stage 6 which will be explained later. If the signal conditions $a(n)$, $b(n)$ are different from the signal conditions $a(n-1)$, $b(n-1)$, as is the case if the incremental transducer has been set, a pulse is transmitted to a counter 7, which may assume e.g. four conditions, 0, 1, 2, 3.

Said counter 7 activates via its outputs in steps the comparison stage 6, which has the function of monitoring the pre-determined sequence of the signal conditions a , b from the incremental transducer 1. If the sequence complies with the rules, a signal reaches the output OK. Said signal emits a strobe pulse to the input T of the storage means 4, so that the current signal condition is made available together with the next following one for the comparison in the comparison stage 5. If the sequence does not comply with the rules, a signal reaches the output OK. Said signal on the one hand re-sets the counter 7 to the initial position 0, on the other it sets the storage means 4 to a defined initial value, e.g. 0, 1 or 1, 0. During further advance of the counter 7 via an OR gate 9 the sequence of the signal conditions is checked. If the condition $a \neq b$ is established, a direction register 8, which outputs the direction of variation of the incremental transducer 1, is triggered via the input T. The direction register 8 consists e.g. of a D-type flip-flop. After that the comparison stage 6 checks the condition $a = b = 1$. During the subsequent condition $a \neq b$ the counter is again brought to the basic position 0 and a disturbance-free pulse IMP is emitted.

There is shown in Fig. 3, by way of explanation of the mode of operation of the comparison stage 6 in Fig. 2, a possible circuit layout. The signal conditions a , b are supplied in parallel to four logic gates. The NOR gate 10, the EXOR gate 11, the AND gate 12 and the EXOR gate 13 are involved. Said gates are activated in cyclic sequence by the outputs 0, 1, 2, 3 of the counter 7 via AND gates 14, 15, 16, 17. On each occasion that the logic operation is fulfilled at times pre-determined by the outputs of the counter, a signal reaches the output OK of the comparison stage 6 via the OR gate 18. Otherwise there appears at the output OK of the comparison stage 6 a signal via the inverter 19. If the pre-determined sequence is adhered to, there appears on each occasion at the output OK a signal and the output 2 emits a pulse IMP. In the case of disturbed signal conditions said pre-determined sequence is not obtained, so that it is also impossible for a pulse to be obtained at the output 2.

As was already pointed out at the start of the description, said method explained with a circuit as an example may be implemented in the form of a program, the operating sequence of which will be explained with reference to Fig. 4.

At the start of the program routine the incremental transducer is read out and in a following step the signal conditions are compared with a previously stored value. If equality is established, the program skips back to the beginning. If inequality is established, which is an indication of the operation of the incremental transducer, it is checked continuously whether the different conditions conform to the correct sequence. In a first comparison it is enquired whether the counter is emitting the condition $Z = 0$. In this case it is checked whether the incremental transducer is emitting the condition $IG0$. The condition $IG0$ is defined as $a = 0$ and $b = 0$. If said condition $IG0$ is not established, the program skips back to the beginning. If $IG0$ is established, the next condition $Z = Z+1$ is set, and the read-out value a, b transferred into the storage means 4, and the program begins with a new enquiry. The new enquiry establishes whether $Z = 1$ is set. In this case it is enquired whether the condition $IG1$ is present. $IG1$ means that the outputs a, b are different. If this is not the case, the condition $Z = 0$ is set and the program skips back to the beginning. If $IG1$ is established, then the condition $Z = Z+1$ is set, and the values for a, b are in turn written into the storage means 4, and the program skips back to the beginning. On renewed enquiry the condition $Z = 2$ is enquired about, it being established in the case of an affirmative answer whether the condition $IG2$ is reached. $IG2$ means that both outputs a, b are equal to 1. If $IG2$ is answered in the negative, the condition $Z = 0$ is again set and the program skips back to the beginning. If the condition $Z = 2$ is answered in the negative, this means that the condition $Z = 3$ is enquired about and it is thereupon established whether $IG1$ is again present, i.e. both outputs a, b must be different. If this is the case, a pulse IMP is emitted and the program skips back to the beginning and the evaluation starts afresh. It will be seen that a pulse IMP is generated only if the sequence of the signals a, b conforms to the pattern $00:01(10):11:10(01)$.

Incremental transducers of this kind are used e.g. for the control of positioning elements for loudness level, high and low-pitched notes or else balance in a low-frequency amplifier, or for frequency setting in a radio or television receiver, for the operation of a search run or for tracking skips during the scanning of a compact disc in a CD playback unit. An incremental transducer of this kind may also be used with advantage for the search run or for setting the timer in a video recorder. The latter may also be successfully used, to take a further example, as a speed and direction sensor in vehicles of all kinds.

Claims

1. Method for the evaluation of signals at the outputs (A, B) of an incremental transducer ($1, 1'$), in which the signals consist of two phase-displaced pulses ($Sa, Sb = 0$ or 1) with a defined, direction-dependent signal sequence ($Sa, Sb = 0,0; 0,1; 1,1; 1,0$ or $0,0; 1,0; 1,1; 0,1$), characterised in that in order to distinguish between mains pulses and

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disturbing pulses the signals ($S_a(n)$, $S_b(n)$) are compared respectively with the signals ($S_a(n-1)$, $S_b(n-1)$) which have come before in time, the successive signals being subjected to a logical test condition whether they conform to the defined signal sequence, and that a mains pulse is derivable at the output (A or B) of the incremental transducer (1, 1') only if the logical condition is fulfilled.

2. Method according to claim 1, characterised in that the signals (S_a , S_b) are periodically scanned at the outputs (A, B) of the incremental transducer (1) and stored temporarily in a first storage means (2) whose contents are transferred to a second storage means (4) if the defined signal sequence is adhered to.
3. Method according to claim 2, characterised in that the frequency for the scanning of the first storage means (2) is at least four times as high as the highest frequency generated by the incremental transducer.
4. Method according to claim 2, characterised in that the signals ($S_a(n)$, $S_b(n)$) of the incremental transducer (1) read out from the first storage means (2) are compared with the signals ($S_a(n-1)$, $S_b(n-1)$) read out from the second storage means (4) in a comparison stage (5).

