159159

Photoarray for detecting time-dependent image data

Technical Field

The invention relates to a photoarray, i.e. an array of photosensitive elements, for detecting time-dependent image data, which comprises an array of cells, with each cell having a photosensor generating a signal dependent on a light intensity at the cell.

Background Art

Real time artificial vision using a photoarray, such as disclosed in US 2003/0015647, is traditionally limited to the frame rate at which the array is sampled. On the other hand, such photoarrays generate a huge amount of redundant data that needs powerful and costly post processing.

Disclosure of the Invention

The problem to be solved by the present invention is to provide a photoarray that is better suited for real time artificial vision. This problem is solved by the photoarray of claim 1.

Accordingly, the photoarray of the present invention comprises a topologically one- or two-dimensional array of cells, which may or may not have rectangular boundaries, where each cell has a photosensor generating a sensor signal dependent on the light intensity at its cell, a first capacitor being charged by current proportional to the time derivative of the sensor signal, at least one threshold detector detecting if the voltage over said first capacitor exceeds a threshold value and generating an output signal if yes, and a dis-

G00002

charge device for discharging the first capacitor after occurrence of said output signal.

In other words, charging (or discharging) the first capacitor to a given charge (defined by the threshold value) generates an event in the form of the output signal. This method of digitization is especially suited for a photoarray because it allows to reduce, in very simple manner, the amount of data at its source, namely at the cell. Data communication out of the array only occurs when the incoming light intensity changes. Hence, the amount of data to be processed is reduced drastically and the photoarray can transfer information at a higher rate than a conventional device.

The discharge device is used to reset the capacitor after an event.

The photoarray may further comprise a signal collector collecting the output signals from all the cells.

Advantageously, upon receipt of an output signal from a given cell, the signal collector controls a reset signal generator of the given cell to generate a reset signal for discharging the first capacitor. This allows the signal collector to control the firing rate of the cells.

Each cell can further comprise a second capacitor in series to the first capacitor. The first capacitor in arranged between an input and an output of an inverting amplifier and the second capacitor is arranged between the photosensor and the amplifier's input. The two capacitors and the amplifier form a switched capacitor amplifier. Advantageously, the second capacitor is much larger (e.g. ten times as large) than the first capacitor, which allows to achieve a high amplifier gain. Since the ratio between the capacities of the capacitors defines the closed-loop gain of the amplifier and since capacitors can be manufactured with high accuracy on a chip, this technique allows all cells of the photoarray

to have very similar response even if the properties of other elements in the cells differ due to tolerances in the manufacturing process.

Advantageously, the signal from the photosensor is proportional to the logarithm of the incoming light intensity at the given cell, which allows detection of signals over a wide dynamic range and, additionally, removes dependence on the absolute illumination.

Brief Description of the Drawings

The invention will be better understood and objects other than those set forth above will become apparent when consideration is given to the dependent claims or the following detailed description thereof. Such description makes reference to the annexed drawings, wherein:

Fig. 1 is a circuit diagram of a single cell of a photoarray according to the present invention,

Fig. 2 is a block circuit diagram of part of the photoarray of Fig. 1, and

Fig. 3 are is a timing diagram of some of the signals in the cell of Fig. 1.

Modes for Carrying Out the Invention

As mentioned above, the photoarray of the present invention comprises a plurality of, advantageously identical, cells, where each cell has a photosensor generating a sensor signal and circuitry for processing the sensor signal.

An possible embodiment of such a cell is shown in Fig. 1.

At the input side of the cell, it comprises a photodiode D generating a photocurrent proportional to the incoming light intensity I.

The photosensor further comprises four transistors T1, T2, T3 and T4, which form an amplifier with substantially logarithmic response, generating a sensor signal having a voltage linearly related to log(I) at point P1, i.e. the voltage V at point P1 is V = const + k·log(I) with constant values k and const. Similar circuitry is e.g. known from US 5 376 813, the disclosure of which is incorporated by reference herein.

The feedback arrangement has the additional advantage that it speeds up the response time of the circuit by actively clamping the photodiode voltage at a virtual ground, so that a change in photocurrent need only charge or discharge the photodiode capacitance by a small amount.

In the embodiment of Fig. 1, the currents through the photodiodes D of all cells are summed in a current adder 1 and a voltage proportional to the logarithm of this sum is fed to the gate of transistor T3, which allows a reduction of the power consumption of the amplifier at low intensities. This technique is described in US 2004/0067876, the disclosure of which is incorporated by reference herein.

The voltage from point P1 is fed to the gate of a transistor T5a in series with a transistor T5b of the same polarity. The gate voltage of transistor T5b is at a fixed potential. Transistors T5a and T5b form a near-unity-gain source follower voltage buffer. The voltage at the output P2 between the transistors is again linearly related to log(I). The purpose of the voltage buffer is to isolate the two stages, thereby reducing feedback and possible instability.

The voltage from output P2 is fed to a switched capacitor amplifier formed by two transistors T6 and T8 in series, a first capacitor C1, a second capacitor C2 and a transistor T7. Transistor T7 acts as a discharge device for discharging the first capacitor C1. Transistor T6 is an inverting amplifier with an amplifier

output P3 located between transistors T6 and T8. First capacitor C1 is arranged between amplifier output P3 and the input of this inverting amplifier (i.e. the gate of transistor T6), i.e. the amplifier will strive keep the voltage at the gate of transistor T6 constant by adjusting the voltage over first capacitor C1. The voltage at the gate of second transistor T8 is at a given, fixed potential "diff". Transistor T8 sinks a bias current for amplifier input transistor T6. It also determines in part the output resistance of the amplifier. The inverting amplifier formed from T6 and T8 is designed to have voltage gain substantially larger than the ratio of capacitor values C2/C1.

The operation of the switched capacitor amplifier is as follows: After a reset of the amplifier by discharging capacitor C1 by shorting it to the output node P3 through transistor switch T7, the voltage at amplifier output P3 is equal to the voltage at the gate of transistor T6. This voltage is determined by the bias current sunk by transistor T8. Turning off transistor switch T7 (opening the switch) places the switched capacitor amplifier in the active amplifying condition. If the inverting amplifier formed by T8 and T9 has open loop gain substantially larger than the capacitor ratio C2/C1, the closed-loop gain of the switched capacitor amplifier is given by the ratio C2/C1, which is advantageously set to be fairly high, e.g. C2/C1 = 10, for the reasons mentioned above. Then feedback from P3 to the gate of transistor T6 holds the gate of T6 closely to a constant voltage—a virtual ground. Therefore current flowing onto capacitor C2 must also flow out of capacitor C1. This current is proportional to the change rate of the voltage at P2, i.e. proportional to d(log(I))/dt. The voltage appearing at output P3 is proportional to the change at input P2 times the closed loop gain C2/C1.

The voltage of amplifier output P3 is fed to two threshold detectors. The first of these threshold de-

tectors is comprised of a first transistor assembly consisting of a transistor T9 and a second transistor assembly consisting of two transistors T10, T11 arranged in parallel. Transistor T9 of the first transistor assembly has the same polarity, geometry and size as transistor T6. Transistors T10, T11 of the second transistor assembly have the same polarity, geometry and size as transistor T8, and they are connected in parallel, i.e. their drains, sources and gates are tied to each other. The drain-source channel of transistor T9 is in series to the drain-source channels of transistors T10 and T11. The gates of the transistors T10 and T11 are connected to a fixed potential "on", which is substantially equal to the potential "diff". The output ON of the first threshold detector is formed by point P4 between the two transistor assemblies T9 and T10, T11.

For illustration we will consider the condition where the potentials "diff", "on", and "off" are identical, although it will become evident that their relative values determine the actual thresholds.

The first threshold detector works as follows: After discharging first capacitor C1, amplifier output P3 and therefore the gate voltage of transistor T9 is at the same potential as the gate of transistor T6. Since the parallel transistors T10, T11 are capable of sinking twice the current of the single transistor T8, voltage ON is near ground and transistor T9 is saturated.

When the voltage at point P2 rises, capacitors C1 and C2 are charged and the voltage at amplifier output P3 drops. Once that the voltage at amplifier output P3 is below a given lower threshold voltage, transistor T9 becomes capable of sourcing more current than the transistors T10 and T11, and transistors T10 and T11 become saturated and the voltage at point P4 rises to near the positive supply, i.e. output signal ON goes to logical 1. As described below, output signal ON is fed to a signal collector, which will eventually generate a reset

signal at the gate of transistor T7 for discharging first capacitor C1. Voltage at amplifier output P3 goes back to its original value and output signal ON goes back to 0. The cycle can restart again.

The second threshold detector is comprised, as the first threshold detector, of two transistor assemblies. However, in this case, the first transistor assembly consists of two parallel transistors T12, T13, while the second transistor assembly consists of a single transistor T14. The transistors T12, T13 are of equal polarity, size and geometry as transistor T6, while transistor T14 is of equal polarity, size and geometry as transistor T8. The output OFF of the second threshold detector is formed by point P5 between transistor assembly T12, T13 and transistor assembly T14.

The operation of the second threshold detector is similar to the one of the first threshold detector. However, after discharging capacitor C1, transistor T14 will be saturated and signal OFF will be logical 1. When the voltage at point P2 starts to drop, the voltage at amplifier output P3 starts to rise according to the charge accumulated on capacitor C1, until is reaches a given upper threshold voltage, where transistors T12 and T13 become saturated, the voltage at point P5 starts to drop and output signal OFF goes to logical 0. Output signal OFF is again fed to the signal collector, which will eventually generate a reset signal at the gate of transistor T7 for discharging first capacitor C1.

The preferred embodiment uses transistor assemblies T10,T11 and T12,T13 consisting of two transistors connected in parallel, because the use of these "unit transistors" results in thresholds that are better controlled against process variations and allow the use of nominally-identical control signals "diff", "on" and "off". However, it should be clear that these transistor assemblies can be each replaced by single transistors as long as "on" and "off" are controllable.

From the above it becomes apparent that the circuitry shown in Fig. 1 generates two output signals ON and OFF. Signal ON is issued when the voltage over first capacitor C1 rises above a given first, positive threshold value, while signal OFF is issued when the voltage over first capacitor C1 falls below a given second, negative threshold value. Once an output signal ON or OFF is issued, the circuitry can be reset by feeding a reset signal to transistor switch T7.

In the following, the operation of the cell of Fig. 1 in the photoarray is described by reference to Fig. 2.

The cells 10 can be arranged in a one- or two-dimensional array. Fig. 2 shows an embodiment with a two-dimensional array, where the cells 10 are arranged in rows and columns. For simplicity, only one cell 10 is shown in Fig. 2 - all other cells are arranged in the same manner, each at an intersection of a row and a column.

As can be seen, the ON and OFF output signals of cell 10 at row i and column j are fed to two transistors T20a, T20b (after inversion of the OFF output signal by means of an inverter, thereby taking account of the negative polarity of the signal generated by the second threshold detector) and they are "wire-ored" to a row signal line i. In fact, the output signals of all cells of a given row i are "wire-ored" to the same row signal line i. A pullup device on each row pulls the row line high when no cells in the row pull it low. The signals on the row signal lines are called "row signals".

All row signal lines are fed to a row arbiter 14, which forms part of the signal collector of the photoarray. Once that row arbiter 14 receives a row signal on a given row signal line i and it has no other row signals pending, it issues a row acknowledge signal on a row acknowledge line i attributed to the same row i. The row acknowledge signal is only issued once row arbiter 14 de-

termines that the photoarray is ready to process a next event, as described below.

The row acknowledge signal is fed to two AND-gates 16, 18 attributed to each cell of the given row i. First AND-gate 16 ANDs the row acknowledge signal and the inverted OFF output signal, and second AND-gate 18 ANDs the row acknowledge signal and the ON output signal. Hence, the AND-gates 16, 18 generate signals only if a cell is currently issuing a row signal and receives a row acknowledge signal. The signals from the AND-gates 16, 18 are fed, through transistors T21, T22 to a column signal OFF line j and a column signal ON line j attributed to column j, which again allows to "wire-or" all the column signals of a given column.

All column signal OFF lines and column signal ON lines input to a column arbiter 20, which forms part of the signal collector of the photoarray. Once that column arbiter 20 receives a column signal on a given column signal ON line j or column signal OFF line j, it issues a column acknowledge signal on a column acknowledge ON line j or a column acknowledge OFF line j, respectively, attributed to the same column j. The column acknowledge signal is only issued once column arbiter 20 knows that the photoarray is ready to process a next event, as described below.

The signals from the column acknowledge OFF line and the column acknowledge ON line are fed to an OR-gate 22 to generate a column acknowledge signal on a common column acknowledge line j. At each cell the signals from the row acknowledge line and the column acknowledge line of the corresponding row and column are fed to an AND-gate 24 and from there to a pulse generator 26 to generate the reset signal to be fed to transistor T7.

Hence, first capacitor C1 is discharged as soon as the row and column arbiters both generate a row and column acknowledge signal on the row and column acknowledge lines of the corresponding cell. Discharging

first capacitor C1 will force the output signals ON and OFF of cell 10 to go to their inactive state.

The pulse generator 26 generates a pulse of controllable duration, called the refractory period. During refractory period the switched capacitor amplifier is held in reset. The purpose of controllability of the refractory period is to limit the firing rate of the output signals ON and OFF of each cell, thereby preventing a single cell from overloading the signal collector, either in case of malfunction or a very rapidly changing input signal.

The signal collector of the photoarray further comprises an encoder 28, which has inputs r and c connected to all row acknowledge lines as well as all column acknowledge OFF lines and column acknowledge ON lines of the photoarray. Once that both the row arbiter 14 and the column arbiter 20 acknowledge an event from a given cell, encoder 28 can determine the address of that cell from the state of the row and column acknowledge lines, because only those belonging to the given cell will be in their active state. It also can determine if the signal generating the event was an ON or an OFF signal. The corresponding address and state (ON or OFF) information is fed as an "event" to a buffer 30 to be accessed by an external receiver. After the event has been collected from buffer 30, buffer 30 tells row arbiter 14 and column arbiter 20 that it is ready to store a next event. Column arbiter 20 drops its column acknowledge signal and row arbiter 14 is ready to acknowledge a next row signal.

As can be seen from the above, the photoarray can generate ON and OFF events from all its pixels. The rate of these events depends on the rate of change of the light signal. Using the ON and OFF events for each pixel, it becomes possible to reconstruct the input signal at the given pixel. This is illustrated in Fig. 3, where upper graph shows the input signal I, its time derivative

d/dt and the voltage over first capacitor C1, where the ON and OFF events are indicated by circles. The lower graph of Fig. 3 shows the input signal and the reconstructed input signal, the latter being calculated by adding a given intensity at each ON event and subtracting the same at each OFF event.

In the embodiment shown so far, there was one row signal line per row and two column signal lines per column. Two column signal lines were required for encoding the polarity (ON or OFF) of the signal. Alternatively, there could be two row signal lines for encoding the polarity and only one column signal line.

Similarly, if only the ON or the OFF output signals, and not both, are to be collected by the photoarray's signal collector, only one row signal line per row and only one column signal line per column would be required. In that case, however, other measures must be taken to generate a reset signal for discharging capacitor C1 after generating a signal not forwarded to the arbiters. For example, if only the ON output signals are fed to the arbiters, the OFF output signal could be fed directly and locally back to transistor T7 for resetting the cell.

While there are shown and described presently preferred embodiments of the invention, it is to be distinctly understood that the invention is not limited thereto but may be otherwise variously embodied and practiced within the scope of the following claims.

Claims

1. A photoarray for detecting time-dependent image data comprising an array of cells (10), each cell (10) comprising

a photosensor (D, T1 - T4) generating a sensor signal dependent on a light intensity at said cell (10),

a first capacitor (C1) being charged by a current proportional to a time-derivative of said sensor signal,

at least one threshold detector (T9 - T11, T12 - T14) detecting if a voltage over said first capacitor (C1) exceeds a threshold value and generating an output signal (ON, OFF) if yes, and

a discharge device (T7) for discharging said first capacitor (C1) after occurrence of said output signal (ON, OFF).

2. The photoarray of claim 1 wherein each cell (10) further comprises a second capacitor (C2) in series to said first capacitor (C1), wherein said first capacitor (C1) in arranged between an input and an output of an inverting amplifier (T6) and said second capacitor (C2) is arranged between said photosensor (D, T1 - T4) and said input.

3. The photoarray of claim 2 wherein said second capacitor (C2) is much larger than said first capacitor (C1).

4. The photoarray of any of the claims 2 or 3, wherein said inverting amplifier (T6) is formed by a first transistor (T6) with said first capacitor (C1) arranged between an amplifier output (P3) and a gate of said first transistor (T6), wherein a drain-source channel of said first transistor (T6) is in series to second transistor (T8) of opposite polarity, wherein a gate of the second transistor (T8) is applied to a defined potential.

5. The photoarray of claim 4,

wherein said threshold detector (T9 - T11, T12 - T14) comprises a first transistor assembly (T9; T12, T13) in series to a second transistor assembly (T10, T11; T14),

wherein at least one transistor assembly comprises at least one transistor (T9; T12, T13) and wherein at least one transistor assembly comprises at least two transistors (T10, T11; T14),

wherein the transistors of the first transistor assembly (T9; T12, T13) have the same polarity, geometry and size as the first transistor (T6) and wherein the transistors of the second transistor assembly (T10, T11; T14) have the same polarity, geometry and size as the second transistor (T8),

wherein the amplifier output (P3) is connected to the gate or gates of the transistors of the first transistor assembly (T9; T12, T14), and

wherein said output signal (ON, OFF) is generated at a point (P4, P5) between said first and said second assembly.

6. The photoarray of claim 5, wherein the gate or gates of said transistor(s) in said second assembly (T10, T11; T14) are tied to substantially the same voltage as the gate of the second transistor (T8).

7. The photoarray of any of the preceding claims wherein said array of cells (10) is a two-dimensional array of cells (10).

8. The photoarray of any of the preceding claims further comprising a signal collector (14, 20, 28, 30) collecting said output signals (ON, OFF) from all said cells (10).

9. The photoarray of claim 8 further comprising reset signal generators (24, 26), wherein each reset signal generator (24, 26) is connected to trigger the discharge device (T7) of one of said cells (10),

wherein said output signals (ON, OFF) are fed to said signal collector and wherein, upon receipt of an output signal (ON, OFF) from a given cell (10), said signal collector controls said reset signal generator (24, 26) of the given cell (10) to trigger the discharge device (T7) of the given cell (10).

10. The photoarray of any of claim 9, wherein said array of cells (10) is a two-dimensional array of cells (10), wherein said cells (10) are arranged in rows and columns, said photoarray comprising

one or two row signal lines per row, wherein the output signals (ON, OFF) of the cells (10) of each row are tied as row signals to said row signal line,

a row arbiter (14) connected to said row signal lines and detecting said output signals (ON, OFF),

one row acknowledge line per row, wherein said row arbiter (14) generates a row acknowledge signal on said row acknowledge line upon receipt of an output signal (ON, OFF) on the row's row signal line,

one or two column signal lines per column, wherein each cell (10) generates a column signal on its column signal line if it generates a row signal on its row signal line and obtains a row acknowledge signal on its row acknowledge line,

a column arbiter (20) connected to said column signal lines and detecting said column signals, and

one column acknowledge line per column, wherein said column arbiter (20) generates a column acknowledge signal upon receipt of a column signal on the column's column signal line,

wherein said reset signal generator (24, 26) of each cell (10) is connected to said row acknowledge line and said column acknowledge line of its cell (10) for triggering said discharge device (T7) in the presence of a row acknowledge signal and a column acknowledge signal.

11. The photoarray of claim 10 further comprising an encoder (28) connected to said column acknowledge signal lines and row acknowledge signal lines for calculating an address of the cell (10) generating an output signal (ON; OFF).

12. The photoarray of any of the claims 10 or 11 wherein said row acknowledge lines and said column acknowledge lines are wired-or lines carrying signals from all cells (10) in their row or column, respectively.

13. The photoarray of any of the preceding claims wherein said sensor signal is proportional to a logarithm of the light intensity at said cell (10).

14. The photoarray of any of the preceding claims wherein each cell (10) comprises

a first threshold detector (T9 - T11) detecting if a voltage over said first capacitor (C1) exceeds a first, upper threshold value and generating a first output signal (ON) if yes and

a second threshold detector (T12 - T14) detecting if a voltage over said first capacitor (C1) falls below a second, lower threshold value and generating a second output signal (OFF) if yes.