Description

The present invention relates to apparatus for controlling a field or frame store signal processor in the presence of nonstandard video signals.

Field and frame store memories may be used in such video signal processing systems as comb filters, progressive scan systems and temporal noise reduction systems. In each of these systems, samples that are separated by a field or frame time are combined to produce processed samples. These systems are generally designed to operate on signals that are well correlated from field to field or from frame to frame. When video signals are not well correlated because of interfield motion or because the signals are produced by a nonstandard source, the performance of the field or frame memory signal processor may be degraded.

It is desirable to at least partially defeat the field or frame processing when a lack of correlation is detected to minimize degredation of the reproduced image. For example, many frame memory signal processing systems include motion detectors which modify or circumvent the frame memory processing steps for portions of the image that display moving objects.

As set forth above, signals from nonstandard sources, or nonstandard signals, may be poorly correlated from field to field or frame to frame. As used in this application, the term nonstandard signal means a color video signal in which the ratio of the chrominance subcarrier frequency, f_{sc}, to the horizontal line frequency, f_H, deviates significantly from the defined standard. This ratio may be critical for sampled data video signal processing systems, such as digital television receivers. In these systems, the sampling rate is usually chosen to be multiple of f_{sc} to take advantage of signal interrelationships dictated by the particular video signal standard. For example, in the NTSC standard, the frequency f_{sc} is the 455th harmonic of one-half of the line frequency f_H. Since f_{sc} is a harmonic of one-half f_H, there is a 180° phase shift in the chrominance signal from line to line and from frame to frame, while there is no phase shift in the luminance signal components. This relationship is exploited by frame and line comb filters to separate the luminance and chrominance components of the composite video signals. When composite video samples taken at a $4f_{sc}$ rate are subtracted from samples delayed by one line or one frame time, the luminance components of the samples tend to cancel, leaving only the chrominance components. Similarly, when samples separated by one line or one frame are added, the chrominance components tend to cancel leaving only the luminance components. For a frame comb filter to be effective, the samples from the two frames should be closely aligned. If misaligned samples are applied to a comb filter, the luminance and chrominance components of the samples may be uncorrelated and, consequently, the comb filter may produce distorted chrominance and luminance signals.

Sample misalignment from a field to field or from frame to frame may be a problem for other types of field or frame memory signal processors as well. For example, when the average ratio of f_{sc} to f_H does not match the standard ratio, as in some video games and personal computers, the image may skew from field to field. This skew may cause a field progressive scan system to display a jagged image and may cause a uniform loss of horizontal image resolution for signals processed by a recursive noise reducing filter.

Misalignment problems can occur, however, even when the average ratio of f_{sc} to f_H matches the standard ratio, if the instantaneous ratio changes significantly from line to line. For example, in video tape recorders (VTR's) and in video disk players the line frequency, f_H,is determined by the speed of the tape or disc while the subcarrier frequency, f_{sc}, is determined by a piezoelectric crystal. Because of imperfections in the tape or disk, f_H may vary significantly from line to line while f_{sc} remains relatively fixed. This variation in the ratio of f_{sc} to f_H may produce distortion on the edges of objects for images processed by a frame or field comb filter, it may randomly reduce the horizontal resolution of a temporal noise reducing system and it may cause a progressive scan system to display a jagged image.

Nonstandard signal detectors exist which will discriminate between broadcast and cable television signals, which conform closely to the standard, and nonstandard video game or personal computer signals. Many of these detectors, however, may not be able to detect nonstandard signals from VTR's and video disk players.

U.S. Patent US-A-4,335,403 entitled "Horizontal Countdown System For Television Receivers" discloses one type of nonstandard signal detector. This detector compares a "processed sync pulse", having a 280 ns pulse width with a "flyback center pulse" having a 560 ns pulse width. Assuming that a 70 ns overlap is needed to detect coincidence, this system allows signals which may deviate from the standard by as many as six 70 ns samples in a horizontal line to pass as standard signals. These signals could seriously degrade the performance of a field or frame signal processor.

Another nonstandard signal detector is described in U.S. Patent US-A-4,454,531 entitled "Digital Circuit For Providing A Binary Signal On The Occurrence Of A Predetermined Frequency Ratio Of Two Signals". The detector described in this reference uses a counter to derive a horizontal

line frequency pulse from a sampling clock signal which is fixed in frequency relative to the color subcarrier frequency. A monostable multivibrator, or one-shot, stretches these horizontal frequency pulses to be at least two clock periods wide. The stretched pulses are applied to the up/down input of a second counter and horizontal sync pulses, derived from the input signal, are applied to the clock input of the second counter. The second counter counts up for any horizontal sync pulse which falls within the window defined by the stretched horizontal line frequency pulse (i.e. for standard signals) and counts down for horizontal sync pulses which do not fall within this window (i.e. for nonstandard signals). If the value held by the second counter at the end of a field is above a predetermined threshold, the signals which generated the field are presumed to be standard and the value held by a third counter is incremented. If, however, the value held by the second counter at the end of a field falls below this threshold, the value held by the third counter is set to zero. When the value in the third counter reaches approximately 1000, the output signal of the detector changes to indicate that standard signals are being processed.

The 1000 field delay may make this detector unsuitable for use with a field or frame memory. A temporary loss of coincidence in an otherwise standard signals due to a change between two cameras, for example, may cause the detector to disable the field or frame memory processing, reducing the quality of the displayed image. In the NTSC system, the 1000 field delay would cause the low quality image to be displayed for 13 seconds before field or frame memory signal processing would be allowed to resume.

JP-A-59 23987 discloses a video signal processing system including a source of composite video signals which include line synchronizing and field synchronizing components. The system comprises furthermore: a nonstandard signal detector coupled to said source for developing a control signal which is in a first state when said line synchronizing component has a frequency which substantially conforms to a frequency determined by a ratio between line frequency and color subcarrier signal frequency (sampling clock which is chosen to be four times the frequency of the colour subcarrier) established for a predetermined video standard and which is in a second state otherwise; and a multi-mode video signal processor having first and second operating modes; wherein during the first operating mode, YC separation is performed by a comb line filter and during the second operating mode YC separation is performed by a band-pass filter.

According to the present invention, there is provided a video signal processing system including a source of composite video signals which include line synchronizing and field synchronizing components, said system comprising: a nonstandard signal detector coupled to said source for developing a control signal which is in a first state when said line synchronizing component has a frequency which substantially conforms to a frequency determined by a ratio between line frequency and color subcarrier signal frequency established for a predetermined video signal standard and which is in a second state otherwise; a multi-mode video signal processor having first and second operating modes; and means responsive to said control signal, for determining the mode of operation of said multi-mode video signal processor; characterized in that said processor includes memory means coupled to said source for storing at least one field of said composite video signal; and said processor, during operation in said first operating mode, effects a combination of signals from said source with stored prior field signals from said memory means to produce processed video signals; and said non-standard signal detector includes means for developing an indicating signal which changes from one state to another state substantially coincident with changes of said control signal from said first state to said second state, and which changes from said other state to said one state after said control signal has been in said first state for an integral number of periods of said vertical field synchronizing signal wherein said integral number of periods corresponds to the number of such periods required to fill said memory means; and said signal processor operates in said first operating mode when said indicating signal exhibits a said one state, and operates in said second operating mode when said indicating signal exhibits said other state.

For a better understanding of the present invention reference will now be made by way of example to the drawings, in which:

FIGURE 1 is a block diagram of a portion of a digital television signal processing system incorporating an embodiment of the present invention.

FIGURE 2 is a block diagram showing a nonstandard signal detector suitable for use in the embodiment shown in FIGURE 1.

FIGURE 3 is a block diagram of a digital retriggerable one-shot which may be used in the nonstandard signal detector shown in FIGURE 2.

FIGURE 4A is a block diagram showing an adaptive comb filter suitable for use as the multi-mode signal processor in the embodiment shown in FIGURE 1.

FIGURE 4B is a block diagram showing a recursive noise reducing filter suitable for use as the multi-mode signal processor in the embodiment of the invention shown in FIGURE 1.

FIGURE 4C is a block diagram showing an adaptive field progressive scan system suitable for use as the multi-mode signal processor in the embodiment of the invention shown in FIGURE 1.

In the drawings, broad arrows represent busses for multiple-bit parallel digital signals. Line arrows represent corrections carrying analog signals or single bit digital signals. Depending on the processing speed of the devices, compensating delays may be required in certain of the signal paths. One skilled in the art of digital circuit design would know where such delays would be needed in his particular system.

In FIGURE 1, a source of composite video signals 10, which may include the tuner, intermediate frequency amplifier and video detector of a conventional color television receiver, provides analog composite video signals to sync separator circuit 16. The sync separator 16 generates horizontal and vertical synchronization pulses and burst gate pulses from the analog composite video signals by conventional means. The horizontal synchronization pulses are applied to the horizontal phase locked loop (PLL) 20. PLL 20 produces a signal which is phase locked to the horizontal synchronization pulses from sync separator 16. Ideally, PLL 20 has a relatively wide lock-in range so that it may respond quickly to phase shifts in the horizontal synchronization pulses derived from the composite video signals. A suitable horizontal phase locked loop may be built from conventional components, such as the RCA CD4046A integrated circuit.

The primary function of PLL 20 is to provide relatively noise-free horizontal synchronization signals. In systems where noise immunity is not an important design consideration, the PLL 20 may be removed.

The phase-locked horizontal line frequency pulses from PLL 20 are applied to pulse forming circuitry which includes AND gate 19, delay element 21 and inverter 23. The output terminal of PLL 20 is connected to delay element 21 and to one input terminal of AND gate 19. Delay element 21 provides delayed pulses to inverter 23, the output terminal of which is connected to the second input terminal of AND gate 19. The pulses provided by AND gate 19 start at substantially the same time as the pulses from PLL 20 but have a pulse width approximately equal to the delay provided by delay element 21. In the present embodiment, this delay is less than 140 ns so that the signal HS, provided by AND gate 19, is a horizontal line frequency pulse signal that is phase-locked to the horizontal sync component of the received composite video signal and that has a relatively narrow pulse width (i.e. less than two periods of the $4f_{sc}$ clock signal).

The vertical synchronization pulses from sync separator 16 are applied to a conventional vertical frequency PLL 18 which produces a vertical synchronization signal, VS. Signal VS is locked in frequency and phase to the vertical synchronization pulses derived from the composite video signals by sync separator 16.

The burst gate signal, BG, is applied by sync separator 16 to a PLL 14 which produces a sampling clock signal that has a frequency four times the frequency of the color subcarrier signal and that is phase-locked to the color synchronizing burst component of the composite video signals. PLL 14 may be a conventional digitally controlled PLL similar to the one disclosed in U.S. Patent 4,291,332 entitled "Phase-Locked Circuit". The $4f_{sc}$ clocking signal provided by PLL 14 is applied to analog to digital converter (ADC) 12 to control the rate at which digital samples, representing the composite video signals from source 10, are produced by the ADC 12. Digital samples provided by ADC 12 are applied to PLL 14. PLL 14 uses the burst gate signal, BG, to extract from these composite video samples the color burst samples which are used to phase-lock the $4f_{sc}$ clock signals.

The horizontal and vertical synchronization signals, HS and VS and the $4f_{sc}$ clock signal are applied to nonstandard signal detector 22.

FIGURE 2 is a block diagram showing details of nonstandard signal detector 22. In this figure, the $4f_{sc}$ clock signal is applied to the count input terminal C of programmable down counter 210. An eight-bit digital value is applied to the preset input port P of counter 210 by digital value source 212, retriggerable one-shot 216 and inverter 218. As explained below, counter 210 may be preset to count down from one of two values. One of these values is used to change the phase of the horizontal sync signal provided by the down counter to align it to the phase of the received horizontal sync pulses. The other Value is used to produce a horizontal sync signal which conforms to the ratio between f_{sc} and f_H set by the applicable signal standard when the phases of the two signals are aligned.

When the counter 210 counts down to zero, it produces a logic high output signal. This signal is applied to the preset enable input terminal (PE) of the counter 210. The logic high signal applied to terminal PE sets the counter to the value applied to its preset input port synchronous with the leading edge of the next $4f_{sc}$ clock pulse. Since the counter value is no longer zero after it is preset, the counter produces a logic low output signal. Accordingly,

counter 210 produces output pulses that are approximately $1/(4f_{sc})$ wide at approximately one horizontal line (1H) time intervals.

The pulses from counter 210 are applied to one input terminal of AND gate 214. The horizontal sync signal, HS, from the AND gate 19 is applied to the other input terminal of AND gate 214. AND gate 214 is a coincidence detector. It produces an output pulse when the horizontal pulses from PLL 20 and from counter 210 overlap in time. This coincidence pulse is applied to the trigger input terminal, T, of horizontal retriggerable one-shot 216. One-shot 216 converts a coincidence pulse applied to its trigger input terminal into an output pulse that is a predetermined number of horizontal line periods wide. One-shot 216 is retriggerable, so that, once triggered, each subsequent coincidence pulse extends the output pulse of the one-shot by the predetermined number of horizontal line periods.

In the present embodiment, the output pulses provided by one-shot 216 are 25 horizontal line periods wide. Consequently, the output of the one-shot 216 maintains a logic high state if a coincidence is detected at least once in each 25 horizontal line intervals. This signal has been found to be a good indicator of standard or nonstandard signals; it is in a logic high state when the ratio between f_{sc} and f_H closely approximates the standard ratio and when the deviations about this ratio from line to line are minimal.

The output signal from one-shot 216 is inverted by inverter 218 and applied to the reset input terminals of the frequency divider 220 and the set-reset flip-flop 222. The vertical sync signal VS from PLL 18 is applied to the signal input terminal of frequency divider 220. Frequency divider 220, which frequency divides the field rate vertical sync signal by four, develops a signal that has a two-frame period and a 50% duty cycle. The output signal from frequency divider 220 is applied to the set input terminal of flip-flop 222.

When standard signals are being processed, the reset input signals to frequency divider 220 and flip-flop 222 are both in a logic low state and, after at least two fields of standard signal have been processed by the frequency divider 220, the set input signal to the flip-flop 222 is in a logic high state. Consequently, the signal provided by flip-flop 222 is in a logic high state.

When a nonstandard signal is detected, however, inverter 218 applies a logic high signal to the reset inputs of the frequency divider 220 and the flip-flop 222. This signal resets the frequency divider, changing the signal applied to the set input of the flip-flop 222 and the signal provided by the flip-flop to logic low signals. When the output signal from inverter 218 again changes to a logic low state, indicating that standard signals are being processed, the output signal from flip-flop 222 remains in a logic low state for one frame time. This delay allows the frame memory signal processing circuitry to store one frame of standard signals before frame processing is resumed.

As stated above, programmable down counter 210 may be preset to count down from one of two values. The six most significant bits of each of these values are supplied by source 212. The two least significant bits are supplied by inverter 218 and one-shot 216. In the present embodiment, the value provided by source 212 is $E3_{16}$ (227_{10}) (the subscripts 16 and 10 indicate hexadecimal and decimal notation respectively). When the two least significant bits are concatenated to this six bit value, preset values of $38D_{16}$ (909_{10}) and $38E_{16}$ - (910_{10}) are obtained, corresponding to the output signal of the one-shot being in a logic high and a logic low state respectively.

When the counter 210 is preset to 909, one pulse is emitted by the counter for every 910 pulses of the $4f_{sc}$ clock signal. The counter cycles every 910 instead of 909 clock pulses because it has a synchronous preset. After the counter has processed 909 clock pulses to count from 909 to zero, a logic high signal is applied to its preset enable input and synchronous with the next clock pulse, the 910th, the counter is preset to 909.

When the counter 210 is preset to 910, the counter cycles every 911 clock pulses and the signal provided by the counter 210 has a frequency slightly less than f_H. In this mode, the pulses produced by the counter 210 drift relative to the horizontal sync pulses until a pulse provided by the counter 210 coincides with a horizontal sync pulse from AND gate 19. It is contemplated that the rate of drift between the horizontal sync pulses and the pulses provided by the counter may be changed by changing the difference between the two count values or by changing the magnitude of the count values to change the period of the signals produced by the counter to be a multiple or a fraction of a horizontal line period.

As described above, one-shot 216 may be a conventional monostable multivibrator, having a pulse-width time constant determined by a resistor-capacitor (RC) network. FIGURE 3 shows an alternative implementation of the one-shot 216 which does not need an RC network. Horizontal sync pulses from PLL 20 are applied to the one-shot 216 as shown in phantom in FIGURE 2. These horizontal sync pulses are applied to one input terminal of AND gate 310. The output signal of the AND gate 310 is applied to the count input terminal, C, of counter 312. The output terminal of counter 312 is connected to the input terminal of inverter 314 which provides the output signal of the one-shot.

This output signal is applied to the second input terminal of AND gate 310. The trigger input terminal of the digital one-shot is the reset input terminal, R, of the counter 312.

When the output signal of the counter is in a logic high state (i.e. when the counter has counted to its maximum value), the output of inverter 314 is in a logic low state. The logic low signal from inverter 314 disables AND gate 310, so horizontal sync pulses are not applied to the count input terminal of the counter 312. When a pulse is applied to the reset terminal of counter 312, however, the output signal of the counter changes to a logic low state, and the inverter 314 applies a logic high signal to enable AND gate 310 to pass horizontal sync pulses. Counter 312 counts these pulses until it reaches its maximum value and once again disables the AND gate. In the present embodiment, the maximum value of the counter 312 is 25.

Referring again to FIGURE 1, the nonstandard signal detector 22 applies its output signal to field or frame memory processor 24. Processor 24 may, for example, include a comb filter, a recursive noise reducing filter or an interlaced scan to progressive scan conversion systems. Processor 24 processes the digitized composite video samples applied to it by ADC 12. In this embodiment of the invention, processor 24 provides separated luminance and chrominance signals, Y and C respectively to luminance/chrominance signal processor 26. Processor 26 may include circuitry to demodulate the C signal into color difference signals and circuitry to combine the color difference signals with the luminance signal to produce the primary color signals R, G and B. These primary color signals may be used to drive a display device (not shown).

FIGURE 4A is a block diagram of an adaptive frame comb filter which illustratively may be used to implement the function of processor 24 of FIG. 1. Composite video samples are simultaneously applied to a conventional frame comb filter 410 and to a conventional line comb filter 412. The luminance signals from the frame comb filter 410 and from the line comb filter 412 are applied to separate data input ports of multiplexer 414. Similarly, the chrominance signals from filters 410 and 412 are applied to separate data input ports of multiplexer 416. The signal provided by nonstandard signal detector 22 is applied to the control input terminals of multiplexers 414 and 416. Each of the multiplexers 414 and 416 is configured to pass the signal from the frame comb when the control signal is in a logic high state and to pass the signal from the line comb when the control signal is in a logic low state. As stated above, the control signal changes to a logic high state only after one frame of standard signals has been received. This allows the frame comb filter 410 to accumulate one frame of standard samples before frame memory processing is resumed.

FIGURE 4B is a block diagram of a recursive noise reducing filter illustrative of alternative apparatus for implementing the function of signal processor 24 of FIGURE 1. Composite video samples are applied to sample scaler 452 by ADC 12. Scaler 452 multiplies each of the samples by a scale factor K and applies the scaled samples to one input port of adder 454. Adder 454 adds these scaled samples to corresponding samples from frame store 458 that have been scaled by a factor of 1-K in sample scaler 460. The samples developed by adder 454 are applied to one data input port of multiplexer 450. Composite video samples from ADC 12 via delay element 448 are applied to the other data input terminal of multiplexer 450.

Delay element 448 provides compensating delay substantially equal to the processing time through sample scaler 452 and adder 454. The control signal applied to multiplexer 450 is the output signal provided by nonstandard signal detector 22. When this signal is in a logic high state, the multiplexer 450 applies the samples from adder 454 to the input port of Y/C separating filter 462. When the signal from detector 22 is in a logic low state, the multiplexer 450 applies the samples from delay element 448 to filter 462. Y/C separating filter 462 may extract the luminance and chrominance components from the composite video samples by conventional means providing a luminance signal Y and a chrominance signal C to luminance/chrominance processor 26.

Composite video samples from the multiplexer 450 are also applied to the input port of chroma inverter 456. The chroma inverter 456 inverts the chrominance components of these samples. The composite video samples provided by chroma inverter 456 are applied to the frame store 458. Frame store 458 may be a conventional shift register type frame memory. In an NTSC signal processing system, this memory may have 477,750 pixel storage locations.

Samples delayed by one frame time relative to the samples from ADC 12 are applied to the input port of sample scaler 460 by frame store 458. Sample scaler 460 multiplies these samples by a factor of 1-K. These scaled samples are added to the samples provided by sample scaler 452. The chrominance signal phases of the samples from scalers 452 and 460 are the same because the chroma inverter 456 reverses the phase of the frame delayed samples before applying them to the frame store.

Sample scalers 452 and 460, adder 454, chroma inverter 456 and frame store 458 constitute a conventional one-frame recursive noise reducing

filter. A more detailed description of this filter can be found in the article by McMann et al. entitled "A Digital Noise Reducer For Encoded NTSC Signals", SMPTE Journal, Vol. 87, No. 3, pp. 129-133 (March, 1978).

FIGURE 4C is a block diagram of an adaptive interlace scan to progressive scan conversion system which uses a field store memory, providing an additional example of apparatus suitable for implementing the function of processor 24 of FIG. 1. An interlace scan to progressive scan conversion system may be used, for example, in a television receiver to reduce the loss of vertical resolution and frame-rate flicker artifacts of an interlaced scan signal. Systems which display a progressive scan image double the number of lines in each field and the rate at which the lines processed to display a full image frame during each field period. Two types of progressive scan systems that are known in the art are field progressive scan systems and line progressive scan systems.

A typical field progressive scan system is described in U.S. Patent 4,426,661 entitled "Television Receiver Including A Circuit For Doubling Line Scanning Frequency" which is hereby incorporated by reference. In this system, composite video signals are delayed one field time and applied along with undelayed signals to a speed-up circuit. The speed-up circuit doubles the scan rate of each of the signals and inserts the field-delayed lines in-between the undelayed lines. This signal is displayed at twice the rate of the interlaced signal to provide a progressive scan image.

U.S. Patent 4,415,931 entitled "Television Display With Doubled Horizontal Lines", hereby incorporated by reference, describes a line progressive scan system. In this system, each line of each field is displayed twice in a single field time. This system increases the number of lines in each field but may not provide the same vertical resolution as a field progressive scan system. However, a line progressive scan system may produce a better image than a field progressive scan system when nonstandard signals are being processed. The field-to-field correlation errors which may occur in nonstandard signals may cause a field progressive scan system to display a jagged image while causing almost no distortion in a line progressive scan system.

In FIGURE 4C, composite video signals from ADC 12 are applied to both the field progressive scan system 470 and to the line progressive scan system 472. The double-rate signals provided by systems 470 and 472 are applied to the two data input ports of multiplexer 474. The control signal input terminal, of multiplexer 474 is coupled to nonstandard signal detector 22. Multiplexer 474 is configured to pass the double-rate signal from the field progressive scan system 470 when the control signal from detector 22 is in a logic high state and to pass the signal from the line progressive scan system 472 otherwise. The signal provided by multiplexer 474 is applied to Y/C separation filter 476, which may separate the luminance and chrominance components from the composite video samples by conventional means to provide a luminance signal, Y, and a chrominance signal, C, to luminance/chrominance processor 26.

Although an illustrative embodiment of the invention has been shown in a digital color television signal processing system including a field or frame memory processor, it is contemplated that the invention may also be practiced in an analog system which uses a charge-coupled device (CCD) or delay line field or frame store memory. It is also contemplated that the invention may be used in systems which store frames or fields of processed video signals as well as in systems which store composite video signals.

Claims

1. A video signal processing system including a source (10) of composite video signals which include line synchronizing and field synchronizing components, said system comprising:

a nonstandard signal detector (22) coupled to said source for developing a control signal which is in a first state when said line synchronizing component has a frequency which substantially conforms to a frequency determined by a ratio between line frequency and color subcarrier signal frequency established for a predetermined video signal standard and which is in a second state otherwise;

a multi-mode video signal processor (24) having first and second operating modes; and

means (414,416; 450; 474) responsive to said control signal, for determining the mode of operation of said multi-mode video signal processor;

characterized in that

said processor includes memory means (410,458,470) coupled to said source for storing at least one field of said composite video signal; and

said processor, during operation in said first operating mode, effects a combination of signals from said source with stored prior field signals said memory means to produce processed video signals; and

said non-standard signal detector includes means (216,218,220,222) for developing an indicating signal which changes from one state to another state substantially coincident with changes of said control signal from said first

filter. A more detailed description of this filter can be found in the article by McMann et al. entitled "A Digital Noise Reducer For Encoded NTSC Signals", SMPTE Journal, Vol. 87, No. 3, pp. 129-133 (March, 1978).

FIGURE 4C is a block diagram of an adaptive interlace scan to progressive scan conversion system which uses a field store memory, providing an additional example of apparatus suitable for implementing the function of processor 24 of FIG. 1. An interlace scan to progressive scan conversion system may be used, for example, in a television receiver to reduce the loss of vertical resolution and frame-rate flicker artifacts of an interlaced scan signal. Systems which display a progressive scan image double the number of lines in each field and the rate at which the lines processed to display a full image frame during each field period. Two types of progressive scan systems that are known in the art are field progressive scan systems and line progressive scan systems.

A typical field progressive scan system is described in U.S. Patent 4,426,661 entitled "Television Receiver Including A Circuit For Doubling Line Scanning Frequency" which is hereby incorporated by reference. In this system, composite video signals are delayed one field time and applied along with undelayed signals to a speed-up circuit. The speed-up circuit doubles the scan rate of each of the signals and inserts the field-delayed lines in-between the undelayed lines. This signal is displayed at twice the rate of the interlaced signal to provide a progressive scan image.

U.S. Patent 4,415,931 entitled "Television Display With Doubled Horizontal Lines", hereby incorporated by reference, describes a line progressive scan system. In this system, each line of each field is displayed twice in a single field time. This system increases the number of lines in each field but may not provide the same vertical resolution as a field progressive scan system. However, a line progressive scan system may produce a better image than a field progressive scan system when nonstandard signals are being processed. The field-to-field correlation errors which may occur in nonstandard signals may cause a field progressive scan system to display a jagged image while causing almost no distortion in a line progressive scan system.

In FIGURE 4C, composite video signals from ADC 12 are applied to both the field progressive scan system 470 and to the line progressive scan system 472. The double-rate signals provided by systems 470 and 472 are applied to the two data input ports of multiplexer 474. The control signal input terminal, of multiplexer 474 is coupled to nonstandard signal detector 22. Multiplexer 474 is configured to pass the double-rate signal from the field progressive scan system 470 when the control signal from detector 22 is in a logic high state and to pass the signal from the line progressive scan system 472 otherwise. The signal provided by multiplexer 474 is applied to Y/C separation filter 476, which may separate the luminance and chrominance components from the composite video samples by conventional means to provide a luminance signal, Y, and a chrominance signal, C, to luminance/chrominance processor 26.

Although an illustrative embodiment of the invention has been shown in a digital color television signal processing system including a field or frame memory processor, it is contemplated that the invention may also be practiced in an analog system which uses a charge-coupled device (CCD) or delay line field or frame store memory. It is also contemplated that the invention may be used in systems which store frames or fields of processed video signals as well as in systems which store composite video signals.

Claims

1. A video signal processing system including a source (10) of composite video signals which include line synchronizing and field synchronizing components, said system comprising:

a nonstandard signal detector (22) coupled to said source for developing a control signal which is in a first state when said line synchronizing component has a frequency which substantially conforms to a frequency determined by a ratio between line frequency and color subcarrier signal frequency established for a predetermined video signal standard and which is in a second state otherwise;

a multi-mode video signal processor (24) having first and second operating modes; and

means (414,416; 450; 474) responsive to said control signal, for determining the mode of operation of said multi-mode video signal processor;

characterized in that

said processor includes memory means (410,458,470) coupled to said source for storing at least one field of said composite video signal; and

said processor, during operation in said first operating mode, effects a combination of signals from said source with stored prior field signals said memory means to produce processed video signals; and

said non-standard signal detector includes means (216,218,220,222) for developing an indicating signal which changes from one state to another state substantially coincident with changes of said control signal from said first

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state to said second state, and which changes from said other state to said one state after said control signal has been in said first state for an integral number of periods of said vertical field synchronizing signal wherein said integral number of periods corresponds to the number of such periods required to fill said memory means; and

said signal processor (24) operates in said first operating mode when said indicating signal exhibits a said one state, and operates in said second operating mode when said indicating signal exhibits said other state.

2. A system in accordance with claim 1, wherein said integral number is two.

3. A system in accordance with claim 1 or 2 wherein:

said signal processor (Fig. 4A) comprises (1) a frame comb filter (410) including said memory means (410) for separating luminance and chrominance signal components from said composite video signals, and (2) alternative means (412) comprising a line comb filter, for separating the luminance and chrominance signal components of said composite video signals; and

wherein said frame comb filter (410) is enabled when said processor operates in said first operating mode, and said alternative separating means (412) is enabled when said processor operates in a second operating mode.

4. A system as set forth in claim 1 or 2 wherein said memory means (458), of the signal processor (Fig. 4B) has an input port and an output port and a sufficient number of cells to store at least one frame of composite video signals;

and the signal processor further comprises

means (454) coupled to said source of composite video signals and to the output port of said memory means, for combining composite video signals from said source with stored composite video signals from said memory means to produce temporally averaged composite video signals;
and

means (450) for delivering said temporally averaged composite video signals to said input port of said memory means.

5. A system as set forth in claim 4 wherein the output of said processor (Fig. 4B) is derived from said combining means (454) when the indicating signal is in said one state.

6. A system as set forth in claim 1 wherein:

the memory means (470) is coupled to said source for storing at least one field of said composite video signals;

and the signal processor (Fig. 4C) further comprises

main scan converting means (470) coupled to said memory means (470) and to said source for combining said stored signals with signals from said source to produce progressive scan signals; and

alternative scan converting means (472), coupled to said source and not including a field memory, for converting said composite video signals into progressive scan signals; and

wherein the output of said signal processor is derived from said main scan converting means (470) when it operates in the said first operating mode, and from said alternative scan converting means (472) when it operates in the said second operating mode.

Revendications

1. Système de traitement de signaux vidéo comportant une source (10) de signaux vidéo composites qui comprennent des composantes de synchronisation de lignes et des composantes de synchronisation de champ, ledit système comprenant :

un détecteur de signaux non standard (22) couplé à ladite source pour développer un signal de commande qui est dans un premier état lorsque ladite composante de synchronisation de lignes possède une fréquence qui est sensiblement conforme à une fréquence déterminée par un rapport entre la fréquence de lignes et la fréquence du signal sous-porteur de couleurs, établi pour un standard de signaux vidéo prédéterminé et qui autrement est dans un second état ;

un processeur de signaux vidéo multimode (24) présentant des premier et second modes opératoires de fonctionnement ;
et

des moyens (414, 416 ; 450 ; 474) agissant en réponse auxdits signaux vidéo pour déterminer le mode de fonctionnement du processeur de signaux vidéo multimode ;

caractérisé en ce que

ledit processeur comprend des moyens de mémoire (410, 458, 470) couplés à ladite source pour stocker au moins un champ dudit signal vidéo composite ; et

ledit processeur, lors du fonctionnement selon ledit premier mode opératoire, effectue une combinaison de signaux à partir de ladite

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source avec des signaux de champ préalablement stockés à partir desdits moyens de mémoire afin de produire des signaux vidéo traités et

ledit détecteur de signaux non standard comprend des moyens (216, 218, 220, 222) pour développer un signal d'indication qui change d'un état à un autre état, sensiblement en coïncidence avec des changements dudit signal de commande dudit premier état audit second état et qui change de cet autre état vers ledit premier état, après que ledit signal de commande ait été dans ledit premier état, pendant un nombre entier de périodes dudit signal de synchronisation de champ vertical, dans lequel ledit nombre entier de périodes correspond au nombre de telles périodes nécessaires au remplissage desdits moyens de mémoire ; et

ledit processeur de signal (24) fonctionne selon ledit premier mode opératoire lorsque ledit signal d'indication présente l'un de ses états et fonctionne selon ledit second mode opératoire lorsque ledit signal d'indication présente l'autre état.

2. Système selon la revendication 1 dans lequel ledit nombre entier est le chiffre 2.

3. Système selon la revendication 1 ou 2 dans lequel :

ledit processeur de signaux (Fig. 4A) comprend (1) un filtre à encoches de trame (410) incluant lesdits moyens de mémoire (410) pour séparer desdits signaux vidéo composites les composantes de signal de luminence et de chrominance et (2) des moyens alternatifs (412) comprenant un filtre à encoches de lignes, pour séparer desdits signaux vidéo composites les composantes de signal de luminence et de chrominance ; et

dans lequel ledit filtre à encoches de trame (410) est activé lorsque ledit processeur fonctionne selon ledit premier mode opératoire et lesdits moyens de séparation alternatifs (412) sont activés lorsque ledit processeur fonctionne selon ledit second mode opératoire.

4. Système selon la revendication 1 ou 2 dans lequel lesdits moyens de mémoire (458) du processeur de signaux (Fig. 4B) possèdent un point d'accès d'entrée et un point d'accès de sortie et un nombre suffisant de cellules pour stocker au moins une trame de signaux vidéo composites ;

et ledit processeur de signaux comprend en outre

des moyens (454) couplés à ladite source de signaux vidéo composites et au point d'accès de sortie desdits moyens de mémoire, pour combiner des signaux vidéo composites provenant de ladite source avec des signaux vidéo composites stockés à partir desdits moyens de mémoire, pour produire des signaux vidéo composites temporairement de valeur moyenne ; et

des moyens (450) pour délivrer lesdits signaux vidéo composites temporairement de valeur moyenne audit point d'accès d'entrée desdits moyens de mémoire.

5. Système selon la revendication 4 dans lequel la sortie dudit processeur (Fig. 4B) est dérivée desdits moyens de combinaison (454) lorsque le signal d'indication est dans l'un de ses dits états.

6. Système selon la revendication 1 selon lequel

lesdits moyens de mémoire (470) sont couplés à ladite source pour stocker au moins un champ desdits signaux vidéo composites ;

et le processeur de signaux (Fig. 4C) comprend en outre

des moyens principaux de transformation de balayage (470) couplés auxdits moyens de mémoire (470) et à ladite source pour combiner lesdits signaux stockés avec des signaux provenant de ladite source afin de produire des signaux de balayage progressif ; et

des moyens de transformation de balayage alternatifs (472), couplés à ladite source et ne comprenant pas de mémoire de champ, pour transformer lesdits signaux vidéo composites en signaux de balayage progressif ; et

dans lequel la sortie dudit processeur de signal est dérivée desdits moyens principaux de transformation de balayage (470) lorsqu'il fonctionne selon ledit premier mode opératoire, et desdits moyens alternatifs de transformation de balayage (472) lorsqu'il fonctionne selon ledit second mode opératoire.

Patentansprüche

1. Videosignalaufbereitungssystem mit einer Quelle (10) zusammengesetzter Videosignale, welche Zeilensynchron- und Teilbildsynchron-Anteile enthalten, wobei das System das folgende umfaßt:

einen mit der Quelle verbundenen Detektor für nicht genormte Signale (22) zum Erzeugen eines Steuersignals, welches sich in einem ersten Zustand befindet, wenn der Zeilensynchronanteil eine Frequenz aufweist, die im wesentlichen mit einer Frequenz übereinstimmt,

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die von einem für eine vorgegebene Videosignalnorm bekannten Verhältnis zwischen Zeilenfrequenz und Farbträgersignal-Frequenz bestimmt ist, und das sich anderenfalls in einem zweiten Zustand befindet;

einen für mehrfache Betriebsmodi vorgesehenen Videosignalprozessor (24) mit ersten und zweiten Betriebsarten; und

Mitteln (414, 416; 450; 474), die auf das Steuersignal reagieren, zum Bestimmen der Betriebsart des für mehrfache Betriebsmodi vorgesehenen Videosignalprozessors;

dadurch gekennzeichnet, daß

der Prozessor mit der Quelle verbundene Speichermittel (410, 458, 470) zum Speichern von mindestens einem Teilbild des zusammengesetzten Videosignals enthält; und

daß der Prozessor, während er in der ersten Betriebsart arbeitet, ein Zusammensetzen von Signalen von der Quelle mit gespeicherten Signalen eines vorhergehonden Teilbildes aus dem Speicher bewirkt, um aufbereitete Videosignale zu erzeugen; und

daß der Detektor für nicht genormte Signale Mittel (216, 218, 220, 222) zum Erzeugen eines Indikatorsignals enthält, welches, im wesentlichen übereinstimmend mit den Wechseln des Steuersignales von dem ersten zu dem zweiten Zustand, von einem Zustand in einen anderen Zustand wechselt und von dem anderen Zustand in den einen Zustand wechselt, nachdem das Steuersignal für eine ganze Zahl von Perioden des vertikalen Teilbildsynchronsignals den ersten Zustand innehatte, wobei die ganze Zahl von Perioden der Anzahl solcher Perioden entspricht, die benötigt wird, die Speichermittel zu füllen; und

daß der Signalprozessor (24) in der ersten Betriebsart arbeitet, wenn das Indikatorsignal den einen Zustand zeigt, und in der zweiten Betriebsart arbeitet, wenn das Indikatorsignal den anderen Zustand zeigt.

2. System gemäß Anspruch 1, wobei die ganze Zahl zwei beträgt.

3. System gemäß Anspruch 1 oder 2, wobei:

der Signalprozessor (Fig. 4A) (1) ein Vollbild-Kammfilter (410) mit den Speichermitteln (410) zum Trennen von Luminanz- und Chrominanzsignal-Anteilen aus den zusammengesetzten Videosignalen und (2) alternative Mittel (412) mit einem Zeilen-Kammfilter zum Trennen der Luminanz- und Chrominanzsignal-Anteile der zusammengesetzten Videosignale enthält; und

wobei das Vollbild-Kammfilter (410) eingeschaltet wird, wenn der Prozessor in der ersten Betriebsart arbeitet, und die alternativen Mittel (412) eingeschaltet werden, wenn der Prozessor in einer zweiten Betriebsart arbeitet.

4. System wie in Anspruch 1 oder 2 angegeben, wobei die Speichermittel (458) des Signalprozessors (Fig. 4B) einen Eingangsport und einen Ausgangsport sowie eine hinreichende Anzahl von Zellen zum Speichern von mindestens einem Vollbild der zusammengesetzten Videosignale aufweist;

und der Signalprozessor weiterhin umfaßt:

mit der Quelle zusammengesetzter Videosignale und dem Ausgangsport der Speichermittel verbundene Mittel (454) zum Zusammensetzen zusammengesetzter Videosignale von der Quelle mit gespeicherten zusammengesetzten Videosignalen von den Speichermitteln zum Erzeugen zeitlich gemittelter zusammengesetzter Videosignale; und

Mittel (450) zum Liefern der zeitlich gemittelten zusammengesetzten Videosignale zu dem Eingangsport der Speichermittel.

5. System wie in Anspruch 4 angegeben, wobei das Ausgangssignal des Prozessors (Fig. 4B) von den Mitteln zum Zusammensetzen (454) abgeleitet wird, wenn sich das Indikatorsignal in dem einen Zustand befindet.

6. System wie in Anspruch 1 angegeben, wobei:

die Speichermittel (470) mit der Quelle verbunden sind, um mindestens ein Teilbild der zusammengesetzten Videosignale zu speichern;

und der Signalprozessor (Fig. 4C) weiterhin umfaßt:

mit den Speichermitteln (470) und der Quelle verbundene Haupt-Abtastwandlungsmittel (470) zum Zusammensetzen der gespeicherten Signale mit Signalen von der Quelle, um progressive Abtastsignale zu erzeugen; und

alternative Abtastwandlungsmittel (472), welche

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mit der Quelle verbunden sind und keinen Teilbildspeicher enthalten, zum Wandeln der zusammengesetzten Videosignale in progressive Abtastsignale; und

wobei das Ausgangssignal des Signalprozessors von den Haupt-Abtastwandlungsmitteln (470) abgeleitet wird, wenn er in der ersten Betriebsart arbeitet, und von den alternativen Abtastwandlungsmitteln (472), wenn er in der zweiten Betriebsart arbeitet.

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