D E S C R I P T I O N

SUBSTRATE PROCESSING METHOD AND STORAGE MEDIUM

Technical Field

[0001]

The present invention relates to a substrate processing method for performing a denaturing process for denaturing a predetermined substance and a process for dissolving and removing the denatured substance, in manufacturing a semiconductor device by use of, e.g., a dual damascene method. The present invention also relates to a storage medium that stores a program for executing a method of this kind.

Background Art

[0002]

In semiconductor devices, a decrease in the interconnection line space due to miniaturization brings about a larger capacitance between interconnection lines, which makes the signal propagation rate lower, thereby resulting in a delay in operation speed. In order to solve this problem, developments are being made in insulative materials (Low-k materials) with a low specific dielectric constant (k-value), and multi-layer interconnection lines using such insulative materials. On the other hand, copper is attracting attentions as an interconnection line material, because it has a low resistivity and a high electro-migration resistance.

Where copper is used for forming interconnection lines in grooves and/or connection holes, a single damascene method and/or a dual damascene method are frequently used.

[0003]

FIG. 1 is an explanatory view for explaining the serial steps of a process for forming a multi-layer cupper interconnection line, using a dual damascene method. On a silicon substrate (not shown), there is disposed a low dielectric constant film (Low-k film) 200, which is an insulating film made of a Low-k material. At first, a lower interconnection line 202 made of copper is formed in the insulating film 200 with a barrier metal layer 201 interposed therebetween. Then, a Low-k film 204 used as an inter-level insulating film is formed thereon with an etching stopper film 203 interposed therebetween. Then, an anti-reflective coating (BARC: Bottom Anti-Reflective Coating) 205 and a resist film 206 are formed in this order on the surface of the Low-k film 204. Then, the resist film 206 is subjected to light exposure with a predetermined pattern and is then development, so that a circuit pattern is formed on the resist film 206 (step (a)).

[0004]

Then, using the resist film 206 as a mask, the Low-k film 204 is etched to form a via-hole 204a (step

(b)). Then, the anti-reflective coating 205 and resist film 206 are removed by, e.g., a chemical liquid process and an ashing process. Then, a sacrificial film 207 is formed on the surface of the insulating film 204 including the via-hole 204a (step (c)). At this time, the via-hole 204a is filled with the sacrificial film 207.

[0005]

Then, a resist film 208 is formed on the surface of the sacrificial film 207. Then, the resist film 208 is subjected to light exposure with a predetermined pattern and is then development, so that a circuit pattern is formed on the resist film 208 (step (d)). Then, using the resist film 208 as a mask, the sacrificial film 207 and Low-k film 204 are etched to form a wider trench 204b on the via-hole 204a (step (e)). Then, the resist film 208 and sacrificial film 207 are removed to complete the via-hole 204a and trench 204b in the insulating film 204 (step (f)). Then, the via-hole 204a and trench 204b are filled with copper as an upper interconnection line.

[0006]

Incidentally, the sacrificial film 207 is sometimes made of an Si-O based inorganic material, which is difficult to remove by the conventional ashing process used for removing a resist film. There is a case where a chemical liquid is used to dissolve a film

of this kind, but the processing rate is very low.

[0007]

As a technique for removing a sacrificial film of this kind, there is proposed a method in which a process gas containing water vapor and ozone is used to denature the sacrificial film to be soluble in a predetermined chemical liquid, and then the sacrificial film is removed by the chemical liquid (Jpn. Pat. Appln. KOKAI Publication No. 2004-214388).

[0008]

However, where a process gas containing water vapor and ozone is used to perform a liquid-solubilization process, as described above, and then a chemical liquid is used to perform a cleaning process, a Low-k material may be damaged and thereby increase the specific dielectric constant thereof. This may deteriorate effects obtained by use of the Low-k material as an inter-level insulating film.

[0009]

In this respect, as a technique for recovering damage of this kind, Jpn. Pat. Appln. KOKAI Publication No. 2006-049798 discloses a method for performing a silylation process after etching or resist film removal. This silylation process is arranged to reform damaged surface portions by a silylation agent, thereby forming end groups of alkyl groups, such as methyl groups. This technique may be applied also to a process for

recovering damage after the cleaning process or denaturing process described above.

[0010]

However, even where the silylation process is performed after the cleaning process or denaturing process, recovery of the k-value is insufficient, as the case may be.

Disclosure of Invention

[0011]

An object of the present invention is to provide a substrate processing method that can sufficiently recover the k-value of a low dielectric constant film, even where the k-value is increased due to damage caused to the film by a denaturing process and a subsequent dissolving process.

Another object of the present invention is to provide a storage medium that stores a program for executing the substrate processing method.

[0012]

According to a first aspect of the present invention, there is provided a substrate processing method comprising: performing an etching process on a low dielectric constant film disposed on a substrate, thereby forming a predetermined pattern thereon; denaturing a remaining substance to be soluble in a predetermined liquid after the etching process; dissolving and removing the substance thus denatured,

by supplying the predetermined liquid thereon; then, performing a silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and baking the substrate after the silylation process.

[0013]

According to a second aspect of the present invention, there is provided a substrate processing method comprising: forming a sacrificial film on a low dielectric constant film disposed on a substrate; forming an etching mask on the sacrificial film, and etching the sacrificial film and the low dielectric constant film, thereby forming a predetermined pattern thereon; denaturing the sacrificial film and the etching mask to be soluble in a predetermined liquid; dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon; then, performing a silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and baking the substrate after the silylation process.

[0014]

In the first and second aspects, after said denaturing a remaining substance and before said dissolving and removing the substance denatured, the

method may further comprise performing a silylation process on a surface of the low dielectric constant film with the pattern formed thereon. The low dielectric constant film preferably comprises a porous low dielectric constant material. The low dielectric constant film may include alkyl groups as end groups.

[0015]

Further, said denaturing a remaining substance may comprise supplying a process gas containing water vapor and ozone. Alternatively, said denaturing a remaining substance may comprise supplying a process gas containing ozone. The predetermined liquid may comprise an acidic or alkaline chemical liquid.

[0016]

Further, the silylation agent used for the silylation process may comprise a compound including silazane bonds (Si-N) in molecules. The compound including silazane bonds in molecules may be selected from the group consisting of TMDS (1,1,3,3-Tetramethyldisilazane), TMSDMA (Dimethylaminotrimethylsilane), and DMSDMA (Dimethylsilyldimethylamine).

[0017]

Furthermore, said baking the substrate is preferably performed at a temperature higher than a temperature used for the silylation process. Specifically, said baking the substrate is preferably

performed at a temperature of 150 to 400℃. In addition, the method may further comprise performing a baking process before the silylation process.

[0018]

According to a third aspect of the present invention, there is provided a substrate processing method to be performed on a substrate including an etching target film, which has been prepared by performing an etching process on the etching target film, thereby forming a predetermined pattern thereon, then denaturing a remaining substance to be soluble in a predetermined liquid after the etching process, and then dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon, the method comprising: performing a silylation process on a surface of the etching target film by supplying a silylation agent thereon; and baking the substrate after the silylation process.

[0019]

According to a fourth aspect of the present invention, there is provided a storage medium that stores a program for execution on a computer to control a substrate processing system, wherein the program, when executed, causes the computer to control the substrate processing system to conduct a substrate processing method comprising: performing an etching process on a low dielectric constant film disposed on a

substrate, thereby forming a predetermined pattern thereon; denaturing a remaining substance to be soluble in a predetermined liquid after the etching process; dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon; then, performing a silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and baking the substrate after the silylation process.

[0020]

According to a fifth aspect of the present invention, there is provided a storage medium that stores a program for execution on a computer to control a substrate processing system, wherein the program, when executed, causes the computer to control the substrate processing system to conduct a substrate processing method comprising: forming a sacrificial film on a low dielectric constant film disposed on a substrate; forming an etching mask on the sacrificial film, and etching the sacrificial film and the low dielectric constant film, thereby forming a predetermined pattern thereon; denaturing the sacrificial film and the etching mask to be soluble in a predetermined liquid; dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon; then, performing a

silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and baking the substrate after the silylation process.

[0021]

According to a sixth aspect of the present invention, there is provided a storage medium that stores a program for execution on a computer to control a substrate processing system, wherein the program, when executed, causes the computer to control the substrate processing system to conduct a substrate processing method to be performed on a substrate including an etching target film, which has been prepared by performing an etching process on the etching target film, thereby forming a predetermined pattern thereon, then denaturing a remaining substance to be soluble in a predetermined liquid after the etching process, and then dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon, the method comprising: performing a silylation process on a surface of the etching target film by supplying a silylation agent thereon; and baking the substrate after the silylation process.

[0022]

According to the present invention, after the

denaturing process and dissolving process are performed in this order, the silylation process is performed and then substrate baking is further performed. Consequently, the low dielectric constant film that has a specific dielectric constant (k-value) decreased due to damage thereto is processed such that the k-value is sufficiently recovered. Specifically, after the dissolving process, moisture is contained in the low dielectric constant film, and then this moisture reacts with the silylation agent to generate an Si-containing by-product. This Si-containing by-product has a high k-value in itself, and prevents the k-value from being sufficiently decreased even if the silylation process is performed to recover damage by forming end groups of alkyl groups, such as methyl groups. Particularly, where the low dielectric constant film is porous, a lot of moisture is contained in pores, so the Si-containing by-product is generated inside the film and makes the problem described above notable. In light of this, according to the present invention, the baking process is performed to decompose and remove the Si-containing by-product. Consequently, the low dielectric constant film is free from the Si-containing by-product that increases the k-value, so the k-value of the low dielectric constant film is sufficiently recovered.

Brief Description of Drawings

[0023]

[FIG. 1] This is an explanatory view for explaining the serial steps of a process for forming a multi-layer cupper interconnection line, using a conventional dual damascene method.

[FIG. 2] This is an explanatory view schematically showing the arrangement of a wafer processing system used for a semiconductor device manufacturing process employing a dual damascene method, to which a substrate processing method according to an embodiment of the present invention is applied.

[FIG. 3] This is a plan view schematically showing the structure of a cleaning apparatus used in the wafer processing system shown in FIG. 2.

[FIG. 4] This is a front view schematically showing the structure of the cleaning apparatus used in the wafer processing system shown in FIG. 2.

[FIG. 5] This is a back view schematically showing the structure of the cleaning apparatus used in the wafer processing system shown in FIG. 2.

[FIG. 6] This is a sectional view schematically showing a denaturing unit disposed in the cleaning apparatus.

[FIG. 7] This is a sectional view schematically showing a silylation unit disposed in the cleaning apparatus.

[FIG. 8] This is a sectional view schematically showing a cleaning unit disposed in the cleaning

apparatus.

[FIG. 9] This is a sectional view schematically showing a hot plate unit disposed in the cleaning apparatus.

[FIG. 10] This is a flowchart showing a semiconductor device manufacturing process employing a dual damascene method, to which a substrate processing method according to an embodiment of the present invention is applied.

[FIG. 11] This is an explanatory view for explaining states appearing in steps of the flowchart shown in FIG. 10.

[FIG. 12] This is a view for explaining damage of a Low-k film and recovery thereof by silylation.

Best Mode for Carrying Out the Invention

[0024]

An embodiment of the present invention will now be described with reference to the accompanying drawings. Hereinafter, the present invention is exemplified by a case where a semiconductor device is manufactured by a dual damascene method.

[0025]

FIG. 2 is an explanatory view schematically showing the arrangement of a wafer processing system used for a semiconductor device manufacturing process employing a dual damascene method, to which a substrate processing method according to an embodiment of the

present invention is applied. This wafer processing system includes a process section 100 and a main control section 110. The process section 100 includes an SOD (Spin On Dielectric) apparatus 101, a resist coating/development apparatus 102, a light exposure apparatus 103, a cleaning apparatus 104, an etching apparatus 105, a sputtering apparatus 106 used as a PVD apparatus, an electrolytic plating apparatus 107, and a CMP apparatus 109 used as a polishing apparatus. The main control section 110 includes a process controller 111, a user interface 112, and a storage portion 113. The SOD apparatus 101, sputtering apparatus 106, and electrolytic plating apparatus 107 of the process section 100 is film formation apparatuses. As a method for transferring a wafer W between apparatuses in the process section 100, a transfer method by an operator and/or a transfer method by a transfer unit (not shown) are used.

[0026]

Each of the apparatuses in the process section 100 is connected to and controlled by the process controller 111 having a CPU. The process controller 111 is connected to the user interface 112, which includes, e.g., a keyboard and a display, wherein the keyboard is used for a process operator to input commands for operating the apparatuses in the process section 100, and the display is used for showing

visualized images of the operational status of the apparatuses in the process section 100. Further, the process controller 111 is connected to the storage portion 113, which stores recipes with control programs and process condition data recorded therein, for realizing various processes performed in the process section 100 under the control of the process controller 111.

[0027]

A required recipe is retrieved from the storage portion 113 and executed by the process controller 111 in accordance with an instruction or the like through the user interface 112, as needed. Consequently, each of various predetermined processes is performed in the process section 100 under the control of the process controller 111. Recipes may be stored in a readable storage medium, such as a CD-ROM, hard disk, flexible disk, or nonvolatile memory. Further, recipes may be utilized on-line, while it is transmitted among the respective apparatuses in the process section 100, or transmitted from an external apparatus through, e.g., a dedicated line, as needed.

In place of the global control by the main control section 110, or along with the global control by the main control section 110, each of the apparatuses in the process section 100 may be provided with and controlled by its own control section including a

process controller, a user interface, and a storage portion.

[0028]

The SOD apparatus 101 is used to apply a chemical liquid onto a wafer W to form an inter-level insulating film formed of, e.g., a Low-k film, or an etching stopper film by a spin coating method. Although the structure of the SOD apparatus 101 is not shown in detail, the SOD apparatus 101 includes a spin coater unit and a heat processing unit to perform a heat process on a wafer W with a coating film formed thereon. In the case of a wafer processing system, a CVD apparatus may be used to form an insulating film on a wafer W by a chemical vapor deposition (CVD) method, in place of the SOD apparatus 101.

[0029]

The resist coating/development apparatus 102 is used to form a resist film used as an etching mask, and an anti-reflective coating. Although the resist coating/development apparatus 102 is not shown in detail, the resist coating/development apparatus 102 includes a resist coating unit, a BARC coating unit, a sacrificial film coating unit, a developing unit, and thermal processing units. The resist coating unit is arranged to apply a resist liquid onto a wafer W to form a resist film by spin coating. The BARC coating unit is arranged to apply an anti-reflective coating

(BARC) onto a wafer W. The sacrificial film coating unit is arranged to apply a sacrificial film (SLAM) onto a wafer W. The developing unit is arranged to perform a development process on a resist film which has been subjected to light exposure with a predetermined pattern in the light exposure apparatus 103. The thermal processing units are arranged to respectively perform thermal processes on a wafer W with a resist film formed thereon, a wafer W treated by a light exposure process, and a wafer W treated by a development process.

[0030]

The light exposure apparatus 103 is used to subject a wafer W with a resist film formed thereon to light exposure with a predetermined circuit pattern. The cleaning apparatus 104 is arranged to perform a cleaning process using purified water or a chemical liquid, a denaturing process of polymer residues or the like remaining after an etching process, and a recovery process of an inter-level insulating film for damage due to etching, as described later in detail.

[0031]

The etching apparatus 105 is arranged to perform an etching process on an inter-level insulating film or the like formed on a wafer W. The etching process may be of a type using plasma or a type using a chemical liquid. The sputtering apparatus 106 is used to form,

e.g., each of an anti-diffusion film and a Cu seed layer. The electrolytic plating apparatus 107 is arranged to embed Cu in a groove having a Cu seed layer formed therein to form a groove interconnection line. The CMP apparatus 109 is arranged to perform a planarization process on a surface of a groove interconnection line filled with Cu, and so forth.

[0032]

Next, a detailed explanation will be given of the cleaning apparatus 104, which plays an important part of the present invention. FIGS. 3, 4, and 5 are a plan view, a front view, and a back view, respectively, schematically showing the cleaning apparatus 104. The cleaning apparatus 104 includes a carrier station 4, a process station 2, a transfer station 3, and a chemical station 5. The carrier station 4 is arranged such that carriers each storing wafers W are sequentially transferred from other processing apparatuses onto the carrier station 4. The carrier station 4 is also arranged such that carriers each storing wafers W processed in the cleaning apparatus 104 are transferred from the carrier station 4 to processing apparatuses for subsequent processes. The process station 2 includes a plurality of process units arranged to respectively perform a cleaning process, a denaturing process, and a recovery process. The transfer station 3 is arranged to transfer a wafer W between the process

station 2 and carrier station 4. The chemical station 5 is arranged to perform manufacture, preparation, and storage of chemical liquid, purified water, gas, and so forth to be used in the process station 2.

[0033]

Each carrier C contains therein wafers W essentially in a horizontal state at regular intervals in the vertical direction (Z-direction). The wafers W are transferred to and from the carrier C through one side of the carrier C, which is opened and closed by a lid 10a (which is not shown in FIG. 3, but shown in FIGS. 4 and 5 in a detached state).

[0034]

As shown in FIG. 3, the carrier station 4 has a table 6 on which carriers C can be placed at three positions arrayed in a Y-direction defined in FIG. 3. Each carrier C is placed on the table 6 such that the side provided with the lid 10a faces a partition wall 8a between the carrier station 4 and transfer station 3. The partition wall 8a has window portions 9a formed therein at positions corresponding to the mount positions for carriers C. Each of the window portions 9a is provided with a shutter 10 on the transfer station 3 side to open/close the window portion 9a. This shutter 10 includes holding means (not shown) for holding the lid 10a of a carrier C, so that the holding means can hold the lid 10a and withdraw it into the

transfer station 3, as shown in FIGS. 4 and 5.

[0035]

The transfer station 3 is provided with a wafer transfer unit 7 disposed therein, which has a wafer transfer pick 7a for holding a wafer W. The wafer transfer unit 7 is movable in the Y-direction along guides 7b (see FIGS. 4 and 5) extending on the floor of the transfer station 3 in the Y-direction. The wafer transfer pick 7a is slidable in an X-direction, movable up and down in the Z-direction, and rotatable in the X-Y plane (θ rotation).

[0036]

With the arrangement described above, the wafer transfer pick 7a can access any one of the carriers C placed on the table 6, in a state where the shutters 10 are retreated to allow the interior of the carriers C to communicate with the transfer station 3 through the window portions 9a. Accordingly, the wafer transfer pick 7a can transfer a wafer W from any height position in each of the carriers C, and can transfer a wafer W onto any height position in each of the carriers C.

[0037]

The process station 2 includes two wafer transit units (TRS) 13a and 13b on the transfer station 3 side. For example, the wafer transit unit (TRS) 13b is used to place a wafer W when the wafer W is transferred from the transfer station 3 to the process station 2. The

wafer transit unit (TRS) 13a is used to place a wafer W when the wafer W is returned to the transfer station 3 after it is subjected to a predetermined process in the process station 2.

[0038]

On the rear side of the process station 2, there are denaturing units (VOS) 15a to 15f arranged to process polymer residues, a resist film, and/or a sacrificial film remaining after an etching process, by a gas containing water vapor and ozone (O_3), so as to denature them to be soluble in a predetermined chemical liquid. In the denaturing units (VOS) 15a to 15f, polymer residues, a resist film, and/or a sacrificial film remaining after an etching process only change their chemical properties to be soluble in a predetermined chemical liquid, while they maintain their shapes or the like.

[0039]

Silylation units (SCH) 11a and 11b are disposed on the denaturing units (VOS) 15a and 15d, and are arranged to perform a silylation process on an inter-level insulating film damaged by the denaturing process, cleaning process, or the like, to recover the damage.

[0040]

On the front side of the process station 2, there are cleaning units (CNU) 12a to 12d arranged to perform a chemical liquid process or water washing process on a

wafer W treated by the denaturing units (VOS) 15a to 15f, so as to remove denatured polymer residues or the like.

[0041]

In the process station 2, four hot plate units (HP) 19a to 19d are stacked at a position opposite to the wafer transit units (TRS) 13a and 13b with a main wafer transfer unit 14 interposed therebetween. The hot plate units (HP) 19a to 19d are arranged to bake a wafer W after the silylation process in the silylation units (SCH) 11a and 11b and/or to heat and dry a wafer W treated by the cleaning units (CNU) 12a to 12d. Further, cooling plate units (COL) 21a and 21b are stacked on the wafer transit unit (TRS) 13a, and are arranged to cool a wafer W treated by the heat and dry process. The wafer transit unit (TRS) 13b may be arranged as a cooling plate unit. A fan and filter unit (FFU) 25 is disposed at the top of the process station 2, and is arranged to send clean air into the process station 2.

[0042]

The main wafer transfer unit 14 is disposed essentially at the center of the process station 2, and is arranged to transfer a wafer W within the process station 2. The main wafer transfer unit 14 has a wafer transfer arm 14a for transferring a wafer W. The main wafer transfer unit 14 is rotatable about a Z-axis.

Further, the wafer transfer arm 14a is movable back and forth in a horizontal direction, and movable up and down in the Z-direction. With this arrangement, the main wafer transfer unit 14 can access the respective units disposed in the process station 2 to transfer a wafer W between the units, without moving itself in the X-direction.

[0043]

The chemical station 5 includes a process gas supply portion 16, a cleaning liquid supply portion 17, and a silylation agent supply portion 18. The process gas supply portion 16 is arranged to supply ozone, water vapor, and so forth as process gases to the denaturing units (VOS) 15a to 15f disposed in the process station 2. The cleaning liquid supply portion 17 is arranged to supply a cleaning liquid to the cleaning units (CNU) 12a to 12d. The silylation agent supply portion 18 is arranged to supply a silylation agent, a carrier gas, and so forth to the silylation units (SCH) 11a and 11b.

[0044]

Next, a detailed explanation will be given of the structure of the denaturing unit (VOS) 15a with reference to the schematic sectional view shown in FIG. 6. The other denaturing units (VOS) 15b to 15f have exactly the same structure as the denaturing unit (VOS) 15a. This denaturing unit (VOS) 15a includes an

airtight chamber 30 for accommodating a wafer W. The chamber 30 is formed of a stationary lower container 41a, and a lid 41b that covers the top face of the lower container 41a. The lid 41b is movable up and down by a cylinder 43 fixed to a frame 42 of the film denaturing unit (VOS) 15a. FIG. 6 shows both of a state where the lid 41b is in close contact with the lower container 41a, and a state where the lid 41b is retreated above the lower container 41a.

[0045]

The lower container 41a is provided with an O-ring 51 disposed on the top face of a raised portion at the rim. When the lid 41b is moved down by the cylinder 43, the rim of the bottom face of the lid 41b comes into contact with the top face of the raised portion at the rim of the lower container 41a and presses the O-ring 51 to form an airtight process space in the chamber 30.

[0046]

The lower container 41a includes a stage 33 for placing a wafer W thereon. The stage 33 is provided with proximity pins 44 at a plurality of positions to support the wafer W.

[0047]

The stage 33 includes a heater 45a built therein, and the lid 41b includes a heater 45b built therein, so that each of the stage 33 and lid 41b is maintained at a predetermined temperature. Consequently, the

temperature of a wafer W can be kept constant.

[0048]

The lid 41b has hook members 46 at, e.g., three positions (only two of them are shown in FIG. 6) on the bottom face to hold a wafer W. The wafer W is transferred to and from the hook members 46 by the wafer transfer arm 14a. When the lid 41b is moved down while a wafer W is supported by the hook members 46, the wafer W is transferred onto the proximity pins 44 provided on the stage 33, on the way.

[0049]

The lower container 41a has a gas feed port 34a for supplying a process gas into the chamber 30, and a gas exhaust port 34b for exhausting the process gas out of the chamber 30. The gas feed port 34a is connected to the process gas supply unit 16, and the gas exhaust port 34b is connected to an exhaust unit 32.

[0050]

When a wafer W is processed by a process gas, the pressure inside the chamber 30 is preferably maintained at a constant positive pressure. For this purpose, the lower container 41a and lid 41b are supplied with not only a pressing force by the cylinder 43, but also a clamping force by a lock mechanism 35 through projecting portions 47a and 47b respectively disposed on end sides of the lower container 41a and lid 41b.

[0051]

The lock mechanism 35 includes a support shaft 52, a rotary tube 55 rotatable by a rotator unit 54, a circular plate 56 fixed to the rotary tube 55, and pinching devices 57 disposed at the rim of the circular plate 56. Each of the pinching devices 57 includes press rollers 59a and 59b and a roller holding member 48 which holds rotary shafts 58.

[0052]

The projecting portions 47a and 47b are equidistantly disposed at four positions, between which gap portions 49 are defined. The projecting portions 47a and 47b of each set are disposed at positions overlapping with each other. When the pinching devices 57 are positioned in the gap portions 49, the lid 41b can be freely moved up and down.

[0053]

When the circular plate 56 is rotated along with the rotary tube 55 by a predetermined angle, the press rollers 59b are stopped at the top faces of the projecting portions 47b, while the press rollers 59a are stopped under the projecting portions 47a. The other denaturing units have exactly the same structure as that described above.

[0054]

Next, a detailed explanation will be given of the structure of the silylation unit (SCH) 11a with reference to the schematic sectional view shown in FIG.

7. The other silylation unit (SCH) 11b has exactly the same structure as the silylation unit (SCH) 11a. The silylation unit (SCH) 11a includes a chamber 61 for accommodating a wafer W. The chamber 61 is formed of a stationary lower container 61a, and a lid 61b that covers the lower container 61a. The lid 61b is movable up and down by an elevating unit (not shown). The lower container 61a includes a hot plate 62, around which nitrogen gas with vapor of a silylation agent carried therein, such as DMSDMA (Dimethylsilyldimethylamine), is supplied into the chamber 61. DMSDMA is vaporized by a vaporizer 63, and carried by N_2 gas into the chamber 61.

[0055]

The hot plate 62 is adjustable in temperature within a range of, e.g., from a room temperature to 400℃. The hot plate 62 is provided with pins 64 on the surface to support a wafer W. Where a wafer W is mounted not directly on the hot plate 62, the wafer W is prevented from being contaminated on its bottom surface. The lower container 61a is provided with a first seal ring 65 disposed on the top face of the peripheral portion. The lid 61b is provided with a second seal ring 66 disposed on the bottom face of the peripheral portion. When the lid 61b is pressed against the lower container 61a, the second seal ring 66 comes into contact with the first seal ring 65. The

space defined between the first and second seal rings 65 and 66 can be pressure-reduced. When the pressure of this space is reduced, it is ensured that the chamber 61 is airtight. The lid 61b has an exhaust port essentially at the center for exhausting nitrogen gas with DMSDMA carried therein supplied into the chamber 61. The exhaust port 67 is connected to a vacuum pump 69 through a pressure adjusting unit 68.

[0056]

In FIG. 7, liquid DMSDMA is vaporized by the vaporizer 63, and carried by N_2 gas into the chamber 61. Alternatively, vaporized DMSDMA gas (i.e., DMSDMA vapor) may solely be supplied into the chamber 61. When DMSDMA is supplied into the chamber 61, the interior of the chamber 61 is maintained at a predetermined vacuum level. Accordingly, utilizing the pressure difference between the vaporizer 63 and chamber 61, DMSDMA gas is easily supplied into the chamber 61.

[0057]

Next, a detailed explanation will be given of the structure of the cleaning unit 12a with reference to the schematic sectional view shown in FIG. 8. The other cleaning units (CNU) 12b to 12d have exactly the same structure as the cleaning unit 12a. The cleaning unit (CNU) 12a includes an annular cup CP disposed at the center, and a spin chuck 71 disposed inside the cup

(CP). The spin chuck 71 is arranged to fix and hold a wafer W by means of vacuum suction, and to be rotated by a drive motor 72 in this state. A drain line 73 is connected to the bottom of the cup (CP) to exhaust the cleaning liquid and purified water.

[0058]

The drive motor 72 is disposed to be movable up and down in an opening 74a formed in the unit bottom plate 74. The drive motor 72 is coupled with an elevating mechanism 76, such as an air cylinder, and a vertical guide 77 through a cap-like flange member 75. The drive motor 72 is provided with a cylindrical cooling jacket 78 attached on its side. The flange member 75 is attached to cover the upper half of the cooling jacket 78.

[0059]

When a chemical liquid or the like is supplied onto a wafer W, the lower end 75a of the flange member 75 comes into close contact with the unit bottom plate 74 near the rim of the opening 74a to make the unit interior airtight. When a wafer W is transferred between the spin chuck 71 and wafer transfer arm 14a, the drive motor 72 and spin chuck 71 are moved up by the elevating mechanism 76, so that the lower end of the flange member 75 is separated upward from the unit bottom plate 74.

[0060]

A cleaning liquid supply mechanism 80 is disposed above the cup (CP) to supply a predetermined cleaning liquid onto the surface of a wafer W. The cleaning liquid is used for dissolving a substance denatured by one of the denaturing units (VOS) 15a to 15f (which will be referred to as a denatured substance, hereinafter), such as a denatured sacrificial film, present on the wafer.

[0061]

The cleaning liquid supply mechanism 80 includes a cleaning liquid delivery nozzle 81, a cleaning liquid supply portion 17, a scan arm 82, a vertical support member 85, and an X-axis driving mechanism 86. The cleaning liquid delivery nozzle 81 is arranged to deliver the cleaning liquid onto the surface of a wafer W held on the spin chuck 71. The cleaning liquid supply portion 17 is arranged to supply the predetermined cleaning liquid to the cleaning liquid delivery nozzle 81. The scan arm 82 is arranged to hold the cleaning liquid delivery nozzle 81, and to be movable back and forth in the Y-direction. The vertical support member 85 is arranged to support the scan arm 82. The X-axis driving mechanism 86 is disposed on a guide rail 84 extending in the X-axis direction on the unit bottom plate 74, and is arranged to shift the vertical support member 85a in the X-axis direction. The scan arm 82 is movable in the vertical

direction (Z-direction) by a Z-axis driving mechanism 87, so that the cleaning liquid delivery nozzle 81 can be moved to an arbitrary position above a wafer W, and retreated to a predetermined position outside the cup (CP).

[0062]

The cleaning liquid supply portion 17 can selectively supply one of a dissolving/removing liquid and a rinsing liquid consisting of purified water to the cleaning liquid delivery nozzle 81. The dissolving/removing liquid is used for dissolving a denatured substance, such as a sacrificial film, denatured by the denaturing units (VOS) 15a to 15f, and comprises, e.g., dilute hydrofluoric acid or an amine-based chemical liquid.

[0063]

Next, a detailed explanation will be given of the hot plate unit (HP) 19a used for a baking process after the silylation process, with reference to the schematic sectional view shown in FIG. 9. The other hot plate units (HP) 19b to 19d have exactly the same structure as the hot plate unit (HP) 19a. This hot plate unit (HP) 19a includes a process chamber 91 having an essentially cylindrical shape and provided with a wafer table 92 disposed therein on the bottom. The wafer table 92 includes a heater 93 built therein, so that a heat process, such as a baking process after silylation,

can be performed on a wafer W placed on the wafer table 92. The heater 93 is connected to a heater power supply 94. The wafer table 93 is provided with wafer lifter pins (not shown) that can project and retreat relative to the wafer table 93. When the wafer W is loaded and unloaded, the wafer W is set at a predetermined position above the wafer table 92 by the pins. The chamber 91 has a wafer transfer port (not shown) formed in the sidewall 91a.

[0064]

Further, the chamber 91 has an air feed port 95 formed in the sidewall 91a at a position corresponding to the wafer W placed on the table 92, and an air exhaust port 96 formed in the ceiling wall 91b at the center.

[0065]

The denaturing units (VOS) 15a to 15c and denaturing units (VOS) 15d to 15f described above have structures essentially symmetric with respect to a partition wall 22b. The silylation unit (SCH) 11a and silylation unit (SCH) 11b have structures essentially symmetric with respect to the partition wall 22b. Similarly, the cleaning units (CNU) 12a and 12b and cleaning units (CNU) 12c and 12d have structures essentially symmetric with respect to the partition wall 22a.

[0066]

Next, an explanation will be given of a semiconductor device manufacturing process employing a dual damascene method, to which a substrate processing method according to an embodiment of the present invention is applied.

FIG. 10 is a flowchart showing a semiconductor device manufacturing process employing a dual damascene method. FIG. 11 is an explanatory view for explaining states appearing in steps of the flowchart shown in FIG. 10.

[0067]

At first, a wafer W is prepared from an Si substrate (not shown) as follows. Specifically, an insulating film 120 is disposed on the substrate. A lower interconnection line 122 made of copper is disposed in the insulating film 120 with a barrier metal layer 121 interposed therebetween. A stopper film (such as an SiN film or SiC film) 123 is disposed on the insulating film 120 and lower interconnection line 122 made of copper. The wafer W is transferred into the SOD apparatus 101, in which an inter-level insulating film (which will be referred to as a Low-k film, hereinafter) 124 made of a low dielectric constant material (Low-k material) is formed on the stopper film 123 (Step 1). Consequently, the state shown in FIG. 11-(a) is prepared.

[0068]

Then, the wafer W with the Low-k film 124 formed thereon is transferred into the resist coating/development apparatus 102, in which an anti-reflective coating 125 and a resist film 126 are sequentially formed on the Low-k film 124 by the resist coating unit. Then, the wafer W is transferred into the light exposure apparatus 103, in which the wafer W is subjected to a light exposure process with a predetermined pattern. Then, the wafer W is transferred back into the resist coating/development apparatus 102, in which the resist film 126 is subjected to a development process by the developing unit to form a predetermined circuit pattern on the resist film 126 (Step 2). Then, the wafer W is transferred into the etching apparatus 105, in which an etching process is performed on the wafer W (Step 3). Consequently, as shown in FIG. 11-(b), a via-hole 124a reaching the stopper film 123 is formed in the Low-k film 124.

[0069]

The wafer W with the via-hole 124a formed thereon is transferred into the cleaning apparatus 104, in which a chemical liquid process is performed on the wafer W by one of the cleaning units (CNU) 12a to 12d to remove the resist film 126 and anti-reflective coating 125 from the wafer W (Step 4 and FIG. 11-(c)).

[0070]

Then, the wafer W is transferred into the resist coating/development apparatus 102, in which a sacrificial film 127 made of an inorganic material (such as an Si-O based material) is formed on the surface of the Low-k film 124 having the via-hole 124a by the sacrificial film coating unit (Step 5). At this time, the via-hole 124a is filled with the sacrificial film 127. Then, a resist film 128 to be used as an etching mask is formed on the surface of the sacrificial film 127 by the resist coating unit. Then, the resist film 128 is subjected to light exposure with a predetermined pattern by the light exposure apparatus 103. Then, the resist film 128 is subjected to a development process by the developing unit (Step 6). Consequently, as shown in FIG. 11-(d), a circuit pattern is formed on the resist film 128, such that a groove wider than the via-hole 124a is formed in the resist film 128 above the via-hole 124a.

[0071]

Then, the wafer W is transferred into the etching apparatus 105, in which an etching process is performed on the Low-k film 124 on the wafer W (Step 7). Consequently, as shown in FIG. 11-(e), a wider trench 124b is formed above the via-hole 124a. Since the sacrificial film 127 is formed on the Low-k film 124, the bottom surface of the etched portion in the Low-k film 124 can be flat.

[0072]

The wafer W thus treated by the etching process is transferred into the cleaning apparatus 104, in which the wafer W is sequentially subjected to a denaturing process of the sacrificial film 127 and resist film 128 (Step 8 and FIG. 11-(f)), and a removing process of the sacrificial film 127, resist film 128, and polymer residues (Step 9 and FIG. 11-(g)).

[0073]

Specifically, at first, a carrier C storing wafers treated by the etching process is placed on the table 6. Then, the lid 10a of the carrier C and the shutter 10 are retreated in the transfer station 3 side to open the corresponding window portion 9a. Then, a wafer W at a predetermined position in the carrier C is transferred into the wafer transit unit (TRS) 13b by the wafer transfer pick 7a.

[0074]

Then, the wafer W placed in the wafer transit unit (TRS) 13b is transferred by the wafer transfer arm 14a into one of the denaturing units (VOS) 15a to 15h, in which the denaturing process of the sacrificial film 127 and resist film 128 is performed in Step 8 described above (FIG. 11-(f)).

[0075]

In this case, the lid 41b of the chamber 30 is first retreated above the lower container 41a. In this

state, the wafer transfer arm 14a that holds the wafer W is moved forward such that the wafer W is inserted at a position slightly higher than the portions for supporting the wafer W in the hook members 46 attached to the lid 41b (portions extending in the horizontal direction). Then, the wafer transfer arm 14a is moved down to transfer the wafer W onto the hook members 46.

[0076]

After the wafer transfer arm 14a is retreated from the denaturing unit (VOS) 15a, the lid 41b is moved down to bring the lid 41b into close contact with the lower container 41a, and the lock mechanism 35 is further operated to set the chamber 30 in an airtight state. When the lid 41b is moved down, the wafer W is transferred from the hook members 46 onto the proximity pins 44 on the way.

[0077]

The stage 33 and lid 41b are maintained at predetermined temperatures by the heaters 45a and 45b. For example, the stage 33 is maintained at 100℃, and the lid 41b is maintained at 110℃.

[0078]

When the stage 33 and lid 41b are set at predetermined temperatures (such as 110℃ to 120℃), and the temperature distribution of the wafer W becomes essentially uniform, a mixture gas of ozone and nitrogen (with an ozone content of 9 wt% and at a flow

rate of 4 L/min, for example) is first solely supplied from the process gas supply unit 16 into the chamber 30. At this time, the gas is adjusted such that the chamber 30 is filled with the mixture gas of ozone and nitrogen to have a predetermined positive pressure of, e.g., 0.2 MPa by gauge pressure.

[0079]

Then, a process gas prepared by mixing water vapor with the mixture gas of ozone and nitrogen (with a water vapor content corresponding to 16 ml/min expressed in terms of liquid, for example) is supplied from the process gas supply unit 16 into the chamber 30. With this process gas, the sacrificial film 127 formed on the wafer W is denatured to be easily dissolved in a particular chemical liquid, such as HF. Further, polymer residues deposited on the resist film 128 and wafer W (such as polymer residues generated by the etching process) are also denatured to be easily dissolved in the chemical liquid. As described above, the process gas denatures the sacrificial film 127, resist film, and polymer residues. The supply rate and exhaust rate of the process gas to and from the chamber 30 are controlled for the interior of the chamber 30 to have a predetermined positive pressure.

[0080]

When the process using the process gas on the wafer W is finished, the supply of the process gas is

stopped. Further, nitrogen gas is supplied from the process gas supply unit 16 into the chamber 30 to purge the interior of the chamber 30 with nitrogen gas. This purge process is performed to completely exhaust the mixture gas of ozone and nitrogen even from the exhaust unit 32, so that no mixture gas of ozone and nitrogen flows from the exhaust unit 32 back into the chamber 30 and leaks out of the chamber 30 when the chamber 30 is opened thereafter.

[0081]

When the nitrogen gas purge process is finished, it is confirmed that the inner pressure and external pressure of the chamber 30 are the same. This is done, because, if the chamber 30 is opened while the inner pressure of the chamber 30 is higher than atmospheric pressure, the chamber 30 may be damaged. After the inner pressure of the chamber 30 is confirmed, the lock mechanism 35 breaks up the clamping force applied to the lower container 41a and lid 41b, and then the lid 41b is moved up. When the lid 41b is moved up, the wafer W is moved up along with the lid 41b while being supported by the hook members 46. Then, the wafer transfer arm 14a is inserted into the gap between the lower container 41a and lid 41b, so that the wafer W is transferred from the hook members 46 onto the wafer transfer arm 14a.

[0082]

When the denaturing process is finished at one of the film denaturing units (VOS) 15a to 15f, the sacrificial film 127 and so forth have been not yet removed from the wafer W. Accordingly, a dissolving/removing process (cleaning process) is performed to remove the sacrificial film 127 and so forth from the wafer W (Step 9 described above).

[0083]

When the dissolving/removing process is performed, the wafer W is transferred into one of the cleaning units (CNU) 12a to 12d. In this unit, a predetermined chemical liquid (such as dilute hydrofluoric acid or amine-based chemical liquid) that can dissolve the sacrificial film 127 and so forth is supplied to perform the dissolving/removing process on the sacrificial film 127 and so forth (Step 9 described above and FIG. 11-(g)).

[0084]

Specifically, when the dissolving/removing process is performed, the wafer W is transferred into one of the cleaning units (CNU) 12a to 12d. The wafer W is placed on the spin chuck 71 and is held thereon essentially in a horizontal state by means of vacuum suction. Then, a chemical liquid that can dissolve denatured substances of the sacrificial film 127 and so forth is supplied from the cleaning liquid delivery nozzle 81 of the cleaning liquid supply mechanism 80

onto the surface of the wafer W to form a puddle of the solution. After this state is held for a predetermined time, the wafer W is rotated to throw off the chemical liquid from the surface of the wafer W. Further, while the wafer W is rotated, the chemical liquid is supplied onto the surface of the wafer W to completely remove the sacrificial film 127 and so forth. At this time, the resist film 128 and polymer residues are also dissolved and removed by the chemical liquid for removing the sacrificial film 127. After the chemical liquid process, while the wafer W is rotated by the drive motor 72, purified water is supplied onto the wafer W to perform a water washing process on the wafer W. Then, the wafer W is rotated at a higher speed to perform spin-drying. The spin-drying of the wafer W may be performed while a drying gas is supplied onto the wafer W.

[0085]

A damaged portion 130 is formed by this process in the surface of the Low-k film 124, as shown in FIG. 11-(g). This damaged portion 130 is a portion changed from a hydrophobic state to a hydrophilic state when the Low-k film 124 is subjected to the dissolving/removing process of Step 9. This portion increases the specific dielectric constant of the Low-k film 124, and thus increases the parasitic capacitance between interconnection lines after interconnection

line formation. Consequently, problems arise in electric properties such that a signal delay occurs and the insulation between groove interconnection lines is deteriorated. At this time, although FIG. 11-(g) clearly shows the damaged portion 130 formed in the Low-k film 124 for the sake of convenience, the boundary between the damaged portion 130 and non-damaged portion is not necessarily clear.

[0086]

In light of the problem described above, after the dissolving/removing process of Step 9, a silylation process is performed (Step 10 and FIG. 11-(h)) to recover the damage of the damaged portion 130 of the Low-k film 124.

[0087]

Damaged portions of this kind have a state with damage as shown in FIG. 12. Specifically, the Low-k film 124, which has methyl groups (Me) as end groups and thus is hydrophobic, reacts with water molecules during the denaturing process using water vapor and ozone and during the dissolving/removing process. Consequently, the number of methyl groups is decreased and the number of hydroxyl groups is increased near the sidewall of the via-hole 124a, so the specific dielectric constant (k-value) is increased. Accordingly, the silylation process is performed to make the Low-k film surface hydrophobic, and thereby

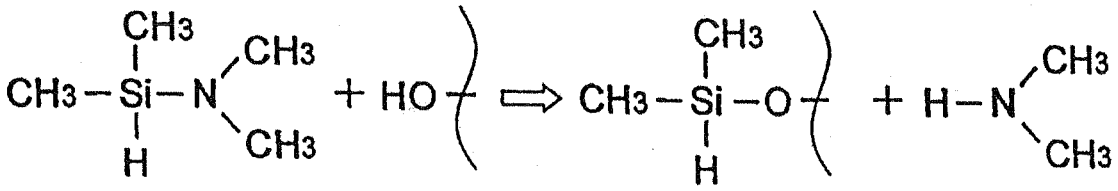
recover the damage.

[0088]

In the silylation process, the wafer W is transferred into one of the silylation units (SCH) 11a and 11, and is placed on the support pins 64 of the hot plate 62. Then, a silylation agent, such as DMSDMA vapor, carried by N_2 gas is supplied into the chamber 61. The conditions of the silylation process are suitably selected in accordance with the type of the silylation agent, as follows. For example, the temperature of the vaporizer 63 is set to be from a room temperature to 50℃. The silylation agent flow rate is set to be 0.6 to 1.0 g/min. The N_2 gas (purge gas) flow rate is set to be 1 to 10 L/min. The process pressure is set to be 532 to 95,976 Pa (4 to 720 Torr). The temperature of the hot plate 62 is set to be from room temperature to 200℃. Where DMSDMA is used as the silylation agent, the following method may be used, for example. Specifically, the temperature of the hot plate 62 is set at 100℃, and the inner pressure of the chamber 61 is decreased to 5 Torr (= 666 Pa). Then, DMSDMA vapor carried by N_2 gas is supplied into the chamber 61 until the inner pressure reaches 55 Torr. Then, the process is performed for, e.g., 3 minutes, while maintaining the pressure. The silylation reaction using DMSDMA is expressed by the following chemical formula 1.

[0089]

[Chemical formula 1]

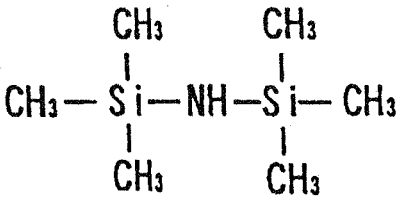


[0090]

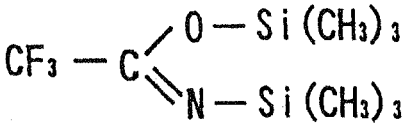
The silylation agent is not limited to DMSDMA described above, and the agent may comprise any substance as long as it causes a silylation reaction. However, it is preferable to use a substance having a relatively small molecular structure selected from the compounds including silazane bonds (Si-N bonds) in molecules, such as a substance having a molecular weight preferably of 260 or less, and more preferably of 170 or less. Namely, examples other than DMSDMA are HMDS (Hexamethyldisilazane), TMSDMA (Dimethylaminotrimethylsilane), TMDS (1,1,3,3-Tetramethyldisilazane), TMSpyrole (1-Trimethylsilylpyrole), BSTFA (N,O-Bis(trimethylsilyl)trifluoroacetamide), and BDMADMS (Bis(dimethylamino)dimethylsilane). Of them, TMDS (1,1,3,3-Tetramethyldisilazane), TMSDMA (Dimethylaminotrimethylsilane), and DMSDMA (Dimethylsilyldimethylamine) are preferable. The chemical structures of these substances are as follows.

[0091]

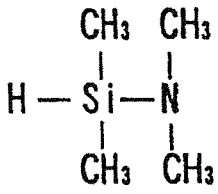
[Chemical formula 2]



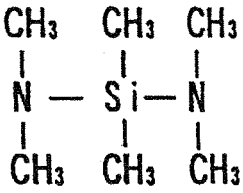
HMDS



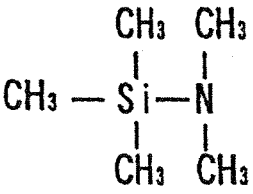
BSTFA



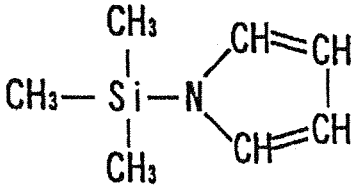
DMSDMA



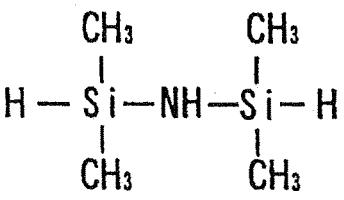
BDMADMS



TMSDMA



TMSpyrole



TMDS

[0092]

Where damage recovery is performed by the silylation process described above, the k-value is decreased to some extent, but cannot reach a predetermined level in many cases. By studying this mechanism, it has been found that this is due to the following reason. Specifically, where a porous material is used for the Low-k film 124 as in the current trend, moisture is contained in the Low-k film 124 during the denaturing process and dissolving/removing process (see FIG. 11-(f) and -(g)), and then this moisture reacts with a silylation agent supplied in the silylation process to generate an Si-containing by-product. The Si-containing by-product thus generated typically has a high k-value exists at the surface and inside of the film, and prevents the k-value from being sufficiently recovered even if the silylation process is performed to recover damage by forming end groups of alkyl groups, such as methyl groups.

[0093]

In light of this, according to this embodiment, after the silylation process is performed on a wafer W, a baking process is performed on the wafer W in one of the hot plate units (HP) 19a to 19d (Step 11 and FIG. 11-(i)). Consequently, the Si-containing by-product in the Low-k film 124 is decomposed and removed, and the

Low-k film 124 is free from the Si-containing by-product that increases the k-value, so the k-value of the Low-k film 124 is sufficiently recovered.

[0094]

When the baking process is performed in one of the hot plate units (HP) 19a to 19d, a wafer W is transferred through the wafer transfer port (not shown) formed in the sidewall 91a of the chamber 91 and placed on the table 92. Then, the heater 93 is supplied with a power to heat the wafer W on the table 92. The heating temperature used at this time is preferably set to be higher than the temperature of the silylation process, because the Si-containing by-product needs to be decomposed. Specifically, the heating temperature is preferably set to be 150 to 400℃, and more preferably to be 300 to 360℃. This baking process may be performed in the silylation units 11a and 11b.

[0095]

After the baking process is thus performed, the wafer W is transferred by the transfer arm 14a from the hot plate unit (HP) onto the wafer transit unit (TRS) 13a. Then, the wafer W is transferred by the wafer transfer unit 7 into a carrier C, which is then transferred from the cleaning apparatus 104.

[0096]

Then, the wafer W is transferred into the sputtering apparatus 106, in which a barrier metal film

and a Cu seed layer (i.e., plating seed layer) are formed on the inner surface of the via-hole 124a and trench 124b. Then, the wafer W is transferred into the electrolytic plating apparatus 107, in which copper 131 used as an interconnection line metal is embedded in the via-hole 124a and trench 124b by electrolytic plating (Step 12 and FIG. 11-(j)). Thereafter, the wafer W is subjected to a heat process to perform an annealing process of the copper 131 embedded in the via-hole 124a and trench 124b (no annealing apparatus is shown in FIG. 1). Then, the wafer W is transferred into the CMP apparatus 109, in which a planarization process of the wafer W is performed by a CMP method (Step 13). Consequently, a predetermined semiconductor device is manufactured.

[0097]

As described above, in order to remove the sacrificial film 127 and so forth, the sacrificial film 127 and so forth are denatured to be soluble in a predetermined chemical liquid, and then the denatured substances are dissolved and removed by the chemical liquid. Where this method is adopted, the silylation process is performed to recover damage formed to the Low-k film 124 until the dissolving/removing process, and then the baking process is further performed. Consequently, the Si-containing by-product that is generated by the silylation and prevents recovery of

the k-value is decomposed, so the k-value of the Low-k film 124 is sufficiently recovered.

[0098]

The Low-k film 124 with a pattern formed thereon may be damaged by the process using water vapor and ozone in the denaturing unit (VOS). If the dissolving/removing process using a chemical liquid is subsequently performed on the film with such damage, pattern peeling may be caused. In light of this, a silylation process may be performed before the dissolving/removing process, so that the damage of the Low-k film 124 is recovered. This silylation process may be performed in one of the silylation units 11a and 11b in the same manner as that of the silylation process performed after the dissolving/removing process.

[0099]

A pre-baking process may be performed before the silylation process performed after the dissolving/removing process. With this heating, moisture remaining on the wafer W is removed, so that the effect of the silylation process is enhanced. The heating temperature used at this time is preferably set to be 200℃ or less. Further, in order to effectively remove moisture, the heating temperature is preferably set to be 50℃ or more. This pre-baking process may be performed in the hot plate units (HP) 19a to 19d or silylation units 11a and 11b.

[0100]

Next, an explanation will be given of an experiment conducted to confirm effects of the present invention. In this experiment, the Low-k film 124 was formed of a porous Low-k film (k-value: about 2.5) and processed in different manners, as shown in Table 1. Specifically, they were a manner (initial: No.1) in which no process was performed thereon, a manner (No.2) in which only the denaturing process (VOS) and dissolving/removing process (Wet) were performed thereon without the silylation process, a manner (No.3) in which the denaturing process (VOS) and dissolving/removing process (Wet) were performed thereon and then the silylation process (LKR) was further performed thereon, a manner (No.4) in which the denaturing process (VOS), dissolving/removing process (Wet), and silylation process (LKR) were performed thereon and then the baking process (Bake) was further performed thereon at 250℃, and a manner (No.5) in which denaturing process (VOS), dissolving/removing process (Wet), and silylation process (LKR) were performed thereon and then the baking process (Bake) was further performed thereon at 350℃. By use of the Low-k film 124 thus processed, the k-value at room temperature, the leakage current at 1MV, the degasification of H_2O, and the degasification of a substance having a molecular weight of 75 were measured. Table 1 shows

results of the measurement.

[0101]

In this experiment, the process conditions were set as follows.

Denaturing process (VOS): at 105℃ for 1 min,

Dissolving/removing process (Wet): with organic alkaline chemical liquid for 1 min,

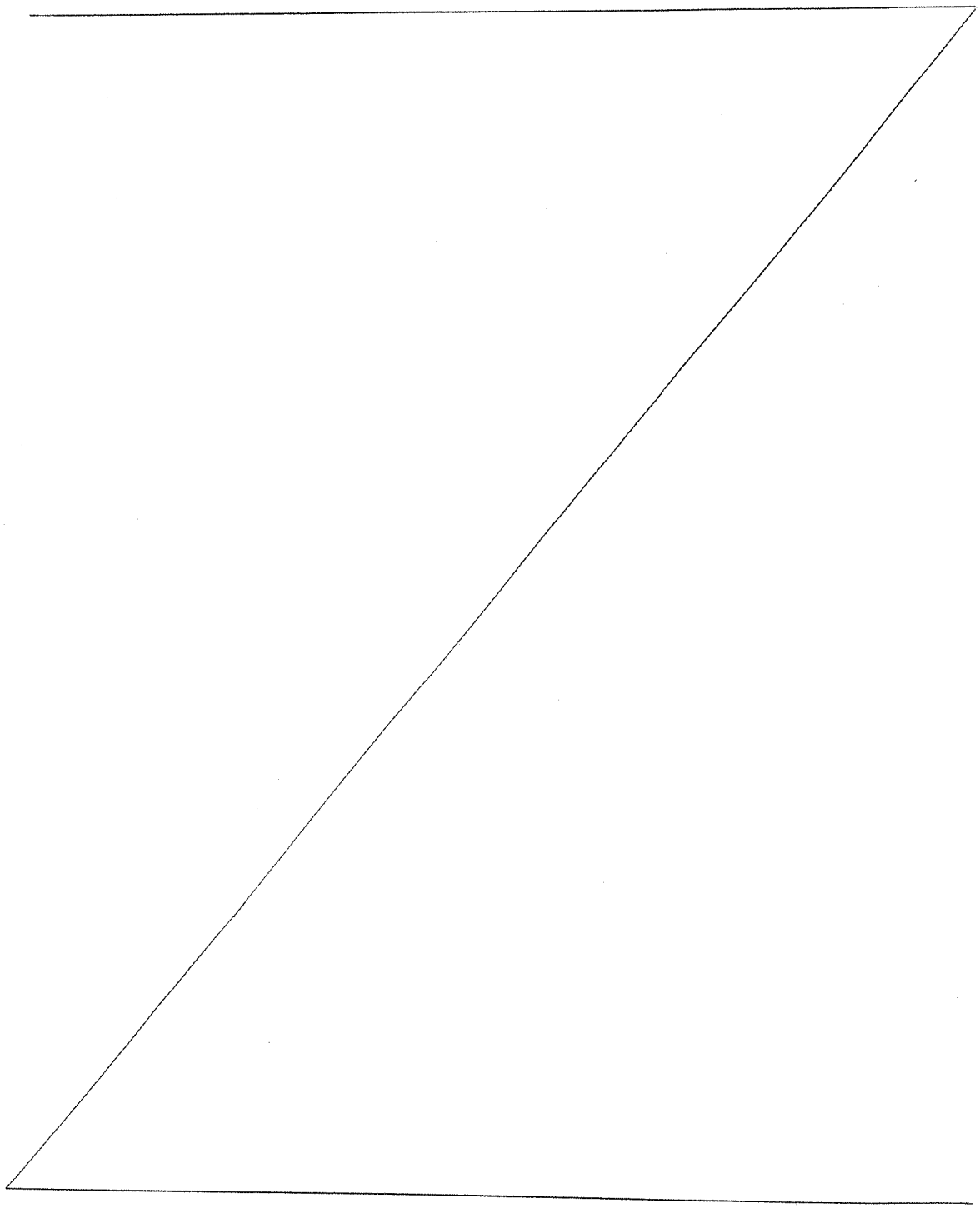
Silylation process (LKR): at 150℃ for 150 sec, and

Baking process (Bake): at atmospheric pressure for 30 min.

[0102]

As shown in Table 1, where the silylation process was performed, recovery of the k-value and decrease in the leakage current were obtained. Further, where the baking process was performed after the silylation process, recovery of the k-value was developed. Particularly, where the baking process was performed at 350℃, the k-value was recovered by about 0.3, as compared to the case where only the silylation process was performed. The degasification of a substance having a molecular weight of 75 was large after the silylation process, but it was decreased after the baking process and particularly after the baking process at 350℃. It is though that the substance having a molecular weight of 75 was an Si-containing by-product, and recover of the k-value obtained by the baking process was caused by a decrease in this Si-

containing by-product. Further, moisture was slightly decreased by the baking process, and this moisture decrease supposedly contributed to recover of the k-value to some extent.



[Table 1]

No.		k-value @R.T.	Leakage @1MV (A/cm^2)	Degasification of H_2O	Degasification of substance having molecular weight of 75
1	Initial	2.7	1.5×10^{-9}	4.1×10^{-8}	2.5×10^{-10}
2	VOS+Wet	4.1	2.5×10^{-5}	3.0×10^{-7}	1.6×10^{-9}
3	VOS+Wet+LKR	3.2	1.5×10^{-9}	6.8×10^{-8}	1.8×10^{-7}
4	VOS+Wet+LKR+Bake 250deg	3.1	2.3×10^{-9}	5.5×10^{-8}	9.1×10^{-8}
5	VOS+Wet+LKR+Bake 350deg	2.9	1.1×10^{-9}	4.2×10^{-8}	4.2×10^{-8}

[0103]

[0104]

The present invention is not limited to the embodiment described above, and it may be modified in various manners. For example, in the embodiment described above, the denaturing process of the sacrificial film and so forth is performed using a mixture gas of water vapor and ozone, but the process may be performed solely using ozone without water vapor. Where the process is performed solely using ozone, the reactivity becomes lower as compared with a case using water vapor and ozone, but the sacrificial film and so forth thus denatured can be sufficiently dissolved in the subsequent dissolving/removing process using a chemical liquid.

[0105]

Further, the Low-k film on which damage recovery can be achieved by the silylation process is not limited to a specific film, and it may be an SOD film of porous MSQ. Alternatively, for example, an SiOC-based film, which is an inorganic insulating film formed by CVD, may be used. A film of this type can be prepared from a conventional SiO_2 film by introducing methyl groups ($-CH_3$) into Si-O bonds present on the film to mix $Si-CH_3$ bonds therewith. Black Diamond (Applied Materials Ltd.), Coral (Novellus Ltd.), and Aurora (ASM Ltd.) correspond to this type. Furthermore, it is possible to employ a porous SiOC-based film.

Also, it is possible to employ an MSQ-based insulating film having a compact texture in place of a porous texture.

[0106]

In the embodiment described above, the present invention is applied to a process using a dual damascene method for manufacturing a semiconductor device including a copper interconnection line, but this is not limiting. The present invention may be applied to any process in which an etching target film may be deteriorated, and a substance to be denatured and removed is present.

C L A I M S

[1] A substrate processing method comprising:

performing an etching process on a low dielectric constant film disposed on a substrate, thereby forming a predetermined pattern thereon;

denaturing a remaining substance to be soluble in a predetermined liquid after the etching process;

dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon;

then, performing a silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and

baking the substrate after the silylation process;

wherein, after said denaturing a remaining substance and before said dissolving and removing the substance denatured, the method further comprises performing a silylation process on a surface of the low dielectric constant film with the pattern formed thereon, by supplying a silylation agent thereon.

[2] The substrate processing method according to claim 1, wherein the low dielectric constant film comprises a porous low dielectric constant material.

[3] The substrate processing method according to claim 1, wherein the low dielectric constant film includes alkyl groups as end groups.

[4] The substrate processing method according to claim

1, wherein said denaturing a remaining substance comprises supplying a process gas containing water vapor and ozone.

[5] The substrate processing method according to claim 1, wherein said denaturing a remaining substance comprises supplying a process gas containing ozone.

[6] The substrate processing method according to claim 1, wherein the predetermined liquid comprises an acidic or alkaline chemical liquid.

[7] The substrate processing method according to claim 1, wherein the silylation agent used for the silylation process comprises a compound including silazane bonds (Si-N) in molecules.

[8] The substrate processing method according to claim 7, wherein the compound including silazane bonds in molecules is selected from the group consisting of TMDS (1,1,3,3-Tetramethyldisilazane), TMSDMA (Dimethylaminotrimethylsilane), and DMSDMA (Dimethylsilyldimethylamine).

[9] The substrate processing method according to claim 1, wherein said baking the substrate is performed at a temperature higher than a temperature used for the silylation process.

[10] The substrate processing method according to claim 9, wherein said baking the substrate is performed at a temperature of 150 to 400°C.

[11] The substrate processing method according to claim 1, wherein the method further comprises performing a

baking process before the silylation process performed after said dissolving and removing the substance denatured.

[12] A substrate processing method comprising:

forming a sacrificial film on a low dielectric constant film disposed on a substrate;

forming an etching mask on the sacrificial film, and etching the sacrificial film and the low dielectric constant film, thereby forming a predetermined pattern thereon;

denaturing the sacrificial film and the etching mask to be soluble in a predetermined liquid;

dissolving and removing the substance thus denatured, by supplying the predetermined liquid thereon;

then, performing a silylation process on a surface of the low dielectric constant film, by supplying a silylation agent thereon, after said dissolving and removing the substance denatured; and

baking the substrate after the silylation process;

wherein, after said denaturing a remaining substance and before said dissolving and removing the substance denatured, the method further comprises performing a silylation process on a surface of the low dielectric constant film with the pattern formed thereon, by supplying a silylation agent thereon.

[13] The substrate processing method according to claim 12, wherein the low dielectric constant film comprises a porous low dielectric constant material.

[14] The substrate processing method according to claim 12, wherein the low dielectric constant film includes alkyl groups as end groups.

[15] The substrate processing method according to claim 12, wherein said denaturing a remaining substance comprises supplying a process gas containing water vapor and ozone.

[16] The substrate processing method according to claim 12, wherein said denaturing a remaining substance comprises supplying a process gas containing ozone.

[17] The substrate processing method according to claim 12, wherein the predetermined liquid comprises an acidic or alkaline chemical liquid.

[18] The substrate processing method according to claim 12, wherein the silylation agent used for the silylation process comprises a compound including silazane bonds (Si-N) in molecules.

[19] The substrate processing method according to claim 18, wherein the compound including silazane bonds in molecules is selected from the group consisting of TMDS (1,1,3,3-Tetramethyldisilazane), TMSDMA (Dimethylaminotrimethylsilane), and DMSDMA (Dimethylsilyldimethylamine).

[20] The substrate processing method according to claim 12, wherein said baking the substrate is performed at a temperature higher than a temperature used for the silylation process.

[21] The substrate processing method according to claim 20, wherein said baking the substrate is performed at a temperature of 150 to 400°C.

[22] The substrate processing method according to claim 12, wherein the method further comprises performing a baking process before the silylation process performed after said dissolving and removing the substance denatured.