What is claimed is:

1. A method of forming a memory structure, comprising:

forming a number of memory structure regions, wherein the memory structure regions include a bottom electrode material and a sacrificial material;

forming a number of insulator regions between the number of memory structure regions;

forming a number of openings between the number of insulator regions and forming a contoured surface on the number of insulator regions by removing the sacrificial material and a portion of the number of insulator regions;

forming a number of dielectric spacers on the number of insulator regions;

forming a contoured opening between the number of insulator regions and exposing the bottom electrode material by removing a portion of the number of dielectric spacers; and

forming a phase change material in the opening between the number of insulator regions.

2. The method of claim 1, wherein forming a phase change material in the opening between the number of insulator regions includes forming a self-aligned contact for the phase change material and the bottom electrode.

3. The method of claim 1, wherein forming the number of dielectric spacers on the number of insulator regions and removing the portion of the number of dielectric spacers to form the contoured opening between the number of insulator regions and to expose the bottom electrode material defines a contact area for the phase change material and the bottom electrode.

4. The method of claim 1, wherein the method includes removing the sacrificial material of the number of memory structure regions and a portion of the number of insulator regions by reactive ion etching (RIE).

5. The method of any one of claims 1-4, wherein the method includes forming a top electrode over the phase change material.

6. The method of any one of claims 1-4, wherein the phase change material is a Germanium-Antimony-Tellurium (GST) material.

7. The method of any one of claims 1-4, wherein an amount of phase change material formed in the opening between the number of insulator regions is controlled by the size of the dielectric spacers on the insulator regions.

8. A method of forming memory cells, comprising:

removing a sacrificial material and a portion of a number of insulator regions to form a contoured opening between the number of insulator regions;

forming a number of spacers on the number of insulator regions to further define the contoured opening between the number of insulator regions; and

forming a phase change material in the contoured opening between the number of insulator regions.

9. The method of claim 8, wherein forming the phase change material in the contoured opening between the number of insulator regions creates a self-aligned contact between the phase change material and a bottom electrode.

10. The method of claim 8, wherein the method includes forming a phase change material in the contoured opening between the number of insulator regions by physical vapor deposition (PVD).

11. The method of claim 8, wherein forming a number of spacers on the number of insulator regions defines a contact area between the bottom electrode material and the phase change material.

12. The method of any one of claims 8-11, wherein the method includes forming a top electrode over the phase change material.

13. The method of any one of claims 8-11, wherein forming a number of spacers on the number of insulator regions to further define the contoured opening between the number of insulator regions includes removing a portion of the number of spacers.

14. A method of forming a memory array, comprising:

forming a number of memory structure regions, wherein the memory structure regions include a bottom electrode material and a sacrificial material;

forming a number of insulator regions between the number of memory structure regions;

forming a number of openings between the number of insulator regions and forming a contoured surface on the number of insulator regions by removing the sacrificial material and a portion of the number of insulator regions;

forming a number of dielectric spacers on the number of insulator regions;

forming a conductive material in the opening between the number of insulator regions;

forming a phase change material over the conductive material and a top electrode material over the phase change material;

removing a portion of the phase change material and the top electrode material to form an opening that exposes a portion of the number of insulator regions; and

forming a dielectric material in the opening that exposed the portion of the number of insulator regions.

15. The method of claim 14, wherein forming the dielectric material in the opening that exposed the portion of the number of insulator regions isolates the memory cell from adjacent memory cells.

16. The method of claim 15, including forming the conductive material in the opening between the number of insulator regions by physical vapor deposition

(PVD) and using chemical mechanical planarization (CMP) to remove a portion of the conductive material to a top surface of the insulator regions.

17. The method of claim 15, wherein forming the conductive material in the opening between the number of insulator regions creates a self-aligned contact between the bottom electrode material and the phase change material.

18. The method of any one of claims 14-17, wherein forming the dielectric material in the opening that exposed the portion of the number of insulator regions isolates adjacent memory cells from each other in the memory array.

19. The method of claim 18, wherein a contact between the phase change material and the top electrode is self-aligned.

20. A memory cell, comprising:

a bottom electrode;

a phase change material, wherein the phase change material contacts the bottom electrode in an opening between a number of insulator regions that include spacers with contoured surfaces and the contact area between the bottom electrode and the phase change material is defined by a distance between the number of insulator regions; and

a top electrode, wherein the top electrode is formed over the phase change material.

21. The memory cell of claim 20, wherein the phase change material contacts the bottom electrode in a self-aligned opening between the number of insulator regions.

22. The memory device of any one of claims 20-21, wherein the spacers are formed on the number of insulator regions and further define the distance between the number of insulator regions.

23. The memory device of any one of claims 20-21, wherein the phase change material is a Germanium-Antimony-Tellurium (GST) material.

What is claimed is:

1. A method of forming a memory structure, comprising:

forming a number of memory structure regions, wherein the memory structure regions include a bottom electrode material and a sacrificial material;

forming a number of insulator regions between the number of memory structure regions;

forming a number of openings between the number of insulator regions, forming a contoured surface on the number of insulator regions, and exposing the bottom electrode material by removing the sacrificial material and a portion of the number of insulator regions;

forming a number of dielectric spacers on the contoured surface of the number of insulator regions to create a contoured opening between the number of insulator regions; and

forming a phase change material on the number of dielectric spacers and in the contoured opening between the number of insulator regions.

2. The method of claim 1, wherein forming a phase change material in the contoured opening between the number of insulator regions includes forming a self-aligned contact for the phase change material and the bottom electrode.

3. The method of claim 1, wherein forming a number of dielectric spacers on the number of insulator regions defines a contact area for the phase change material and the bottom electrode.

4. The method of claim 1, wherein the method includes removing the sacrificial material of the number of memory structure regions and a portion of the number of insulator regions by reactive ion etching (RIE).

5. The method of claim 1, wherein the method includes forming a top electrode over the phase change material.

6. The method of claim 1, wherein the phase change material is a Germanium-Antimony-Tellurium (GST) material.

7. The method of claim 1, wherein the amount of phase change material formed in the contoured opening between the number of insulator regions is controlled by the size of the dielectric spacers on the contoured surface of the insulator regions.

8. A method of forming memory cells, comprising:

removing a sacrificial material and a portion of a number of insulator regions to form a contoured opening between the number of insulator regions;

forming a number of spacers on the number of insulator regions to further define the contoured opening between the number of insulator regions; and

forming a phase change material on the number of spacers and in the contoured opening between the number of insulator regions.

9. The method of claim 8, wherein forming the phase change material on the number of spacers and in the contoured opening between the number of insulator regions creates a self-aligned contact between the phase change material and a bottom electrode.

10. The method of claim 8, wherein the method includes forming the phase change material on the number of spacers and in the contoured opening between the number of insulator regions by physical vapor deposition (PVD).

11. The method of claim 8, wherein forming the number of spacers on the number of insulator regions defines the contact area between the bottom electrode material and the phase change material.

12. The method of claim 8, wherein the method includes forming a top electrode over the phase change material.

13. The method of claim 8, wherein forming the number of spacers on the number of insulator regions to further define the contoured opening between the number of insulator regions includes removing a portion of the number of spacers.

14. A method of forming a memory array, comprising:

forming a number of memory structure regions, wherein the memory structure regions include a bottom electrode material and a sacrificial material;

forming a number of insulator regions between the number of memory structure regions;

forming a number of openings between the number of insulator regions, forming a contoured surface on the number of insulator regions, and exposing the bottom electrode material by removing the sacrificial material and a portion of the number of insulator regions;

forming a number of dielectric spacers on the number of insulator regions to create a contoured opening between the number of insulator regions;

forming a conductive material on the number of dielectric spacers and in the contoured opening between the number of insulator regions;

forming a phase change material over the conductive material and a top electrode material over the phase change material;

removing a portion of the phase change material and the top electrode material to form an opening that exposes a portion of the number of insulator regions; and

forming a dielectric material in the opening that exposed the portion of the number of insulator regions.

15. The method of claim 14, wherein forming a dielectric material in the opening that exposed the portion of the number of insulator regions isolates the memory cell from adjacent memory cells.

16. The method of claim 15, the method includes forming the conductive material on the number of dielectric spacers and in the contoured opening between the number of insulator regions by physical vapor deposition (PVD) and using chemical mechanical planarization (CMP) to remove a portion of the conductive material to a top surface of the insulator regions.

17. The method of claim 15, wherein forming the conductive material on the number of dielectric spacers and in the contoured opening between the number of insulator regions creates a self-aligned contact between the bottom electrode material and the phase change material.

18. The method of claim 14, wherein forming the dielectric material in the opening that exposed the portion of the number of insulator regions isolates adjacent memory cells from each other in the memory array.

19. The method of claim 18, wherein a contact between the phase change material and the top electrode is self-aligned.