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Comparator Circuit for an Integrator

The invention relates to a comparator circuit for an integrator.

State of the Art

In many electrical circuits, it is necessary to detect the level of the signals and to alter the output signals in respect of their logic level in dependence on the instantaneous height of this level, e.g. for ramp function generators making use of an integrator.

The comparator function may be formed by means of integrated comparators, e.g. of the Type LM 111 from the manufacturer National Semiconductor, and the integrator function by using e.g. an operational amplifier of the Type 741 or a reverse-coupled transistor. A combination of the two can be integrated on a chip.

Normally however, for a defined manner of operation of the comparator, its input voltage has to lie in a range of ca. 1 - 2 V above earth potential and ca. 1 - 2 V below the operating voltage. The input voltage range that can be utilised is thus appreciably limited with respect to the operating voltage.

Of course, there are comparators e.g. Type LM 193 from the manufacturer National Semiconductor, in which the input voltage can be used down to earth potential. However, the



upper limit of the input voltage range is ca. 1 - 2 V below the operating voltage even with this type.

Moreover, the circuits for such known comparators are relatively expensive and a relatively large chip surface for an integrated comparator circuit for an integrator would be need.

Invention

The object of the invention is to provide a comparator circuit having an extended input voltage range and reduced circuit costs for an integrator.

This object is achieved by the features specified in claim 1. Advantageous developments of the invention are specified in the dependent claims.

In the comparator circuit in accordance with the invention, the saturation of complementary transistors that are controlled by the integrator are utilised such that the comparator outputs only switch when the saturation voltages are attained. The corresponding saturation voltage V_{CEsat} of each of the complementary transistors amounts to ca. 50 mV. Two comparator outputs may be provided for example. The one output alters its logic level when the input voltage of the comparator circuit attains a first threshold value (earth potential + V_{CEsat}) and the other output when the input voltage of the comparator circuit attains a second threshold value (operating voltage - V_{CEsat}).

The output transistor for the first threshold value is controlled by an NPN transistor for example and the output transistor for the second threshold value by a PNP transistor.

Drawings

An embodiment of the invention will be explained hereinafter by means of the drawings. These depict in



Fig. 1 a known comparator circuit for an integrator,

Fig. 2 a comparator circuit for an integrator in accordance with the invention.

Fig. 3 current and voltage diagrams for the comparator circuit when current is flowing into the input 24

Fig. 4 current and voltage diagrams for the comparator circuit when current is flowing out of the input 24

An integrator consisting of an amplifier 10 and an integrating capacitor 11 is illustrated in Fig. 1. Two differential amplifiers 12 and 13 are connected to the output of this integrator. These are connected to an operating voltage 26 (V_{cc}) and to earth potential 27. The reference voltage V_{low} is present on one input 131 of the first differential amplifier 13 and the reference voltage V_{high} is present on one input 121 of the second differential amplifier 12. The voltage V_{high} on the input 121 of the second differential amplifier 12 may then adopt a maximum value ($V_{cc} - 2V$) for example and the voltage V_{low} on the input 131 of the first differential amplifier 13 may adopt a minimum value (earth potential + 1V) for example. The maximum input voltage sweep of the comparator is thus 2 to 3V lower than the operating voltage 26 and a correspondingly integrated combination of an integrator and a comparator needs a relatively large chip surface.

Embodiments

Fig. 2 shows an integrator which consists of the transistors 241 and 242 and the integrating capacitor 21. The integrator is controlled by a current at the input 24 and receives its feed current from a transistor 251 connected up as a current mirror. This delivers an image of the current from the current source using transistor 252.



The integrating capacitor 21 is connected likewise to the mirrored current source using transistor 251.

If a current flows into the input 24, then the voltage at the junction of the transistors 251 and 242 with the integrating capacitor 21 falls because this capacitor is discharged. The voltage at this junction progressively approaches the value zero. This process ends when transistor T 242 is saturated and has a saturation voltage between the collector and emitter of ca. 50 mV. A base current thereby flows in the transistor 242. This base current also flows through the collector of the transistor 241 and is drawn off from resistor 255 and consequently does not flow into the transistor 256. The voltage across transistor 257 thus falls and the transistor 23 blocks. If more current flows into the input 24, then the transistor 241 also saturates so that advantageously, this current does not flow into the integrating capacitor 21, but rather, into the base of the transistor 241. The lower level of the voltage at the above-mentioned junction 251, 242 and 21 is thus detected by the blocking transistor 23. Advantageously, the current through the transistor 252 is only affected in a very small way by the voltage fluctuation at the collector of transistor 241 when the transistor 241 saturates.

If a current flows out from the input 24, then the voltage at the junction of the transistors 251 and 242 with the integrating capacitor 21 rises because this capacitor is charged. The voltage at this junction progressively approaches the operating voltage 26 (Vcc). This process ends when transistor T 251 is saturated and has a saturation voltage between the collector and emitter of ca. 50 mV. A base current thereby flows in the transistor 251. This base current is delivered through the collector of the transistor 253 and then further, through the resistor 254. The voltage across the resistor 254 thereby rises and the transistor 22 becomes conductive. The upper level of the voltage at the above-mentioned junction 251, 242 and 21 is thus detected by the conductive transistor 22.



In this way, a voltage range of $(V_{cc} - 2 \cdot V_{CEsat})$ can advantageously be used for the comparator.

Due to the low circuit outlay needed for the comparator that is combined with the integrator, the chip surface required therefor in the integration process is advantageously small and the feed current for this circuit is advantageously very low.

If the outputs 222 and 232 of the comparator are used in order to reverse the respective poles of a current source for example and, if this current source is connected only to the input 24, then a ramp function generator ensues. Its output voltage can be derived from the connection point of the integrating capacitor 21 and the transistors 242 and 251.

In Fig. 3, there are illustrated some current and voltage versus time waveforms in the comparator circuit in accordance with Fig. 2 for the case where a current is flowing into the input 24. The meanings therein are:

- $i_b(q2)$ the base current of transistor 242
- $i_c(q1)$ the collector current of transistor 241
- $i_e(q5)$ the emitter current of transistor 256
- $i_b(q1)$ the base current of transistor 241
- $v(k1)$ the voltage on the collector of transistor 242
- $v(k2)$ the voltage on the collector of transistor 256
- $v(k6)$ the voltage on the base of transistor 242
- $v(k5)$ the voltage on the base of transistor 23
- $v(k232)$ the voltage on the collector of transistor 23
when this is connected via a resistor to the
operating voltage 26

In Fig. 4, there are illustrated some current and voltage versus time waveforms in the comparator circuit in



accordance with Fig. 2 for the case where a current is flowing out of the input 24. The meanings therein are:

- ic(q3) the collector current of transistor 251
- ic(q4) the collector current of transistor 253
- ib(q3) the base current of transistor 251
- v(k1) the voltage on the collector of transistor 242
- v(k6) the voltage on the base of transistor 242
- v(k4) the voltage on the base of transistor 22
- v(k222) the voltage on the collector of transistor 22
when this is connected via a resistor to the
operating voltage 26

If V_{cc} has a value of 5 V for example, then the utilisable voltage sweep $(5 \text{ V} - 2 \times 0.05 \text{ V}) = 4.9 \text{ V}$. A ramp function having a period of 10 μsec for example can thereby be realised in the case of an appropriate magnitude of the integrating capacitor 21.

In a corresponding, known circuit, only a voltage sweep of $(V_{cc} - 2.5 \text{ V}) = 2.5 \text{ V}$ for example can be utilised. In order to realise a ramp function having the same period, the integrating capacitor 21 would have to have a value of virtually double and correspondingly, would need a chip surface of virtually double the area.



Claims

1. Comparator circuit for an integrator, characterised by transistors (242, 251) controlled by the integrator, the transistors being controlled up to saturation and from their saturation and desaturation there being derived the output signals (222, 232) of the comparator circuit.
2. Comparator circuit according to claim 1, characterised in that the transistors controlled by the integrator are complementary transistors (242, 251).
3. Comparator circuit according to claim 1 or 2, characterised in that the integrator has a current controlled input (24).
4. Comparator circuit according to claim 1, 2 or 3, characterised in that a current source (transistor 252) and a correspondingly reflected current source (transistor 251) is contained.
5. Comparator circuit according to one or more of claims 1 to 4, characterised in that the integrator contains an integration capacitor (21) fed by the reflected current source (transistor 251).

