"A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF PRODUCTION THEREOF".

The present invention relates to a technique which is effective when applied to a semiconductor integrated circuit device. More particularly, the present invention relates to a technique which is effective when applied to a semiconductor integrated circuit device provided with small holes or grooves (e.g. moats, or trenches, formed in the substrate surface).

In order to increase memory capacity, the integration density of a semiconductor integrated circuit device equipped with a dynamic random-access memory (hereinafter called "DRAM") using series circuits of a data storage capacitance element and a switching element as memory cells tends to increase.

There has previously been proposed a technique of improving the integration density of a DRAM by forming small holes or grooves (e.g. moats or trenches) in a main surface of a semiconductor substrate by anisotropic etching, and providing an insulating film along the surface within each moat or trench and a conductive layer over the moat or trench to form a vertical data storage capacitance element, and thus reduce the plan area of each memory cell (Japanese Patent Publication No.

12739/1983).

As a result of experiments and studies on this prior technique, however, we have discovered that, since the corners of the small moats or trenches, produced by anisotropic etching, have an acute-angled shape, reductions in the thickness of the insulating film and the electric field concentration are likely to occur at the corners, so that the electrostatic destruction voltage (dielectric breakdown voltage) of the insulating film of each data storage capacitance element drops markedly.

The results of experiments which we have carried out has revealed that the electrostatic destruction voltage of the insulating film of a vertically-formed data storage capacitance element is only about 50 to 60% of the electrostatic destruction voltage of the insulating film of a flat (horizontal) data storage capacitance element.

If the electrostatic destruction voltage of the insulating film of a data storage capacitance element drops, it is very likely that short-circuits will occur between the semiconductor substrate, which is held at a predetermined potential, and a conductive layer which is held at a different potential. If a short-circuit occurs, the charge stored as data will be lost, and hence

the electrical reliability of the DRAM will deteriorate.

It is therefore an object of the present invention to improve the electrical reliability of semiconductor device, in particular a semiconductor integrated circuit device.

It is another object of the present invention to smooth the acute-angled shape of each corner of small trenches or moats (holes or grooves) in a semiconductor integrated circuit device having such small trenches or moats (holes or grooves).

It is a third object of the present invention to provide an improvement in the electrostatic destruction voltage of an insulating film in a semiconductor integrated circuit device provided with small trenches or moats (holes or grooves) formed in a main surface of a semiconductor substrate, the insulating film being provided along the surface within the small trench or moat (hole or groove), and a conductive layer being formed over the insulating film.

It is a fourth object of the present invention to provide an improvement in the electrostatic destruction voltage of an insulating film and the prevention of the loss of charge stored as a data storage capacitance element consisting, in turn, of a small trench or moat (hole or groove) formed in a main surface of a

semiconductor substrate, an insulating film arranged along the surface within the small trench or moat (hole or groove), and a conductive layer arranged over the insulating film, and a switching element connected in series with the data storage capacitance element.

According to a first aspect of the present invention there is provided a semiconductor device including: a trench in a main surface of a semiconductor substrate, said trench having substantially vertical walls and extending from said main surface into the interior of said semiconductor substrate, said trench having its initially formed sharp corners rounded-off; an insulating film formed over said surface of said semiconductor substrate and along the surface within said trench; and a conductive layer formed over said insulating film, wherein the radius of the rounded-off corners of the trench is at least three times the thickness of the insulating film.

According to a second aspect of the present invention there is provided a method of producing a semiconductor device including the steps of: forming a trench in a main surface of a semiconductor substrate such that said trench has substantially vertical walls and extends from said main surface into the interior of said semiconductor substrate, whereby said trench includes sharp corners; rounding off said sharp corners; forming an insulating film over said main surface of said semiconductor substrate and along the surface within said trench; and

forming a conductive layer over said insulating film, the radius of the rounded-off corners of the trench being at least three times the thickness of the insulating film.

It should be noted that in the following description and claims, the "trench" as described includes, e.g. holes, grooves, moats, trenches, etc., formed in the semiconductor substrate and, in general, refers to any opening formed in the semiconductor substrate and having, e.g. acute-angled corners, and being usable for purposes of the present invention.

In a preferred form of the invention, a silicon nitride film and an etching mask are sequentially formed over a main surface of a semiconductor substrate, and the silicon nitride film and the semiconductor substrate are then selectively etched using the etching mask, to form a heat-resistant treatment mask and a small trench in the semiconductor substrate. Thereafter, an insulating film is formed along the surface within the small trench, using the heat-resistant treatment mask, and is then removed selectively to form a small trench whose sharp corners (acute-angled corners) are smoothed (rounded off).

Thus, generally, the present invention provides for trenches, in the semiconductor substrate, wherein the corners thereof are rounded off, e.g. curved. Since the reduction in the thickness of the insulating film at the corners and the field concentration at these portions can

be restricted by forming the insulating film and a conductive layer in a small trench whose sharp corners have been smoothed (rounded off), in the way described above, for example, the electrostatic destruction voltage of the insulating film can be improved.

The present invention will now be described in greater detail by way of example with reference to and as illutrated in the accompanying drawings, wherein:-

Figure 1 is an equivalent circuit diagram of principal portions of a memory cell array of a DRAM, which is useful for illustrating an embodiment of the present invention;

Figure 2 is a plan view of principal portions of a memory cell array of a DRAM, which is useful for illustrating the structure of an embodiment of the invention;

Figure 3 is a section taken along the line III-III of Figure 2;

Figures 4 to 9 are sections through principal portions of a data storage capacitance element of a DRAM memory cell at each production step, which illustrate a preferred method of producing an embodiment of the present invention;

Figure 10 is a section through principal portions of a DRAM memory cell provided as a model for measuring the

dielectric breakdown voltage of an insulating film of a data storage capacitance element utilizing a small trench;

Figure 11 is an enlarged section through a corner of the small trench of Figure 10;

Figure 12 is a graph of the results of calculations on the electrostatic destruction voltage of an insulating film, obtained using the model shown in Figures 10 and 11;

Figure 13 is a graph of the results of experiments on the electrostatic destruction voltage of an insulating film when the present invention is not applied; and

Figures 14 to 16 are graphs of the results of experiments on the electrostatic destructin voltage of an insulating film when the present invention is applied.

Referring to Figure 1 which is an equivalent circuit diagram of the principal portions of a memory cell array of a DRAM, the circuit includes:

(a) sense amplifiers SA1, SA2... each of which amplify a minute potential difference between a predetermined memory cell and a predetermined dummy cell, which will be described later;

(b) bit lines BL11, BL12 extending from one end of the sense amplifier SA1 in the row direction, and bit lines BL21, BL22 extending from one end of the sense

amplifier SA2 in the row direction, these bit lines transmitting charge as data;

(c) word lines WL1, WL2 which extend in the column direction being connected to predetermined gate electrodes constituting switching MISFETs of the dummy cells, and which turn on and off each MISFET;

(d) word lines WL3, WL4 which extend in the column direction being connected to predetermined gate electrodes constituting switching MISFETs of the memory cells, and which turn on and off each MISFET.

(e) memory cells M11, M12, M21, M22 ... which hold charge acting as data each of the memory cells M11, M12, M21, M22 ... comprising a MISFET Q11, Q12, Q21, Q22 ... of which one end is connected to a predetermined bit line BL, and a gate electrode thereof is connected to a predetermined word line WL, and a data storage capacitance element C11, C12, C21, C22 ... of which one end is connected to the other end of the corresponding MISFET Q11, Q12, Q21, Q22 ..., and the other end thereof is connected to a fixed potential Vss terminal at, for instance, earth potential (0 V), or a substrate bias potential (-2.5 to 3.0 V);

(f) dummy cells D11, D12, D21, D22 which hold a charge which can detect logic "1" and "0" used as data in the memory cells M, each dummy cell D11, D12, D21, D22

... comprising a MISFET QD11, QD12, QD21, QD22 ... of which one end is connected to a predetermined bit line, and whose gate electrode is connected to a predetermined word line WL, a data-detecting capacitance element CD11, CD12, CD21, CD22 ... of which one end is connected to the other end of the corresponding MISFET QD11, QD12, QD21, QD22 ... and whose other end is connected to the fixed potential Vss terminal at, for instance, earth potential or the substrate bias potential, and a clear MISFET CQ for clearing the charge stored in the data-detecting capacitance element CD11, CD12, CD21, CD22 ...; and

(g) a terminal QD which is connected to the gate electrode of the clear MISFET CQ.

The specific construction of this embodiment will now be described with reference to Figures 2 and 3.

The DRAM is constituted by a p^--type semiconductor substrate made of single-crystal silicon. A field-insulating film (device-separation insulating film) is formed on the main surface of the semiconductor substrate 1 in such a manner that it is positioned between a predetermined memory cell and peripheral circuits (not shown) such as semiconductor element-forming regions (active regions) of an address select circuit, a read circuit, a write circuit, etc., known in the art. The insulating film 2 isolates these semiconductor element-

forming regions from one another.

The memory cells of the DRAM are surrounded and defined by the field insulating film 2 which defines a pair of patterns that repeat in the direction in which bit lines extend.

A small trench 3 is formed (e.g., etched, bored, etc.) in the main surface of the semiconductor substrate 1 within the region in which the data storage capacitance element is to be formed, so as to extend inward from the main surface of the element region, this small trench constituting part of the data storage capacitance element. The small trench 3 forms a three-dimensional data storage capacitance element, to reduce the plan area needed for the formation of the data storage capacitance element and to improve the integration density of the DRAM.

The acute-angled shape of all the corners of the small trench 3 is smoothed (rounded off) to a predetermined shape.

An insulating film 4 is formed over the main surface of the semiconductor substrate 1 in the data storage capacitance element region, at least along the surface within the small trench 3. This insulating film 4 will constitute part of an MIS data storage capacitance element. Since the acute-angled shape of the corners of

the small trench 3 has been smoothed, no marked reduction in the film thickness of the insulating film 4, e.g., at the corners, occurs.

A conductive plate 5 is positioned over the insulating film 4 and is electrically connected to other conductive plates adjacent thereto. The conductive plate 5 will constitute part of the MIS data storage capacitance element. The conductive plate 5 consists of, e.g. a doped polycrystalline silicon layer, for example, and is formed by a conductive layer-forming step at the first layer in the production process.

The data storage capacitance element C of each memory cell of the DRAM consists primarily of the semiconductor substrate 1, the small trench 3, the insulating film 4, and the conductive plate 5. When the conductive plate 5 is connected to a potential of about 5V, for example, the data storage capacitance element C defines a depletion layer extending inward from the main surface of the semiconductor substrate 1, and stores as data a charge that is transmitted from the bit lines to the depletion layer through a switching element.

Since the sharp corners of the small trench are smoothed, the marked reductions in the film thickness of the insulating film 4 and the electric field concentration at the corners can be restricted.

Accordingly, the electrostatic destruction voltage of the insulating film 4 is improved, and no short-circuits between the semiconductor substrate 1 and the conductive plate 5 occur, so that the charge stored as data in the data storage capacitance element does not disappear.

An insulating film is arranged in such a manner that it covers the conductive plate 5 and electrically isolates the plate from a word line which will be formed on the insulating film.

An insulating film 7 is formed over the main surface of the semiconductor substrate 1 in a switching element region, this insulating film 7 primarily constituting the gate insulating film of the MISFET

A conductive layer 8 is formed over the insulating film 7, and which constitutes the gate electrode of the MISFET.

A conductive layer 9 is electrically connected to, and integrated with, the conductive layer 8 in the column directions, so as to extend over the insulating film 6. This conductive layer will constitute a word line WL.

In order to reduce resistance and improve the data read and write speeds, the conductive layers 8 and 9 are formed by depositing metal layers having a high melting point (e.g. refractory metals), or layers of a compound between a high melting point metal and silicon (e.g. a

silicide), onto the polycrystalline silicon layers 8A and 9A, respectively. They are formed by a second conductive layer-forming step in the production process. It is possible to use molybdenum, tungsten, titanium, tantalum, or the like as the high melting point metal, or a silicode of one of those metals.

Semiconductor regions 10 which are of the n^+-type are formed in the semiconductor substrate, extending to the main surface of the semiconductor substrate 1 on either side of the conductive layer 8. These regions are used as source and drain regions, and constitute part of the MISFET.

A MISFET Q acting as the switching element of the memory cell of a DRAM consists primarily of the semiconductor substrate 1, the conductive layer 8, the insulating film 7, and a pair of semiconductor regions 10.

Each memory cell includes a data storage capacitance element and a MISFET Q.

An insulating film 11 is positioned in such a manner that it covers the conductive layers 8 and 9, and isolates them electrically from a bit line which will be formed thereon. A phosphosilicate glass film, which can be subjected to glass flow, can be used as the insulating film 11.

A contact hole 12 is formed by selectively removing the insulating films 7 and 11 over the semiconductor region 10, which provides an electrical connection with the bit line which will be disposed on the insulating film 11.

A conductive layer is electrically connected to the semiconductor region 10 through the contact hole 12, and extends in the row direction over the insulating film 11. This layer constitutes the bit line BL. The conductive layer 13 consists of, for example, an aluminium layer, and is formed by a third conductive layer-forming step in the production process.

Specific details of the production method of this embodiment of this invention will now be described with reference to Figures 4 to 9 which are sections through principal portions of the data storage capacitance element of a memory cell of a DRAM at each production step.

First of all, a p^--type semiconductor substrate 1 is prepared. An insulating film 2A is formed over one main surface of the semiconductor substrate in a region thereof in which the semiconductor elements will be formed, and a field-insulating film 2 is formed over the portions of the substrate 1 other than the semiconductor element region.

Mask-forming materials 14 and 15 are sequentially deposited onto the insulating film 2A and the field-insulating film 2, respectively, as shown in Figure 4, for the formation of a small trench. A phosphosilicate glass film formed by chemical vapour deposition (hereinafter called "CVD"), for example, is used as the mask-forming material 15 acting as an etching mask for the formation of the small trench, and the film thickness can range from about 0.8 to about 1.2 μm, for example. A silicon nitride film formed by CVD, for example, is used as the mask-forming material 14 for the mask used to smooth the sharp corners of the small trench, its thickness being about 0.04 to 0.06 μm, for example.

After the step shown in Figure 4, the mask-forming material 15 of the small-trench region within the data storage capacitance element region is selectively removed by dry etching utilizing CHF_3 gas, to form a mask 15A resistant to etching. The mask-forming material 14, the insulating film 2A, and the semiconductor substrate 1 are then removed selectively using mainly the mask 15A, to form the small trench 3A in the main surface of the semiconductor substrate 1 as shown in Figure 5. A mask 14A for a heat-resistant treatment is also formed by substantially the same process of forming small trench 3A, which mask 14A is self-aligned with the small trench

3A. The small trench 3A has a size of about 1.0 x 1.5 μm^2, for example, and is formed by anisotropic (dry) etching utilizing CHF_3 gas in order to minimize the plan area of the data storage capacitance element. It has a depth of about 4.0 to 6.0 μm, extending inward from the main surface of the semiconductor substrate 1. Since the small trench 3A is formed by anisotropic etching, its corners have an acute-angled shape.

After the step shown in Figure 5, the mask 15A is removed to expose the mask 14A. Using this mask 14A, an insulating film 16 is formed over the main surface of the semiconductor substrate 1 along the surface within the small trench 3A, in order to smooth the sharp corners of the small trench 3A, as shown in Figure 6. The insulating film 16 consists of, for example, a silicon oxide film formed by thermal oxidation (e.g. SiO_2), and its thickness of about 0.03 to 0.20 μm.

The thickness of the insulating film 16 drops markedly at sharp corners 16B at the bottom of the small trench 3A and increases at sharp corners 16A at the mouth of the small trench 3A, so that it is formed non-uniformly overall. However, the sharp corners 16A and 16B in the main surface of the semiconductor substrate 1 below the insulating film 16 are smoothed, so that an arc shape is provided thereat (e.g. the corners are rounded

off). Thus, in the present embodiment, the forming of the insulating film 16, using the semiconductor substrat for the formation thereof, acts to round off the corners.

After the step shown in Figure 6, the insulating film 16 is selectively removed by conventional wet etching using the mask 14A as an etching mask, and the small trench 3 whose sharp corners have been smoothed is formed as shown in Figure 7.

The steps of forming and removing the insulating film 16 do not exert any adverse effect on the other portions, such as changing the thickness of the field insulating film 2, because the mask 14A is provided.

As will be described later, we have confirmed that the small trench 3 whose sharp corners have been smoothed to an arc shape of radius of at least, e.g. 0.03 μm in this embodiment ensures that the insulating film of a data storage capacitance element which is formed three-dimensionally therein can provide an electrostatic destruction voltage of about 70 to 90% that of a flat film.

After the step shown in Figure 7, the mask 14A and the insulating film 2A are removed, as done conventionally for removing, e.g. silicon nitride and silicon oxide films, to expose the main surface of the semiconductor substrate, as shown in Figure 8.

After the step shown in Figure 8, an insulating film 4 is formed over the exposed main surface of the semiconductor substrate 1, as shown in Figure 9. In order to form the insulating film of the data storage capacitance element, the insulating film 4 can be a silicon oxide film (e.g. SiO_2) formed by thermal oxidation, for example, and its film thickness can be about 0.01 to 0.03 μm. In order to increase its dielectric constant and store a greater quantity of charge as data, the insulating film 4 may consist of an approximately 0.01 μm thick silicon oxide film (e.g. SiO_2) formed by thermal oxidation, and an approximately 0.02 μm thick silicon nitride film deposited by CVD on the silicon oxide film, for example.

Since the sharp angles at the corners are smoothed, the insulating film 4 is formed over the main surface of the semiconductor substrate 1, and along the surface within the small trench 3, at a substantially uniform thickness.

Thereafter, standard production steps are used to complete the DRAM of this embodiment shown in Figures 2 and 3.

The effect of this embodiment will now be described.

Figure 10 is a section through principal portions of the DRAM memory cell provided as a model in order to

measure the electrostatic destruction voltage of the insulating film of a data storage capacitance element utilizing a small trench; Figure 11 is an enlarged section through a corner of the small trench in Figure 10; Figure 12 is a graph of the results of calculations of the electrostatic destruction voltage of the insulating film, obtained by using the model shown in Figures 10 and 11; Figure 13 is a graph of the results of experiments on the electrostatic destruction voltage of an insulating film when the present invention is not applied; and Figures 14 to 16 are graphs of the results of experiments on the electrostatic destruction voltage of an insulating film when the present invention is applied.

In Figures 10 and 11, reference numerals 3a and 3b denote portions whose sharp angles have been smoothed to a cylindrical shape, and 3c is a portion at which a projection, formed by the effect of foreign matter in the step of forming the small trench 3A, is smoothed to a spherical shape.

Symbol t_{ox} denotes the thickness of the insulating film 4, and r denotes the radius of the arc formed at the corner of the small trench 3.

In Figure 12, the ratio of the radius r to the thickness t_{ox} of the insulating film 4 (r/t_{ox}) is shown

along the axis of the abscissa, and the electrostatic destruction voltage of the insulating film 4 at the small trench 3, when the electrostatic destruction voltage of the insulating film 4 is 1.0 at a planar surface portion, is shown along the axis of the ordinate.

Curve A shows the electrostatic destruction voltage of the insulating film 4 at the portions 3a and 3b shaped into the cylindrical form, and curve B shows the electrostatic destruction voltage of the insulating film 4 at the portion 3c shaped into the spherical form.

As can be seen clearly from Figures 10 to 12, the breakdown voltage of the insulating film 4 can be improved to about 70 to 90% of the flat-portion value by smoothing the sharp corners of the small trench 3 to a radius which is at least three times the thickness t_{ox} of the insulating film 4.

If the thickness t_{ox} of the insulating film 4 is about 0.01 μm, for example, the radius r is to be about 0.03 μm to achieve the above-described results. Therefore, if the insulating film 16 is formed about 0.03 μm thick, the radius r can be about 0.03 μm, and a electrostatic destruction voltage of about 70 to 90% of the flat-portion value can be obtained for the insulating layer 4. The thickness of insulating film 16 can be, e.g. at least 0.03 μm.

In Figures 13 to 16, the electrostatic destruction voltage (V) of the insulating film 4 is shown along the axis of the abscissa, and the number of device which is destroyed when the voltage shown in abscissa is applied between the substrate 1 and electrode 5 along the axis of the ordinate.

Figure 13 shows the electrostatic destruction voltage when the insulating film 4 is formed directly over the surface of a small trench 3A whose sharp corners have not been smoothed.

Figure 14 shows the electrostatic destruction voltage when the insulating film 4 is formed over the surface of a small trench 3 whose sharp corners have been smoothed by the formation of an about 0.05 μm thick insulating film 16.

Figure 15 shows the electrostatic destruction voltage when the insulating film 4 is formed over the surface of a small trench 3 whose sharp corners have been smoothed by the formation of an about 0.10 μm thick insulating film 16.

Figure 16 shows the electrostatic destruction voltage when the insulating film 4 is formed over the surface of a small trench 3 whose sharp corners have been smoothed by the formation of an about 0.20 μm thick insulating film 16.

In all these cases, the thickness t_{ox} of the insulating film 4 is 0.02 μm.

As can be seen clearly from Figures 13 to 16, the formation of a data storage capacitance element in a small trench 3 whose sharp corners have been smoothed can improve the electrostatic destruction voltage of the insulating film 4 by at least about 20%, compared to the case in which the corners are not smoothed.

The above described embodiment has the following effects and advantages:

(a) A small trench whose sharp corners have been smoothed (rounded off) can be formed by forming (etching or boring) a small trench in the main surface of a semiconductor substrate so as to extend inward from the main surface, forming an insulating film along the surface of the small trench, and then selectively removing the insulating film.

(b) Since a small trench whose sharp corners have been smoothed can be obtained by the effect described in (a) above, the marked reductions in the thickness of the insulating film, and the electric field concentration at the corners of the small trench, can be restricted; and in a semiconductor device including the small trench, the insulating film provided over the main surface of the semiconductor substrate and along the surface within the

small trench, and a conductive layer formed over the insulating film, the electrostatic destruction voltage of the insulating film can be improved.

(c) Since a small trench whose sharp corners have been smoothed can be obtained by the effect described in (a) above, marked reductions in the thickness of the insulating film, and the electric field concentration at the corners of the small trench, can be restricted in a data storage capacitance element of a memory cell of a DRAM including the small trench; in a DRAM including the insulating film provided over the main surface of the semiconductor substrate and along the surface within the small trench, and a conductive layer formed over the insulating film, the electrostatic destruction voltage of the insulating film can be improved, and the loss of the charge stored as data can be prevented.

(d) Since the marked reductions in the thickness of the insulating film, and the electric field concentration at the corners of a small trench can be restricted, and the electrostatic destruction voltage of the insulating film can be improved, in a semiconductor device utilizing a small trench as described in (b) above, the electrical reliability of the semiconductor integrated circuit device can be improved.

(e) Since the marked reductions in the thickness of

the insulating film, and the electric field concentration at the corners of a small trench can be restricted, and the electrostatic destruction voltage can be improved, in a data storage capacitance element of a DRAM memory cell utilizing a small trench, and, moreover, since the loss of the charge stored as data can be prevented as described in (c) above, the electrical reliability of the DRAM can be improved.

Whilst the above described embodiment illustrates an example in which the present invention is applied to a data storage capacitance element of a DRAM memory cell utilizing a small trench, it will be appreciated that it is not specifically limited thereto, and can be applied to a capacitance element of a semiconductor integrated circuit device utilizing a small trench.

Attention is drawn to our copending application No 8819232 which has been divided from the present application.

CLAIMS:-



1. A semiconductor device including: a trench in a main surface of a semiconductor substrate, said trench having substantially vertical walls and extending from said main surface into the interior of said semiconductor substrate, said trench having its initially formed sharp corners rounded-off; an insulating film formed over said surface of said semicondctor substrate and along the surface within said trench; and a conductive layer formed over said insulating film, wherein the radius of the rounded-off corners of the trench is at least three times the thickness of the insulating film.

2. A semiconductor device according to claim 1, wherein the radius of the rounded-off corners is at least 0.03μm.

3. A semiconductor device according to claim 1 or 2, wherein said insulating film comprises a film of silicon oxide adjacent the main surface and along the surface of the trench, and a silicon nitride film on the silicon oxide film.

4. A semiconductor device according to any one of the preceding claims, wherein said semiconductor substrate is a silicon single crystal.

5. A semiconductor integrated circuit device including: a series circuit consisting of a data storage capacitance element, said data storage

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capacitance element have a trench formed in a main surface of a semiconductor substrate in such a manner that said trench has substantially vertical walls and extends from said main surface into the interior of said semiconductor substrate, said trench having its initially formed sharp corners rounded off; an insulating film formed over said main surface of said semiconductor substrate and along the surface within said trench; a conductive layer formed over said insulating film; and a switching element connected in series with said data storage capacitance element; wherein the radius of the rounded-off corners of said trench is at least three times the thickness of the insulating film.

6. A method of producing a semiconductor device including the steps of: forming a trench in a main surface of a semiconductor substrate such that said trench has substantially vertical walls and extends from said main surface into the interior of said semiconductor substrate, whereby said trench includes sharp corners; rounding off said sharp corners; forming an insulating film over said main surface of said semiconductor substrate and along the surface within said trench; and forming a conductive layer over said insulating film, the radius of the rounded-off corners of the trench being at least three times the thickness of the insulating film.

7. A semiconductor integrated circuit device constructed substantially as herein described with reference to and as illustrated in Figures 1 to 3 of the accompanying drawings.