

Claims

1. A method of fabricating a semiconductor device, comprising
  - (i) forming a III-V semiconductor material layer comprising a substrate layer and a device layer attached to the substrate layer; and
  - 5       (ii) forming an electrically conductive interlayer to the device layer prior to bonding the electrically conductive interlayer to a partially processed CMOS device layer having at least one transistor.
- 2 A method according to claim 1, further comprising, bonding the conductive interlayer  
10   to the partially processed CMOS device layer.
3. A method according to claim 1 or 2, wherein forming the III-V semiconductor material layer includes epitaxially depositing the device layer on the substrate layer.
- 15   4. A method according to any preceding claim, wherein the device layer includes an optoelectronic device having a top device surface, a bottom device surface and an active optical area between the top device and bottom device surfaces; the bottom device surface being attached to the substrate layer and passage of light is via the bottom device surface.
- 20   5. A method according to claim 4, wherein the substrate layer includes a light transmissible substrate.
6. A method according to claim 4, further comprising removing the substrate layer after  
25   the CMOS device layer is bonded to the electrically conductive interlayer.
7. A method according to claim 6, further comprising bonding a light transmissible substrate to the bottom device surface of the optoelectronic device after removal of the substrate layer.
- 30   8. A method according to any one of claims 4 to 7, further comprising forming vias and metal lines to electrically connect the at least one transistor of the CMOS device layer to the optoelectronic device.

9. A method according to any preceding claim, further comprising depositing a bonding material to the electrically conductive interlayer prior to bonding the CMOS device layer to the electrically conductive interlayer, and the method further comprises chemo-  
5 mechanically polishing the bonding material.

10. A method according to any preceding claim, wherein the electrically conductive interlayer includes indium tin oxide.

10 11. A semiconductor device, comprising  
a partially processed CMOS device layer having at least one transistor;  
a III-V semiconductor material layer comprising a substrate layer and a device layer attached to the substrate layer; and  
an electrically conductive interlayer attached to and sandwiched between the  
15 partially processed CMOS device layer and the device layer.

12. A semiconductor device according to claim 11, wherein the device layer includes an optoelectronic device having a top device surface, a bottom device surface, and an active optical area between the top device and bottom device surfaces, the bottom device  
20 surface being attached to the substrate layer and passage of light is via the bottom device surface.

13. A semiconductor device according to claim 12, wherein the substrate layer includes a light transmissible substrate.