

SEMICONDUCTOR STRUCTURE, MEMORY AND METHOD FOR OPERATING MEMORY

ABSTRACT

Disclosed are a semiconductor structure, a memory and a method for operating the memory. The semiconductor structure includes: a substrate; a first gate structure and a second gate structure that are located on a surface of the substrate and have a same thickness smaller than a preset thickness; and a first doped area and a second doped area that are located in the substrate and are respectively located on two sides of the first gate structure. The first gate structure forms a selection transistor with the first doped area and the second doped area; an orthographic projection of the second gate structure on the substrate is at least partially overlapped with the second doped area. The second gate structure and the second doped area form an antifuse bit structure. A breakdown state and a non-breakdown state of the antifuse bit structure are configured to represent different stored data.

[Fig. 1]