

ABSTRACT

A semiconductor device includes a first gate structure including a plurality of first conductive layers and a plurality of first insulating layers that are alternately stacked; an isolation insulating layer located in the first gate structure, the isolation insulating layer including a first line portion extending in a first direction, a plurality of first protrusions protruding from the first line portion towards one side of the first line portion in a second direction, and a plurality of second protrusions protruding from the first line portion towards another side of the first line portion in an opposite direction to the first protrusions, wherein the second direction is orthogonal to the first direction; a plurality of first memory patterns, wherein one of the plurality of first memory patterns surrounds one of the plurality of first protrusions; and a plurality of first passivation patterns, wherein one of the plurality of first passivation patterns is located between the first line portion and one of the plurality of first memory patterns.

FIG. 1A