CLAIMS

1. A semiconductor device, comprising:

a logic cell on a substrate, the logic cell including a PMOSFET region and an NMOSFET region; and

a first metal layer on the logic cell,

wherein the first metal layer includes,

a first power line and a second power line that extend parallel to each other along a first direction, and

a first lower line, a second lower line, and a third lower line respectively on a first wiring track, a second wiring track, and a third wiring track that are defined between the first power line and the second power line,

wherein the first, second, and third wiring tracks extend parallel to each other along the first direction,

the first lower line includes a first line and a second line that are spaced apart from each other in the first direction at a first distance,

the third lower line includes a third line and a fourth line that are spaced apart from each other in the first direction at a second distance different from the first distance,

the first line has a first convex end that faces the second line and a third convex end that is opposite to the first end,

the third line has a second end that faces the fourth line,

a curvature at the first end is the same as a curvature at the second end, and

a curvature at the third end is different from the curvature at the first end.

2. The semiconductor device of claim 1, wherein

the first distance corresponds to a tip-to-tip distance between the first line and the second line,

the second distance corresponds to a tip-to-tip distance between the third line and the fourth line, and

each of the first distance and the second distance is in a range of 24 nm to 60 nm.

3. The semiconductor device of claim 1 or claim 2, wherein

the second lower line includes a first protrusion and a second protrusion that are on opposite sides of the second lower line,

the first protrusion protrudes toward a first region between the first line and the second line, and

the second protrusion protrudes toward a second region between the third line and the fourth line.

4. The semiconductor device of claim 3, wherein

a line-width of each of the first, second, third, and fourth lines is constant in the first direction without being changed, and

a line-width of the second lower line is not constant based on the first protrusion and the second protrusion.

5. The semiconductor device of any one of claims 1 to 4, wherein the curvature at the third end is less than the curvature at the first end.

6. The semiconductor device of any one of claims 1 to 5, wherein the second end is convexly rounded.

7. The semiconductor device of any one of claims 1 to 6, further comprising:

a first active pattern and a second active pattern on the PMOSFET region and the NMOSFET region, respectively;

a device isolation layer on an upper portion of the substrate, the device isolation layer defining the first active pattern and the second active pattern;

a first channel pattern and a second channel pattern on the first active pattern and the second active pattern, respectively;

a plurality of first source/drain patterns on opposite sides of the first channel pattern, respectively;

a plurality of second source/drain patterns on opposite sides of the second channel pattern, respectively;

a gate electrode running across the first channel pattern and the second channel pattern, the gate electrode extending in a second direction that intersects the first direction;

an active contact connected to at least one of the first and second source/drain patterns; and

a gate contact connected to the gate electrode,

wherein the first metal layer is connected to the active contact and the gate contact.

8. A method of manufacturing the semiconductor device of any one of

claims 1 to 7,

wherein the first lower line and the third lower line are formed using a first photomask, and

the first power line, the second power line, and the second lower line are formed using a second photomask.

9. The method of claim 8,

wherein the first end and the second end are simultaneously formed by an elongation etching, and

the first distance and the second distance are defined by the elongation etched ends.

10. A semiconductor device, comprising:

a logic cell on a substrate, the logic cell including a PMOSFET region and an NMOSFET region; and

a first metal layer on the logic cell,

wherein the first metal layer includes,

a first power line and a second power line that extend parallel to each other along a first direction; and

a first lower line, a second lower line, and a third lower line respectively on a first wiring track, a second wiring track, and a third wiring track that are defined between the first power line and the second power line,

wherein the first, second, and third wiring tracks extend parallel to each other along the first direction,

the first lower line includes a first line and a second line that extend parallel

to each other along the first direction,

the third lower line includes a third line and a fourth line that extend parallel to each other along the first direction,

a tip-to-tip distance between the first line and the second line is a first distance,

a tip-to-tip distance between the third line and the fourth line is a second distance,

each of the first distance and the second distance is a specific distance having a value between about 24 nm and about 60 nm, and

the first distance and the second distance are different from each other,

the first line has a first convex tip that faces the second line and a third convex tip that is opposite to the first tip,

the third line has a second tip that faces the fourth line,

a curvature at the first tip is the same as a curvature at the second tip, and

a curvature at the third tip is different from the curvature at the first tip.

11. The semiconductor device of claim 10, wherein a curvature at a tip of each of the first line and the second line is the same as a curvature at a tip of each of the third line and the fourth line.

12. The semiconductor device of claim 11, wherein a curvature at a tip of the second lower line is different from the curvature at the tip of each of the first line and the second line.

13. The semiconductor device of claim 10, wherein

a tip of each of the first line and the second line is convexly rounded, and

a tip of each of the third line and the fourth line is convexly rounded.

14. A method of manufacturing the semiconductor device of any one of claims 10 to 13, wherein

the first lower line and the third lower line are formed using a first photomask, and

the first power line, the second power line, and the second lower line are formed using a second photomask.

15. A semiconductor device, comprising:

an active pattern on a substrate;

a device isolation layer that fills a trench defining the active pattern;

a source/drain pattern on the active pattern and a channel pattern connected to the source/drain pattern, the channel pattern including a first semiconductor pattern, a second semiconductor pattern, and a third semiconductor pattern that are sequentially stacked and spaced apart from each other;

a gate electrode that extends while running across the channel pattern, the gate electrode includes a first part between the active pattern and the first semiconductor pattern, a second part between the first semiconductor pattern and the second semiconductor pattern, a third part between the second semiconductor pattern and the third semiconductor pattern, and a fourth part on the third semiconductor pattern;

a gate dielectric layer between the channel pattern and the gate electrode;

a plurality of gate spacers on opposite sidewalls of the fourth part of the gate

electrode;

a gate capping pattern on a top surface of the gate electrode;

a first interlayer dielectric layer on the gate capping pattern;

an active contact that penetrates the first interlayer dielectric layer and is coupled to the source/drain pattern;

a gate contact that penetrates the first interlayer dielectric layer and couples to the gate electrode;

a second interlayer dielectric layer on the first interlayer dielectric layer;

a first metal layer in the second interlayer dielectric layer, the first metal layer connected to the active contact and the gate contact;

a third interlayer dielectric layer on the second interlayer dielectric layer; and

a second metal layer in the third interlayer dielectric layer,

wherein the first metal layer includes,

a first power line and a second power line that extend parallel to each other along a first direction, and

a first lower line, a second lower line, and a third lower line respectively on a first wiring track, a second wiring track, and a third wiring track that are defined between the first power line and the second power line,

wherein the first, second, and third wiring tracks extend parallel to each other along the first direction,

the first lower line includes a first line and a second line that are spaced apart from each other in the first direction by a first distance,

the third lower line includes a third line and a fourth line that are spaced apart from each other in the first direction by a second distance different from the first distance,

the first line has a first convex end that faces the second line and a third convex end that is opposite to the first end,

the third line has a second end that faces the fourth line,

a curvature at the first end is the same as a curvature at the second end, and

a curvature at the third end is different from the curvature at the first end.

16. The semiconductor device of claim 15, wherein

the first distance is a tip-to-tip distance between the first line and the second line,

the second distance is a tip-to-tip distance between the third line and the fourth line, and

each of the first distance and the second distance is in a range of about 24 nm to about 60 nm.

17. The semiconductor device of claim 15 or claim 16, wherein the second end is convexly rounded.

18. A method of manufacturing the semiconductor device of any one of claims 15 to 17,

wherein the first lower line and the third lower line are formed using a first photomask, and

the first power line, the second power line, and the second lower line are formed using a second photomask.