DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The invention disclosed in this specification and the like relates to a semiconductor device and a method for manufacturing the semiconductor device.

[0002]

In this specification and the like, a semiconductor device refers to all types of devices which can function by utilizing semiconductor characteristics, and includes in its category an electro-optical device, an image display device, a semiconductor circuit, and an electronic device.

BACKGROUND ART

[0003]

Attention has been drawn to a technique by which transistors are formed using semiconductor thin films formed over a substrate having an insulating surface. These transistors are widely used for electronic devices such as an integrated circuit (IC) and an image display device (also simply referred to as a display device). Although a silicon-based semiconductor material is a common material for a semiconductor thin film applicable to a transistor, an oxide semiconductor has been attracting attention as another material.

[0004]

For example, a technique for forming a transistor using an oxide semiconductor such as zinc oxide or an In-Ga-Zn-based oxide semiconductor is disclosed (see Patent Documents 1 and 2).

[0005]

Another technique is also disclosed: oxide semiconductor layers with different electron affinities (or lower levels of the conduction bands) are stacked to increase the carrier mobility of a transistor (see Patent Documents 3 and 4).

[References]

[Patent Documents]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-096055

[Patent Document 3] Japanese Published Patent Application No. 2011-124360

[Patent Document 4] Japanese Published Patent Application No. 2011-138934

DISCLOSURE OF INVENTION

[0007]

The reliability of semiconductor devices including transistors using an oxide semiconductor certainly needs to be improved for mass production. In particular, a decrease in reliability is caused by a variation or decrease in the electrical characteristics of the semiconductor devices.

[0008]

In view of the above, an object of one embodiment of the present invention is to provide a highly reliable semiconductor device including an oxide semiconductor.

[0009]

Miniaturization of a transistor is also essential for achieving high-speed operation, low power consumption, low costs, high integration, and the like of the transistor.

[0010]

Thus, another object of one embodiment of the present invention is to provide a semiconductor device that includes an oxide semiconductor and is miniaturized while keeping good electrical properties.

[0011]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Other objects are apparent from and can be derived from the description of the specification and the like.

[0012]

In the case where a transistor is formed using an oxide semiconductor, an oxygen vacancy serves as a source of carriers in the oxide semiconductor. Oxygen vacancies contained in the oxide semiconductor appear as localized states in deep energy levels in

the energy gap of the oxide semiconductor. When carriers are trapped by such localized states, the electrical characteristics of the transistor degrade; for example, the transistor becomes normally-on, or has an increased leakage current or a threshold voltage shifted by stress application. It is thus necessary to reduce the amount of oxygen vacancies in the oxide semiconductor in order to improve the reliability of the transistor.

[0013]

In an oxide semiconductor layer, hydrogen, silicon, nitrogen, carbon, and metal elements except for the main components are impurities. For example, part of hydrogen in the oxide semiconductor layer forms a donor level to increase carrier density.

[0014]

Therefore, in order that a semiconductor device including an oxide semiconductor can have stable electrical characteristics, some measures need to be taken to reduce oxygen vacancies in the oxide semiconductor layer with a sufficient supply of oxygen and to reduce the concentration of impurities such as hydrogen.

[0015]

In a semiconductor device of one embodiment of the present invention, oxygen is supplied to a channel formation region from a gate insulating layer under an oxide semiconductor layer and an insulating layer serving as a protective insulating layer over the oxide semiconductor layer, thereby filling oxygen vacancies which might be caused in the channel formation region.

[0016]

In one embodiment of the present invention, an insulating layer including an aluminum oxide film containing excess oxygen is used as the gate insulating layer and the protective insulating layer which supply oxygen to the channel formation region. Here, excess oxygen refers to, for example, oxygen in excess of the stoichiometric composition, or oxygen that can be released by heating at a temperature lower than or equal to that of heat treatment in a manufacturing process of a semiconductor device. For example, an AlO_x (x is greater than 1.5) film can be provided as an aluminum oxide film containing excess oxygen. Excess oxygen contained in the aluminum oxide film can be released by heating to be supplied to the oxide semiconductor layer. Therefore, oxygen can be effectively supplied to the channel formation region when the insulating layer including such an aluminum oxide film is provided under and over the oxide semiconductor layer.

[0017]

The aluminum oxide film containing excess oxygen can be formed by a sputtering method or the like in an atmosphere containing oxygen.

[0018]

The aluminum oxide film is an insulating layer whose oxygen and hydrogen permeability is lower than that of an insulating layer such as a silicon oxide film or a silicon oxynitride film or an oxide semiconductor layer. That is, the aluminum oxide film forms a barrier against oxygen and hydrogen. An insulating layer including the aluminum oxide film thus minimizes generation of oxygen vacancies due to removal of oxygen from a region surrounded by the insulating layer, and prevents entry of hydrogen or a hydrogen compound.

[0019]

In one embodiment of the present invention, a gate insulating layer provided on one of the top and bottom sides of an oxide semiconductor layer and a protective insulating layer provided on the other side of the oxide semiconductor layer are in contact with each other in a region where the oxide semiconductor layer, and a source electrode layer and a drain electrode layer electrically connected to the oxide semiconductor layer do not exist. In other words, in the semiconductor device of one embodiment of the present invention, the oxide semiconductor layer is surrounded by the aluminum oxide film. With such a structure, removal of oxygen and/or entry of impurities such as hydrogen can be minimized and oxygen can be supplied not only on a front channel side and a back channel side of the oxide semiconductor layer but also on a side surface of the oxide semiconductor layer. It is thus possible to reduce variation in the electrical characteristics of a transistor including a channel in the oxide semiconductor layer, offering a highly reliable semiconductor device.

[0020]

More specifically, the following structures can be employed, for example.

[0021]

One embodiment of the present invention is a semiconductor device including a first gate electrode layer; a first gate insulating layer over and in contact with the first gate electrode layer; an oxide semiconductor layer overlapping with the first gate electrode layer with the first gate insulating layer interposed therebetween; a source electrode layer

and a drain electrode layer electrically connected to the oxide semiconductor layer; a second gate insulating layer which is over the source electrode layer and the drain electrode layer and overlaps with the oxide semiconductor layer; a second gate electrode layer overlapping with the oxide semiconductor layer with the second gate insulating layer interposed therebetween; and a protective insulating layer covering the source electrode layer, the drain electrode layer, and the second gate electrode layer. The first gate insulating layer and the protective insulating layer each include an aluminum oxide film containing excess oxygen, and are in contact with each other in a region where the source electrode layer, the drain electrode layer, and the second gate electrode layer do not exist.

[0022]

Another embodiment of the present invention is a semiconductor device including a first insulating layer; a first gate electrode layer buried in the first insulating layer and having an exposed top surface; a first gate insulating layer over and in contact with the first insulating layer and the first gate electrode layer; an oxide semiconductor layer overlapping with the first gate electrode layer with the first gate insulating layer interposed therebetween; a source electrode layer and a drain electrode layer electrically connected to the oxide semiconductor layer; a second gate insulating layer which is over the source electrode layer and the drain electrode layer and overlaps with the oxide semiconductor layer; a second gate electrode layer overlapping with the oxide semiconductor layer with the second gate insulating layer interposed therebetween; and a protective insulating layer covering the source electrode layer, the drain electrode layer, and the second gate electrode layer. The first gate insulating layer and the protective insulating layer each include an aluminum oxide film containing excess oxygen, and are in contact with each other in a region where the source electrode layer, the drain electrode layer, and the second gate electrode layer do not exist.

[0023]

In a cross-section of the above semiconductor device in a channel width direction, the second gate electrode layer preferably covers a side surface and a top surface of the oxide semiconductor layer with the second gate insulating layer interposed therebetween.

[0024]

The aforementioned semiconductor device preferably further includes a first oxide layer which is between the first gate insulating layer and the oxide semiconductor

layer and includes as a constituent element at least one of metal elements contained in the oxide semiconductor layer; and a second oxide layer which is between the second gate insulating layer and the oxide semiconductor layer and includes as a constituent element at least one of metal elements contained in the oxide semiconductor layer. The energy at the bottom of the conduction band of the oxide semiconductor layer is preferably closer to the vacuum level than the energy at the bottom of the conduction band of the first and second oxide layers is by greater than or equal to 0.05 eV and less than or equal to 2 eV.

[0025]

In the above structure, the second oxide layer is preferably provided over the source electrode layer and the drain electrode layer so as to cover the oxide semiconductor layer not covered with the source electrode layer and the drain electrode layer.

[0026]

The structure of one embodiment of the present invention produces the following effects, for example.

[0027]

In the semiconductor device of one embodiment of the present invention, an oxide semiconductor layer is surrounded by insulating layers including an aluminum oxide film containing excess oxygen. Excess oxygen contained in the aluminum oxide film is supplied to the oxide semiconductor layer, in which a channel is to be formed, by heat treatment in a manufacturing process of the semiconductor device. Moreover, the aluminum oxide film forms a barrier against oxygen and hydrogen, which minimizes the removal of oxygen from the oxide semiconductor layer surrounded by the insulating layer including an aluminum oxide film and the entry of impurities such as hydrogen in the oxide semiconductor layer. The oxide semiconductor layer supplied with sufficient oxygen and blocking entry of impurities such as hydrogen is a highly purified intrinsic oxide semiconductor layer.

[0028]

In the above semiconductor device, an electric field is applied to the oxide semiconductor layer vertically from the first gate electrode layer under the oxide semiconductor layer and the second gate electrode layer over the oxide semiconductor layer; as a result, the threshold voltage of the semiconductor device can be controlled effectively. Moreover, the second gate electrode layer is provided to cover a side surface

of the oxide semiconductor layer with the second gate insulating layer interposed therebetween. Accordingly, the electric field can be applied to a channel formation region in both the vertical and horizontal directions, allowing the threshold voltage of a transistor to be controlled more effectively and the subthreshold swing (S value) to be reduced.

[0029]

In the semiconductor device of one embodiment of the present invention, the oxide layer including as a constituent element at least one of metal elements contained in the oxide semiconductor layer is preferably provided between the oxide semiconductor layer and each of the first gate insulating layer and the protective insulating layer which overlap with the oxide semiconductor layer. This suppresses the formation of trap states at the interfaces between the oxide semiconductor layer and each of the insulating layers overlapping with the oxide semiconductor layer. As a result, deterioration of the electrical characteristics of the transistor can be minimized.

[0030]

That is, one embodiment of the present invention preferably has the following structure. The top surface and bottom surface of an oxide semiconductor layer are covered with an oxide layer serving as a barrier film for preventing generation of interface states in the oxide semiconductor layer; a side surface of the oxide semiconductor layer in the channel width direction and the bottom surface thereof are covered with a gate electrode layer with a gate insulating layer interposed therebetween; and the oxide semiconductor layer is surrounded by insulating layers including an aluminum oxide film. Such a structure makes it possible to minimize the generation of oxygen vacancies producing carriers and the entry of impurities in the oxide semiconductor layer and at the interface. Thus, a highly purified intrinsic oxide semiconductor layer can be obtained. The highly purified intrinsic oxide semiconductor layer refers to an intrinsic or substantially intrinsic oxide semiconductor layer. It is thus possible to reduce variation in the electrical characteristics of a transistor including the oxide semiconductor layer and to provide a highly reliable semiconductor device.

[0031]

One embodiment of the present invention allows for providing a highly reliable semiconductor device including an oxide semiconductor.

[0032]

One embodiment of the present invention also allows for providing a semiconductor device that includes an oxide semiconductor and is miniaturized while keeping good electrical properties.

BRIEF DESCRIPTION OF DRAWINGS

[0033]

In the accompanying drawings:

FIGS. 1A to 1C are a plan view and cross-sectional views illustrating one embodiment of a semiconductor device;

FIGS. 2A to 2C are a plan view and cross-sectional views illustrating one embodiment of a semiconductor device;

FIGS. 3A to 3C are cross-sectional views illustrating a method for manufacturing the semiconductor device;

FIGS. 4A to 4C are cross-sectional views illustrating the method for manufacturing the semiconductor device;

FIGS. 5A to 5C are a plan view and cross-sectional views illustrating one embodiment of a semiconductor device, and FIG. 5D is a band diagram;

FIGS. 6A to 6C are a plan view and cross-sectional views illustrating one embodiment of a semiconductor device;

FIG. 7 is a circuit diagram illustrating an example of a semiconductor device;

FIG. 8 is a block diagram illustrating an example of a semiconductor device;

FIG. 9 is a circuit diagram illustrating an example of a semiconductor device;

FIG. 10 is a circuit diagram illustrating an example of a semiconductor device;

FIGS. 11A to 11C illustrate examples of a semiconductor device; and

FIGS. 12A to 12C illustrate embodiments of electronic devices.

BEST MODE FOR CARRYING OUT THE INVENTION

[0034]

Hereinafter, embodiments of the disclosed invention will be described in detail with reference to the accompanying drawings. Note that the invention disclosed in this specification is not limited to the following description, and it is easily understood by

those skilled in the art that modes and details of the invention can be modified in various ways. Therefore, the invention disclosed in this specification is not construed as being limited to the description of the following embodiments. Note that in the structures of one embodiment of the present invention described under, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and description thereof is not repeated. Furthermore, the same hatching pattern is applied to portions having similar functions, and the portions are not especially denoted by reference numerals in some cases.

[0035]

In this specification and the like, ordinal numbers such as "first" and "second" are used in order to avoid confusion among components and do not limit the number.

[0036]

In this specification and the like, a substantially intrinsic oxide semiconductor layer has a carrier density lower than 1×10^{17} /cm^3, lower than 1×10^{15} /cm^3, or lower than 1×10^{13} /cm^3. With a highly purified intrinsic oxide semiconductor layer, a transistor can have stable electrical characteristics.

[0037]

In this specification and the like, the terms "over" and "under" do not necessarily mean "directly on" and "directly under", respectively, in the description of a positional relationship between components. For example, the expression "a gate electrode over a gate insulating layer" does not exclude the case where a component is placed between the gate insulating layer and the gate electrode. The same applies to the term "under".

[0038]

In this specification and the like, a top surface of a film refers to one of the surfaces substantially parallel to a substrate surface that is farther from the substrate surface; and a bottom surface of the film refers to the other of the surfaces substantially parallel to the substrate surface that is closer to the substrate surface.

[0039]

In this specification, the term "parallel" indicates that the angle formed between two straight lines is greater than or equal to −10° and less than or equal to 10°, and accordingly also includes the case where the angle is greater than or equal to −5° and less than or equal to 5°. In addition, the term "perpendicular" indicates that the angle formed

between two straight lines is greater than or equal to 80° and less than or equal to 100°, and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95°.

[0040]

In this specification, trigonal and rhombohedral crystal systems are included in a hexagonal crystal system.

[0041]

[Embodiment 1]

In this embodiment, one embodiment of a semiconductor device and a method for manufacturing the semiconductor device will be described with reference to FIGS. 1A to 1C, FIGS. 2A to 2C, FIGS. 3A to 3C, and FIGS. 4A to 4C. In this embodiment, a transistor including an oxide semiconductor is shown as an example of the semiconductor device.

[0042]

FIGS. 1A to 1C illustrate an example of a structure of a transistor 250. FIG. 1A is a plan view of the transistor 250, FIG. 1B is a cross-sectional view taken along line V1-W1 in FIG. 1A, and FIG. 1C is a cross-sectional view taken along line X1-Y1 in FIG. 1A. Note that in FIG. 1A, some components of the transistor 250 (e.g., an insulating layer 212) are not illustrated to avoid complexity. The same applies to the other plan views in this specification.

[0043]

The transistor 250 illustrated in FIGS. 1A to 1C includes a first gate electrode layer 202 over a substrate 200; an insulating layer 206 in contact with the first gate electrode layer 202; an oxide semiconductor layer 208 overlapping with the first gate electrode layer 202 with the insulating layer 206 interposed therebetween; a source electrode layer 210a and a drain electrode layer 210b electrically connected to the oxide semiconductor layer 208; an insulating layer 214 which is over the source electrode layer 210a and the drain electrode layer 210b and overlaps with the oxide semiconductor layer 208; a second gate electrode layer 216 overlapping with the oxide semiconductor layer 208 with the insulating layer 214 interposed therebetween; and an insulating layer 212 provided over the insulating layer 206 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216.

[0044]

In the transistor 250, the insulating layer 206 between the first gate electrode layer 202 and the oxide semiconductor layer 208 functions as a first gate insulating layer; the insulating layer 214 between the second gate electrode layer 216 and the oxide semiconductor layer 208 functions as a second gate insulating layer; and the insulating layer 212 provided over the oxide semiconductor layer 208 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216 functions as a protective insulating layer.

[0045]

In the transistor 250, an insulating layer including an aluminum oxide film containing excess oxygen is used as the insulating layer 206 under the oxide semiconductor layer 208 and the insulating layer 212 over the oxide semiconductor layer 208.

[0046]

As illustrated in the cross-sectional views of FIGS. 1B and 1C, in both a channel length direction (the direction in which carriers flow) and a channel width direction, the insulating layer 206 functioning as the first gate insulating layer and the insulating layer 212 functioning as the protective insulating layer are in contact with each other in a region where the oxide semiconductor layer 208, the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216 do not exist. In other words, the oxide semiconductor layer 208 in the transistor 250 is surrounded by the insulating layers including an aluminum oxide film.

[0047]

As mentioned above, excess oxygen contained in the aluminum oxide film is released by heat treatment in a manufacturing process of the transistor 250 to be supplied to the oxide semiconductor layer 208. Heat treatment for forming an insulating layer and the like over the oxide semiconductor layer 208 can also serve as this heat treatment. The aluminum oxide film forms a barrier against oxygen and hydrogen. Accordingly, the amount of oxygen vacancies is reduced in the oxide semiconductor layer 208 because removal of oxygen is minimized and a sufficient amount of oxygen is supplied thereto, and furthermore, entry of impurities such as hydrogen is reduced in the oxide semiconductor layer 208. That is, the oxide semiconductor layer 208 is a highly purified

intrinsic oxide semiconductor layer. The transistor 250 including the highly purified and i-type (intrinsic) oxide semiconductor layer 208 has little variation in electrical characteristics and is electrically stable.

[0048]

In order to make the oxide semiconductor layer 208 intrinsic or substantially intrinsic, the concentration of hydrogen, which is measured by secondary ion mass spectrometry (SIMS), is set to be lower than or equal to 2×10^{20} atoms/cm^3, preferably lower than or equal to 5×10^{19} atoms/cm^3, more preferably lower than or equal to 1×10^{19} atoms/cm^3, and still more preferably lower than or equal to 5×10^{18} atoms/cm^3.

[0049]

The concentration of hydrogen is preferably reduced in the insulating layer 206 under the oxide semiconductor layer 208 and the insulating layer 212 over the oxide semiconductor layer 208. Specifically, the concentration of hydrogen in the insulating layers 206 and 212 is preferably lower than 5×10^{19} atoms/cm^3, more preferably lower than 5×10^{18} atoms/cm^3.

[0050]

The transistor 250 in which the highly purified oxide semiconductor layer 208 is used for a channel formation region has an extremely low off-state current. For example, the drain current when the transistor including a highly purified oxide semiconductor layer is in an off state can be lower than or equal to 1×10^{-18} A, preferably lower than or equal to 1×10^{-21} A, and more preferably lower than or equal to 1×10^{-24} A at room temperature (approximately 25 °C), or the drain current can be lower than or equal to 1×10^{-15} A, preferably lower than or equal to 1×10^{-18} A, and more preferably lower than or equal to 1×10^{-21} A at 85 °C. Note that the off state of an n-channel transistor refers to a state where the gate voltage is sufficiently lower than the threshold voltage. Specifically, the transistor is in the off state when the gate voltage is lower than the threshold voltage by 1 V or more, 2 V or more, or 3 V or more.

[0051]

Miniaturization of a transistor leads to an increase in density (higher integration). For example, the channel length of the transistor is made less than or equal to 100 nm, preferably less than or equal to 40 nm, and more preferably less than or equal to 30 nm.

[0052]

An increase in the density (higher integration) of a semiconductor device certainly needs miniaturization of a transistor. However, it is known that a miniaturized transistor has degraded electrical characteristics. For example, short-channel effects are known to occur due to a shortened channel length of a transistor including silicon, in which case the subthreshold swing (S value) increases, or the threshold voltage shifts in the negative direction.

[0053]

However, a transistor including an oxide semiconductor is an accumulation-type transistor whose majority carriers are electrons; therefore, drain-induced barrier lowering (DIBL) as a short-channel effect is less likely to occur than in an inversion-type transistor such as a silicon transistor. In other words, the transistor including an oxide semiconductor is unlikely to suffer the short-channel effects, and is suitable for miniaturization.

[0054]

An electric field is applied to the oxide semiconductor layer 208 vertically from the first gate electrode layer 202 under the oxide semiconductor layer 208 and the second gate electrode layer 216 over the oxide semiconductor layer 208. With such a structure, the electric field is applied to a channel formation region in both the vertical and horizontal directions, allowing the threshold voltage of the transistor 250 to be controlled effectively. Moreover, the S value of the transistor 250 can be reduced. The first gate electrode layer 202 and the second gate electrode layer 216 may have, but are not limited to, the same potential.

[0055]

When the channel width of the transistor 250 is too large, it is difficult for the electric field of the second gate electrode layer 216 to be applied from the direction of a side surface of the channel formation region, causing difficulty in controlling threshold voltage. In order that the electric field can be sufficiently applied from the second gate electrode layer 216 in the direction of the side surface of the oxide semiconductor layer 208, the film thickness of the oxide semiconductor layer 208 is preferably larger than or equal to the channel width.

[0056]

In general, a reduced channel width of a transistor might cause a decrease in

on-state current. The thickness of an active layer can be increased by a known method so that a channel is formed on side surfaces of the active layer to increase the on-state current. In that case, the surface area of a region including the channel increases to cause more carrier scattering at the interface between the channel formation region and a gate insulating layer; therefore, a sufficient increase in on-state current cannot be expected.

[0057]

However, in the transistor 250 of this embodiment, the oxide semiconductor layer 208 including the channel is surrounded by the insulating layers 206 and 212 including an aluminum oxide film containing excess oxygen. Thus, excess oxygen contained in the aluminum oxide film can be supplied to the oxide semiconductor layer 208 and removal of oxygen from the oxide semiconductor layer 208 and entry of impurities such as hydrogen in the oxide semiconductor layer 208 can be minimized. Since oxygen vacancies and hydrogen produce carriers in the oxide semiconductor layer 208, the aluminum oxide film containing excess oxygen reduces carrier scattering which might occur at the interface of the oxide semiconductor layer 208 including the channel.

[0058]

Thus, even with a reduced channel width, the on-state current can be sufficiently increased by increasing the thickness of the oxide semiconductor layer 208 to increase the surface area overlapping with the second gate electrode layer 216.

[0059]

Note that part of hydrogen in the oxide semiconductor layer is trapped in oxygen vacancies. As a result, the oxide semiconductor layer has n-type conductivity and the Fermi level (Ef) thereof is closer to the bottom of the conduction band (Ec). The oxide semiconductor layer including a large amount of hydrogen therefore contributes to an improvement in the field-effect mobility of the transistor though the electrical characteristics thereof might vary. On the contrary, the Fermi energy of the intrinsic or substantially intrinsic oxide semiconductor layer 208 is equal to or close to the mid gap (the middle of the energy gap of the oxide semiconductor layer). In that case, the number of carriers decreases in the oxide semiconductor layer 208, leading to a reduced field-effect mobility.

[0060]

In the transistor 250, however, a gate electric field is applied to the oxide

semiconductor layer 208 in both the vertical and horizontal directions. That is, the gate electric field is applied to the whole of the oxide semiconductor layer 208, whereby current flows in the bulk of the oxide semiconductor layer 208. It is thus possible to improve the field-effect mobility of the transistor 250 while variation in the electrical characteristics is minimized by highly purified intrinsic properties.

[0061]

When the channel length and channel width of a transistor are minimized, a wiring, a semiconductor layer, and the like processed using a resist mask have round edges (curved edges) in some cases. In the case where a thin insulating layer (e.g., a gate insulating layer) is formed to cover an oxide semiconductor layer with a large thickness, poor coverage sometimes causes a defective shape and difficulty in obtaining stable electrical characteristics. It is thus preferable that the oxide semiconductor layer 208 have a round edge so as to improve the coverage of the oxide semiconductor layer 208 with the insulating layer 214.

[0062]

FIGS. 2A to 2C illustrate an example of a structure of a transistor 260 as another example of the transistor of this embodiment. FIG. 2A is a plan view of the transistor 260, FIG. 2B is a cross-sectional view taken along line V2-W2 in FIG. 2A, and FIG. 2C is a cross-sectional view taken along line X2-Y2 in FIG. 2A.

[0063]

The transistor 260 illustrated in FIGS. 2A to 2C includes an insulating layer 205 over the substrate 200; the first gate electrode layer 202 which is buried in the insulating layer 205 and has an exposed top surface; the insulating layer 206 provided over the insulating layer 205 so as to be in contact with the exposed top surface of the first gate electrode layer 202 that is not covered with the insulating layer 205; the oxide semiconductor layer 208 overlapping with the first gate electrode layer 202 with the insulating layers 205 and 206 interposed therebetween; the source electrode layer 210a and the drain electrode layer 210b electrically connected to the oxide semiconductor layer 208; the insulating layer 214 which is over the source electrode layer 210a and the drain electrode layer 210b and overlaps with the oxide semiconductor layer 208; the second gate electrode layer 216 overlapping with the oxide semiconductor layer 208 with the insulating layer 214 interposed therebetween; and the insulating layer 212 provided over

the insulating layer 206 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216.

[0064]

In the transistor 260, the insulating layer 206 between the first gate electrode layer 202 and the oxide semiconductor layer 208 functions as a first gate insulating layer; the insulating layer 214 between the second gate electrode layer 216 and the oxide semiconductor layer 208 functions as a second gate insulating layer; and the insulating layer 212 provided over the oxide semiconductor layer 208 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216 functions as a protective insulating layer.

[0065]

The transistor 260 illustrated in FIGS. 2A to 2C is different from the transistor 250 in FIGS. 1A to 1C in the structure of the first gate electrode layer 202. In the transistor 250, the insulating layer 206 is formed to cover the first gate electrode layer 202 over the substrate. On the contrary, in the transistor 260, the first gate electrode layer 202 is buried in the insulating layer 205 and has an exposed top surface, and the exposed top surface is in contact with the insulating layer 206 functioning as the first gate insulating layer.

[0066]

The other components of the transistor 260 can be similar to those of the transistor 250.

[0067]

An example of a method for manufacturing the transistor 260 will be described with reference to FIGS. 3A to 3C and FIGS. 4A to 4C.

[0068]

The first gate electrode layer 202 (including wirings formed with the same layer) is formed over the substrate 200 having an insulating surface, and an insulating film 205a is formed over the first gate electrode layer 202 (see FIG. 3A).

[0069]

There is no particular limitation on the substrate that can be used as the substrate 200 having an insulating surface as long as it has heat resistance enough to withstand heat treatment performed later. For example, a glass substrate of barium borosilicate glass,

aluminoborosilicate glass, or the like, a ceramic substrate, a quartz substrate, or a sapphire substrate can be used. A single crystal semiconductor substrate or a polycrystalline semiconductor substrate of silicon, silicon carbide, or the like; a compound semiconductor substrate of silicon germanium or the like; an SOI substrate; or the like can be used as the substrate 200, or the substrate provided with a semiconductor element can be used as the substrate 200.

[0070]

The semiconductor device may be manufactured using a flexible substrate as the substrate 200. To manufacture a flexible semiconductor device, the transistor 260 may be directly formed over a flexible substrate; or alternatively, the transistor 260 may be formed over a substrate and then separated from the substrate and transferred to a flexible substrate. Note that in order to separate the transistor 260 from the manufacturing substrate and transfer it to the flexible substrate, a separation layer may be provided between the manufacturing substrate and the transistor 260.

[0071]

The first gate electrode layer 202 can be made using a metal film containing an element selected from molybdenum, titanium, tantalum, tungsten, aluminum, copper, chromium, neodymium, and scandium; a metal nitride film containing any of the above elements as its component (a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film); or the like. Alternatively, a semiconductor film typified by a polycrystalline silicon film doped with an impurity element such as phosphorus, or a silicide film such as a nickel silicide film may be used as the first gate electrode layer 202. The first gate electrode layer 202 can also be made of a conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible that the first gate electrode layer 202 have a stacked structure of the above conductive material and the above metal material.

[0072]

The first gate electrode layer 202 can have a single-layer structure or a layered structure. As one layer of the first gate electrode layer 202 that is in contact with the insulating film 205a, a metal oxide film containing nitrogen, specifically, an In-Ga-Zn-O

film containing nitrogen, an In-Sn-O film containing nitrogen, an In-Ga-O film containing nitrogen, an In-Zn-O film containing nitrogen, a Sn-O film containing nitrogen, an In-O film containing nitrogen, or a metal nitride (e.g., InN or SnN) film can be used. Such a film has a work function of 5 eV (electron volt) or higher, preferably 5.5 eV (electron volt) or higher, and the use of this film as the gate electrode layer enables the threshold voltage of the transistor to shift in the positive direction. Accordingly, a so-called normally-off switching element can be obtained.

[0073]

The first gate electrode layer 202 can be formed by a plasma CVD method, a sputtering method, or the like.

[0074]

The insulating film 205a can have a single-layer structure or a layered structure using a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or the like. Note that the thickness of the insulating film 205a is preferably larger than or equal to at least the thickness of the first gate electrode layer 202.

[0075]

Then, the insulating film 205a is subjected to etch-back treatment or chemical mechanical polishing (CMP) treatment so that part of the first gate electrode layer 202 is exposed. Note that the CMP treatment and the etch-back treatment may be performed in combination. The etch-back treatment or the CMP treatment removes the insulating film 205a over the first gate electrode layer 202, thereby forming the insulating layer 205 in which the first gate electrode layer 202 is buried.

[0076]

Next, the insulating layer 206 is formed over and in contact with the insulating layer 205 (see FIG. 3B).

[0077]

The insulating layer 206 includes at least an aluminum oxide film containing excess oxygen. The insulating layer 206 may have a layered structure of an aluminum oxide film and any of a silicon oxide film, a gallium oxide film, an aluminum oxide film, a silicon nitride film, a silicon oxynitride film, an aluminum oxynitride film, and a silicon nitride oxide film. In the case of the layered structure, insulating films other than the aluminum oxide film may also contain excess oxygen.

[0078]

For example, the insulating layer 206 may have a layered structure in which an aluminum oxide film containing excess oxygen and a silicon oxide film containing excess oxygen are stacked in this order from the side closer to the first gate electrode layer 202. In that case, the aluminum oxide film opposite the oxide semiconductor layer with the silicon oxide film therebetween suppresses outward diffusion of excess oxygen contained in the silicon oxide film, and also allows oxygen to be effectively supplied to the oxide semiconductor layer 208 formed later.

[0079]

The aluminum oxide film included in the insulating layer 206 is preferably formed by a sputtering method using an aluminum oxide target. Alternatively, the aluminum oxide film may be formed by reactive sputtering using an aluminum target. When an aluminum oxide film is formed in an atmosphere containing oxygen, the formed aluminum oxide film can contain excess oxygen. The proportion of oxygen in the deposition gas is preferably higher than or equal to 30 vol%. A rare gas (e.g., argon) may be contained in addition to oxygen.

[0080]

Alternatively, as the aluminum oxide film included in the insulating layer 206, an aluminum oxide film containing silicon oxide may be formed using an aluminum oxide target containing silicon oxide at a proportion of 0.1% to 30%. Because the oxygen permeability of silicon oxide is higher than that of aluminum oxide, excess oxygen contained in the aluminum oxide film including silicon oxide is easily released. In addition, the use of the aluminum oxide film including silicon oxide for a transistor produces an effect of stress relief. On the contrary, a high proportion of silicon oxide reduces barrier properties against oxygen; therefore, the aluminum oxide target preferably contains silicon oxide at a proportion of 30% or lower, for example, at a proportion of 5% or 10%.

[0081]

The insulating layer 206 is preferably formed at a high substrate temperature, in which case the hydrogen concentration in the insulating layer 206 can be reduced. The substrate temperature is, for example, higher than or equal to 100 °C and lower than or equal to 500 °C, preferably higher than or equal to 150 °C and lower than or equal to 450

°C.

[0082]

Next, an oxide semiconductor film is formed over the insulating layer 206 and processed into an island shape to form the oxide semiconductor layer 208 (see FIG. 3C).

[0083]

The oxide semiconductor film may have either a single-layer structure or a layered structure. Furthermore, the oxide semiconductor film may have either an amorphous structure or a crystalline structure.

[0084]

The oxide semiconductor film can be formed by a sputtering method, a molecular beam epitaxy (MBE) method, a CVD method, a pulse laser deposition method, an atomic layer deposition (ALD) method, or the like as appropriate.

[0085]

In the formation of the oxide semiconductor film, the concentration of hydrogen contained in the oxide semiconductor is preferably reduced as much as possible. In order to reduce the hydrogen concentration, for example, in the case where a sputtering method is used for the deposition, a high-purity rare gas (typically, argon) from which impurities such as hydrogen, water, a hydroxyl group, or a hydride have been removed; oxygen; or a mixed gas of oxygen and the rare gas is used as appropriate as an atmosphere gas supplied to a deposition chamber of a sputtering apparatus.

[0086]

The oxide semiconductor film is formed in such a manner that a sputtering gas from which hydrogen and moisture are removed is introduced into a deposition chamber while moisture remaining in the deposition chamber is removed, whereby the hydrogen concentration in the deposited oxide semiconductor film can be reduced. In order to remove the residual moisture in the deposition chamber, an entrapment vacuum pump, for example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. The evacuation unit may be a turbo molecular pump provided with a cold trap. A cryopump has a high capability in removing a hydrogen molecule, a compound containing a hydrogen atom such as water (H_2O) (preferably, also a compound containing a carbon atom), and the like, allowing a reduction in the impurity concentration in the oxide semiconductor film formed in the deposition chamber which is evacuated with the

cryopump.

[0087]

In the case where the oxide semiconductor film is formed by a sputtering method, the relative density (the fill rate) of a metal oxide target used for the deposition is greater than or equal to 90% and less than or equal to 100%, preferably greater than or equal to 95% and less than or equal to 99.9%. With the use of the metal oxide target having high relative density, a dense oxide semiconductor film can be formed.

[0088]

The formation of the oxide semiconductor film while the substrate 200 is kept at high temperature is also effective in reducing the impurity concentration in the oxide semiconductor film. The heating temperature of the substrate 200 may be higher than or equal to 150 °C and lower than or equal to 450 °C; the substrate temperature is preferably higher than or equal to 200 °C and lower than or equal to 350 °C. When the substrate is heated at a high temperature in deposition, the oxide semiconductor film having crystallinity can be formed.

[0089]

An oxide semiconductor used for the oxide semiconductor film contains at least indium (In). In particular, indium and zinc (Zn) are preferably contained. The oxide semiconductor preferably contains, in addition to In and/or Zn, gallium (Ga) serving as a stabilizer that reduces variation in the electrical characteristics of transistors using the above-described oxide semiconductor. It is preferable that one or more elements selected from tin (Sn), hafnium (Hf), aluminum (Al), and zirconium (Zr) be contained as a stabilizer.

[0090]

As another stabilizer, one or plural kinds of lanthanoid such as lanthanum (La), cerium (Ce), praseodymium (Pr), neodymium (Nd), samarium (Sm), europium (Eu), gadolinium (Gd), terbium (Tb), dysprosium (Dy), holmium (Ho), erbium (Er), thulium (Tm), ytterbium (Yb), or lutetium (Lu) may be contained.

[0091]

Examples of the oxide semiconductor include the following: indium oxide; tin oxide; zinc oxide; a two-component metal oxide such as an In-Zn-based oxide, an In-Mg-based oxide, or an In-Ga-based oxide; a three-component metal oxide such as an

In-Ga-Zn-based oxide (also referred to as IGZO), an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, an In-Hf-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, or an In-Lu-Zn-based oxide; and a four-component metal oxide such as an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, or an In-Hf-Al-Zn-based oxide.

[0092]

For example, an In-Ga-Zn-based oxide refers to an oxide containing In, Ga, and Zn as its main components, and there is no limitation on the composition ratio of In, Ga, and Zn. The In-Ga-Zn-based oxide may contain a metal element other than In, Ga, and Zn.

[0093]

Note that, a transistor including an oxide semiconductor containing indium is not limited to that described above, and a material with an appropriate composition may be used depending on required electrical characteristics (e.g., field-effect mobility and threshold voltage) of the transistor. In order to obtain required electrical characteristics, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like be set to be appropriate.

[0094]

Heat treatment is preferably performed after the formation of the oxide semiconductor film. The heat treatment may be performed at a temperature of 250 °C to 650 °C, preferably 300 °C to 500 °C, in an inert gas atmosphere, an atmosphere containing an oxidizing gas at 10 ppm or more, or a reduced pressure atmosphere. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more in order to compensate released oxygen. The heat treatment here allows impurities such as hydrogen and water to be removed from the oxide semiconductor film. The heat treatment may be performed after the oxide

semiconductor film is processed into the island-like oxide semiconductor layer 208.

[0095]

Then, a conductive film is formed over the insulating layer 206 and the island-like oxide semiconductor layer 208 and processed to form the source electrode layer 210a and the drain electrode layer 210b (including wirings formed with the same layer) (see FIG. 4A).

[0096]

The source electrode layer 210a and the drain electrode layer 210b can be formed using the same material as that of the first gate electrode layer 202, and can have a single-layer structure or a layered structure.

[0097]

Although not illustrated, the source electrode layer 210a and the drain electrode layer 210b may have a step-like end with a plurality of steps. The end can be processed by alternately performing the step of making a resist mask recede by ashing and the etching step plural times. It is preferable that the number of steps be increased as the source electrode layer 210a and the drain electrode layer 210b have a larger thickness. When the source electrode layer 210a and the drain electrode layer 210b have the aforementioned shape including a plurality of steps, coverage with the insulating layer 212 formed over the source electrode layer 210a and the drain electrode layer 210b is improved, so that the transistor can have more favorable electrical characteristics and higher long-term reliability.

[0098]

When the conductive film is processed into the source electrode layer 210a and the drain electrode layer 210b, part of the oxide semiconductor layer 208 (regions that are not covered with the source electrode layer 210a and the drain electrode layer 210b) might be etched to be thinned by overetching of the conductive film.

[0099]

Next, an insulating film 214a is formed over the insulating layer 206 so as to cover the source electrode layer 210a and the drain electrode layer 210b (see FIG. 4B).

[0100]

The insulating film 214a can be formed using a material and a method similar to those of the insulating film 205a.

[0101]

Then, a conductive film is formed over the insulating film 214a and processed to form the second gate electrode layer 216 (including wirings formed with the same layer). After that, the insulating film 214a is processed using the second gate electrode layer 216 as a mask, whereby the insulating layer 214 is formed. The insulating layer 214 is preferably processed in a self-aligned manner using the second gate electrode layer 216 as a mask because there is no increase in the number of masks.

[0102]

Next, the insulating layer 212 is formed over the insulating layer 206 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216 (see FIG. 4C). The insulating layer 212 includes at least an aluminum oxide film containing excess oxygen, and can be formed using a structure and a manufacturing method similar to those of the insulating layer 206.

[0103]

Heat treatment may be performed after the formation of the insulating layer 212. The conditions of the heat treatment may be similar to those of the above heat treatment after the formation of the oxide semiconductor film.

[0104]

Through the above steps, the transistor 260 of this embodiment can be obtained.

[0105]

In the semiconductor device of this embodiment, the oxide semiconductor layer is surrounded by the insulating layers including an aluminum oxide film containing excess oxygen. This allows oxygen to be supplied to the oxide semiconductor layer and minimizes the removal of oxygen from the oxide semiconductor layer and the entry of impurities such as hydrogen in the oxide semiconductor layer.

[0106]

It is thus possible to reduce variation in electrical characteristics such as threshold voltage, which might occur due to oxygen vacancies in the channel formation region. Specifically, stable normally-off state is achieved for example. Thus, a semiconductor device which has favorable electrical characteristics and high long-term reliability can be provided.

[0107]

In the semiconductor device of this embodiment, an electric field is applied to the oxide semiconductor layer vertically from the first gate electrode layer under the oxide semiconductor layer and the second gate electrode layer over the oxide semiconductor layer, allowing the threshold voltage of the transistor to be controlled effectively.

[0108]

Moreover, the second gate electrode layer, which overlaps with the oxide semiconductor layer with the second gate insulating layer interposed therebetween, is provided to overlap with the side surface and bottom surface of the channel formation region in the channel width direction, whereby the gate electrode layer is formed to overlap with the side surface and bottom surface of the oxide semiconductor layer. As a result, the electric field is applied to the channel formation region from the side surface and the bottom surface, allowing the threshold voltage of the transistor to be controlled more effectively and the S value to be reduced.

[0109]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0110]

[Embodiment 2]

In this embodiment, a structure of the semiconductor device different from that in Embodiment 1 will be described with reference to FIGS. 5A to 5D and FIGS. 6A to 6C. For the components similar to those in Embodiment 1, the description of Embodiment 1 can be referred to and is not repeated in some cases.

[0111]

FIGS. 5A to 5D illustrate an example of a structure of a transistor 270. FIG. 5A is a plan view of the transistor 270, FIG. 5B is a cross-sectional view taken along line V3-W3 in FIG. 5A, and FIG. 5C is a cross-sectional view taken along line X3-Y3 in FIG. 5A. FIG. 5D is a band diagram schematically showing the energy at the bottom of the conduction band of a layered structure included in the transistor 270.

[0112]

The transistor 270 illustrated in FIGS. 5A to 5C includes, like the transistor 260 in Embodiment 1, the insulating layer 205 over the substrate 200; the first gate electrode layer 202 which is buried in the insulating layer 205 and has an exposed top surface; the

insulating layer 206 provided over the insulating layer 205 so as to be in contact with the top surface of the first gate electrode layer 202; the oxide semiconductor layer 208 overlapping with the first gate electrode layer 202 with the insulating layer 206 interposed therebetween; the source electrode layer 210a and the drain electrode layer 210b electrically connected to the oxide semiconductor layer 208; the insulating layer 214 which is over the source electrode layer 210a and the drain electrode layer 210b and overlaps with the oxide semiconductor layer 208; the second gate electrode layer 216 overlapping with the oxide semiconductor layer 208 with the insulating layer 214 interposed therebetween; and the insulating layer 212 provided over the insulating layer 206 so as to cover the source electrode layer 210a, the drain electrode layer 210b, and the second gate electrode layer 216.

[0113]

The transistor 270 in this embodiment includes, in addition to the structure of the aforementioned transistor 260, a first oxide layer 207 which is between the insulating layer 206 and the oxide semiconductor layer 208 and includes as a constituent element at least one of metal elements contained in the oxide semiconductor layer 208, and a second oxide layer 209 which is between the insulating layer 214 and the oxide semiconductor layer 208 and includes as a constituent element at least one of metal elements contained in the oxide semiconductor layer 208.

[0114]

In the transistor 270, a layered structure of the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209 can be formed in the following manner. The insulating layer 206 is formed over and in contact with the insulating layer 205 through the manufacturing steps of the transistor 260 shown in Embodiment 1, and then, a first oxide film to be the first oxide layer 207, an oxide semiconductor film, and a second oxide film to be the second oxide layer 209 are formed in succession. After that, a resist mask is formed by a photolithography process, and the second oxide film, the oxide semiconductor film, and the first oxide film are processed into island shapes by etching using the resist mask.

[0115]

As mentioned above, the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209 in the transistor 270 are processed using the same resist

mask. Accordingly, the top edge of the first oxide layer 207 is substantially aligned with the bottom edge of the oxide semiconductor layer 208, and the top edge of the oxide semiconductor layer 208 is substantially aligned with the bottom edge of the second oxide layer 209. In other words, the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209 have substantially the same top surface shape.

[0116]

In the above process, the first oxide film, the oxide semiconductor film, and the second oxide film are preferably formed in succession without exposure to the air, in which case impurities such as hydrogen or moisture can be prevented from being adsorbed on the interface of each layer.

[0117]

The oxide semiconductor layer 208 in the transistor 270 includes a layer represented by an In-*M*-Zn oxide, which contains at least indium, zinc, and *M* (*M* is a metal element such as Al, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf). The oxide semiconductor layer 208 preferably contains indium, because the carrier mobility of the transistor increases.

[0118]

The first oxide layer 207 under the oxide semiconductor layer 208 includes an oxide layer which is represented by an In-*M*-Zn oxide (*M* is a metal element such as Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf) and which has a higher proportion of *M* in atomic ratio than the oxide semiconductor layer 208 has. Specifically, the amount of the element *M* in the first oxide layer 207 in atomic ratio is 1.5 times or more, preferably twice or more, and more preferably three times or more as much as that in the oxide semiconductor layer 208. The element *M* is more strongly bonded to oxygen than indium is, and thus have a function of suppressing generation of oxygen vacancies in the oxide layer. That is, oxygen vacancies are less likely to be generated in the first oxide layer 207 than in the oxide semiconductor layer 208.

[0119]

Like the first oxide layer 207, the second oxide layer 209 over the oxide semiconductor layer 208 includes an oxide layer which is represented by an In-*M*-Zn oxide (*M* is a metal element such as Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf) and which has a higher proportion of *M* in atomic ratio than the oxide semiconductor layer 208 has.

Specifically, the amount of the element *M* in the second oxide layer 209 in atomic ratio is 1.5 times or more, preferably twice or more, and more preferably three times or more as much as that in the oxide semiconductor layer 208.

[0120]

In other words, when each of the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209 is an In-*M*-Zn oxide containing at least indium, zinc, and *M* (*M* is a metal element such as Al, Ti, Ga, Ge, Y, Zr, Sn, La, Ce, or Hf), and the first oxide layer 207 has an atomic ratio of In to *M* and Zn which is $x_1:y_1:z_1$, the oxide semiconductor layer 208 has an atomic ratio of In to *M* and Zn which is $x_2:y_2:z_2$, and the second oxide layer 209 has an atomic ratio of In to *M* and Zn which is $x_3:y_3:z_3$, y_1/x_1 and y_3/x_3 are each preferably larger than y_2/x_2. Each of y_1/x_1 and y_3/x_3 is 1.5 times or more as large as y_2/x_2, preferably 2 times or more, and more preferably 3 times or more as large as y_2/x_2. At this time, when y_2 is greater than or equal to x_2 in the oxide semiconductor layer 208, a transistor can have stable electrical characteristics. However, when y_2 is 3 times or more as large as x_2, the field-effect mobility of the transistor is reduced; accordingly, y_2 is preferably smaller than 3 times x_2.

[0121]

In the case of using an In-*M*-Zn oxide for the first oxide layer 207, when Zn and O are not taken into consideration, the proportion of In and the proportion of *M* are preferably less than 50 atomic% and greater than or equal to 50 atomic%, respectively, more preferably less than 25 atomic% and greater than or equal to 75 atomic%, respectively. In the case of using an In-*M*-Zn oxide for the oxide semiconductor layer 208, when Zn and O are not taken into consideration, the proportion of In and the proportion of *M* are preferably greater than or equal to 25 atomic% and less than 75 atomic%, respectively, more preferably greater than or equal to 34 atomic% and less than 66 atomic%, respectively. In the case of using an In-*M*-Zn oxide for the second oxide layer 209, when Zn and O are not taken into consideration, the proportion of In and the proportion of *M* are preferably less than 50 atomic% and greater than or equal to 50 atomic%, respectively, more preferably less than 25 atomic% and greater than or equal to 75 atomic%, respectively.

[0122]

The first oxide layer 207 and the second oxide layer 209 may include different

constituent elements, or include the same constituent elements at the same atomic ratios or different atomic ratios.

[0123]

For example, an oxide semiconductor containing indium, zinc, and gallium can be used for the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209.

[0124]

It is preferable that each of the first oxide layer 207 and the second oxide layer 209 contain one or more kinds of metal elements contained in the oxide semiconductor layer 208, and include an oxide semiconductor whose energy at the bottom of the conduction band is closer to the vacuum level than the energy at the bottom of the conduction band of the oxide semiconductor layer 208 is by 0.05 eV or more, 0.07 eV or more, 0.1 eV or more, or 0.15 eV or more and 2 eV or less, 1 eV or less, 0.5 eV or less, or 0.4 eV or less.

[0125]

When an electric field is applied to the first gate electrode layer 202 and/or the second gate electrode layer 216 in such a structure, a channel is formed in the oxide semiconductor layer 208, because the oxide semiconductor layer 208 has the lowest energy at the bottom of the conduction band in the layered structure of the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209, which is interposed between the insulating layer 206 functioning as part of a first gate insulating layer and the insulating layer 214 functioning as a second gate electrode layer. In other words, the first oxide layer 207 and the second oxide layer 209 prevent the channel of the transistor from being in contact with the insulating layer 206 and the insulating layer 214 which include constituent elements (except oxygen) different from those of the oxide semiconductor layer 208.

[0126]

FIG. 5D schematically shows a band structure of the layered structure including the insulating layer 206, the first oxide layer 207, the oxide semiconductor layer 208, the second oxide layer 209, and the insulating layer 214. In FIG. 5D, Evac denotes the energy of the vacuum level, and Ec denotes the energy at the bottom of the conduction band.

[0127]

FIG. 5D shows that the oxide semiconductor layer interposed between the oxide layers forms a well and a channel is formed in the oxide semiconductor layer in the transistor having the layered structure. The energy at the bottom of the conduction band is changed continuously in the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209; therefore, a U-shaped or round well can be considered to be formed. The channel with such a structure can also be referred to as a buried channel.

[0128]

As shown in FIG. 5D, the energy at the bottom of the conduction band is continuously changed to be curved in the vicinity of the interface between the oxide semiconductor layer 208 and each of the first oxide layer 207 and the second oxide layer 209. The energy band gap of the oxide layer represented by an In-*M*-Zn oxide becomes larger as the proportion of the element *M* increases. Hence, a mixed region (mixed layer) of each layer is formed in the vicinity of the interface between the oxide semiconductor layer 208 and each of the first oxide layer 207 and the second oxide layer 209. The proportion of the element *M* thus changes gradually in the mixed region, whereby the round well shown in FIG. 5D is probably obtained. In addition, oxygen is easily diffused in the first oxide layer 207, the oxide semiconductor layer 208, and the second oxide layer 209 because these layers have similar compositions. On the contrary, the mixed region is unlikely to be formed between the insulating layer 206 and the first oxide layer 207 and between the second oxide layer 209 and the insulating layer 214 because these layers have different compositions. Therefore, a continuous change is not observed in the energy band diagram.

[0129]

When the energy at the bottom of the conduction band has a round well in the vicinity of the interface between the oxide semiconductor layer 208 and each of the first oxide layer 207 and the second oxide layer 209, electric field concentration can be reduced in the vicinity of the interface.

[0130]

FIG. 5D shows an example in which the energy at the bottom of the conduction band of the first oxide layer 207 is closer to the vacuum level than the energy at the bottom of the conduction band of the second oxide layer 209 is. However, the first oxide

layer 207 and the second oxide layer 209 may have the same energy at the bottom of the conduction band, or the energy at the bottom of the conduction band of the second oxide layer 209 may be closer to the vacuum level than the energy at the bottom of the conduction band of the first oxide layer 207 is.

[0131]

Since each of the first oxide layer 207 and the second oxide layer 209 contains one or more kinds of metal elements contained in the oxide semiconductor layer 208, the layered structure including these layers can also be regarded as an oxide stack of layers containing the same main components. The oxide stack of layers containing the same main components is formed not simply by stacking layers but to have a continuous junction (here, in particular, a U-shaped (round) well structure in which energy at the bottom of the conduction band is changed continuously between the layers). This is because when impurities which form a defect state such as a trap center or a recombination center are mixed at each interface, the continuity of the energy band is lost, and thus carriers are trapped or disappear by recombination at the interface.

[0132]

To form a continuous junction, it is necessary to stack the layers in succession without exposure to the air using a multi-chamber deposition apparatus (sputtering apparatus) provided with load lock chambers. Each chamber of the sputtering apparatus is preferably evacuated to a high vacuum (to about 5×10^{-7} Pa to 1×10^{-4} Pa) by an adsorption vacuum pump such as a cryopump so that water and the like acting as impurities for the oxide semiconductor are removed as much as possible. Alternatively, a combination of a turbo molecular pump and a cold trap is preferably used to prevent back-flow of a gas from an exhaust system into a chamber.

[0133]

Not only high vacuum evacuation in a chamber but also high purity of a sputtering gas is necessary to obtain a highly purified intrinsic oxide semiconductor. An oxygen gas or an argon gas used as the sputtering gas is preferably highly purified to have a dew point of −40 °C or lower, preferably −80 °C or lower, and more preferably −100 °C or lower, whereby entry of moisture or the like into the oxide semiconductor can be prevented as much as possible.

[0134]

The first oxide layer 207 and the second oxide layer 209 which are provided over and under the oxide semiconductor layer 208 each serve as a barrier layer and can prevent trap levels formed at an interface between the oxide stack and each of the insulating layers in contact with the oxide stack (the insulating layer 206 and the insulating layer 214) from adversely affecting the oxide semiconductor layer 208 that serves as a main carrier path for the transistor.

[0135]

Specifically, the first oxide layer 207 and the second oxide layer 209 in which oxygen vacancies are less likely to be generated than in the oxide semiconductor layer 208 are provided over and under and in contact with the oxide semiconductor layer 208, allowing a reduction in the amount of oxygen vacancies in the oxide semiconductor layer 208. This prevents the formation of trap levels at the interface with the oxide semiconductor layer 208 due to oxygen vacancies. For example, in the oxide semiconductor layer 208, the absorption coefficient due to the localized levels, which is measured by a constant photocurrent method (CPM) is set lower than 1×10^{-3}/cm, preferably lower than 1×10^{-4}/cm.

[0136]

In addition, when the back channel side of the oxide semiconductor layer 208 is in contact with an insulating layer 214 including a different constituent element (e.g., an insulating layer including a silicon oxide film), an interface state is sometimes formed at the interface of the two layers and the interface state forms a channel. In that case, a second transistor having a different threshold voltage is formed in some cases, which might vary the apparent threshold voltage of the transistor. However, in the transistor 280, the second oxide layer 209 contains one or more kinds of metal elements contained in the oxide semiconductor layer 208; thus, an interface state is less likely to be formed at the interface with the back channel side of the oxide semiconductor layer 208. The second oxide layer 209 thus makes it possible to reduce variation in the electrical characteristics of the transistor, such as a threshold voltage.

[0137]

When a channel is formed at an interface between the insulating layer 206 functioning as the gate insulating layer and the oxide semiconductor layer 208, interface scattering occurs at the interface and the field-effect mobility of the transistor decreases.

However, in the transistor 280, the first oxide layer 207 contains one or more kinds of metal elements contained in the oxide semiconductor layer 208; thus, scattering of carriers is less likely to occur at the interface with the front channel side of the oxide semiconductor layer 208, and the field-effect mobility of the transistor can be increased.

[0138]

Moreover, the first oxide layer 207 and the second oxide layer 209 each also serve as a barrier layer which suppresses formation of an impurity state due to entry of the constituent elements of the insulating layer 206 and the insulating layer 212 into the oxide semiconductor layer 208.

[0139]

For example, the concentration of silicon contained in the oxide semiconductor layer 208 is lower than or equal to $3 \times 10^{18}/cm^3$, preferably lower than or equal to $3 \times 10^{17}/cm^3$. The concentration of carbon contained in the oxide semiconductor layer 208 is lower than or equal to $3 \times 10^{18}/cm^3$, preferably lower than or equal to $3 \times 10^{17}/cm^3$.

[0140]

Note that the impurity concentration in the oxide semiconductor layer can be measured by secondary ion mass spectrometry (SIMS).

[0141]

The thickness of each of the first oxide layer 207 and the second oxide layer 209 is determined so as to prevent constituent elements of the insulating layers 206 and 214, which serve as impurities in the oxide semiconductor, from entering the oxide semiconductor layer 208. An increase in the thickness of the oxide semiconductor layer 208 results in an increase in the on-state current of the transistor 280. Therefore, the thickness of the oxide semiconductor layer 208 is preferably at least larger than the thickness of each of the first oxide layer 207 and the second oxide layer 209.

[0142]

Since the first oxide layer 207 is provided between the gate electrode layer and the oxide semiconductor layer 208 serving as a channel, the thickness of the first oxide layer 207 is preferably as small as possible for an increase in the on-state current of the transistor. Specifically, the thickness of the first oxide layer 207 is, for example, greater than or equal to 0.3 nm and less than 10 nm, preferably greater than or equal to 0.3 nm and less than or equal to 5 nm.

[0143]

If hydrogen or moisture is contained as an impurity in the oxide semiconductor layer, it serves as a donor and forms an n-type region. Therefore, in order to achieve a well-shaped structure, it is useful to provide the insulating layer 206 under the first oxide layer 207 and the insulating layer 212 over the second oxide layer 209, because the insulating layers 206 and 212 each include an aluminum oxide film that prevents entry of hydrogen or moisture from the outside.

[0144]

When the energy difference between the bottom of the conduction band of the first oxide layer 207 or the second oxide layer 209 and the bottom of the conduction band of the oxide semiconductor layer 208 is small, an electron in the oxide semiconductor layer 208 might reach the trap level by passing over the energy difference. When the electron is trapped in the trap level, a negative fixed charge is generated at the interface with the insulating film and the threshold voltage of the transistor shifts in the positive direction.

[0145]

Thus, the energy difference between the bottom of the conduction band of the first oxide layer 207 or the second oxide layer 209 and the bottom of the conduction band of the oxide semiconductor layer 208 is preferably greater than or equal to 0.1 eV, more preferably greater than or equal to 0.15 eV, in which case variation in the threshold voltage of the transistor is reduced and stable electrical characteristics can be obtained.

[0146]

FIGS. 6A to 6C illustrate an example of another structure of the transistor of this embodiment. FIG. 6A is a plan view of a transistor 280, FIG. 6B is a cross-sectional view taken along line V4-W4 in FIG. 6A, and FIG. 6C is a cross-sectional view taken along line X4-Y4 in FIG. 6A.

[0147]

The transistor 280 illustrated in FIGS. 6A to 6C is different from the transistor 270 in FIGS. 5A to 5D in that the second oxide layer 209 is provided over the source electrode layer 210a and the drain electrode layer 210b so as to cover the oxide semiconductor layer 208 which is not covered with the source electrode layer 210a and the drain electrode layer 210b. The other components of the transistor 280 can be similar to

those of the transistor 270.

[0148]

In the transistor 280, a first oxide film to be the first oxide layer 207 and an oxide semiconductor film are formed in succession over the insulating layer 206. After that, the first oxide film and the oxide semiconductor film are processed into island shapes by etching using a resist mask, whereby the first oxide layer 207 and the oxide semiconductor layer 208 are formed. Then, the source electrode layer 210a and the drain electrode layer 210b are formed in contact with part of the first oxide layer 207 and the oxide semiconductor layer 208. A second oxide film to be the second oxide layer 209 and the insulating film 214a are formed in succession over and in contact with the source electrode layer 210a and the drain electrode layer 210b so as to cover the oxide semiconductor layer 208 not covered with the source electrode layer 210a and the drain electrode layer 210b. Next, the second oxide film and the insulating film 214a are processed using the second gate electrode layer 216 as a mask, whereby the second oxide layer 209 and the insulating layer 214 are formed.

[0149]

In the above process, the first oxide film and the oxide semiconductor film, or the second oxide film and the insulating film 214a are preferably formed in succession without exposure to the air, in which case impurities such as hydrogen or moisture can be prevented from being adsorbed on the interface of each layer.

[0150]

As mentioned above, the first oxide layer 207 and the oxide semiconductor layer 208 in the transistor 280 are processed using the same resist mask. Accordingly, the top edge of the first oxide layer 207 is substantially aligned with the bottom edge of the oxide semiconductor layer 208. In other words, the first oxide layer 207 and the oxide semiconductor layer 208 have substantially the same top surface shape. The second oxide layer 209 and the insulating layer 214 are processed using the second gate electrode layer 216 as a mask. Accordingly, the top edge of the second oxide layer 209 is substantially aligned with the bottom edge of the insulating layer 214 and the top edge of the insulating layer 214 is substantially aligned with the bottom edge of the second gate electrode layer 216. In other words, the second oxide layer 209, the insulating layer 214, and the second gate electrode layer 216 have substantially the same top surface shape.

[0151]

In the transistor 280, after the first oxide layer 207 and the oxide semiconductor layer 208 are processed into island shapes, the second oxide film to be the second oxide layer 209 is formed to cover the island-like first oxide layer 207 and the island-like oxide semiconductor layer 208. As a result, the side surfaces of the oxide semiconductor layer 208 and the first oxide layer 207 in the channel width direction are covered with the second oxide layer 209. This suppresses the formation of interface states in the side surface of the oxide semiconductor layer 208 in the channel width direction.

[0152]

In the transistor of this embodiment, the oxide layers including at least one of metal elements contained in the oxide semiconductor layer 208 are provided between the oxide semiconductor layer 208 and each of a gate insulating layer and a protective insulating layer which overlap with the oxide semiconductor layer 208. This suppresses the formation of trap states at the interfaces between the oxide semiconductor layer 208 and each of the insulating layers overlapping with the oxide semiconductor layer 208. As a result, deterioration of the electrical characteristics of the transistor can be minimized.

[0153]

In the transistor of this embodiment, an electric field is applied to the oxide semiconductor layer 208 vertically from the first gate electrode layer 202 under the oxide semiconductor layer 208 and the second gate electrode layer 216 over the oxide semiconductor layer 208, allowing the threshold voltage of the transistor to be controlled effectively.

[0154]

Also in this embodiment, the second gate electrode layer 216 overlapping with the oxide semiconductor layer 208 with the second gate insulating layer interposed therebetween is provided to overlap with the side surface and bottom surface of a channel formation region in the oxide semiconductor layer 208. As a result, the electric field is applied to the channel formation region from the side surface and the bottom surface, allowing the threshold voltage of the transistor to be controlled more effectively and the S value to be reduced.

[0155]

Furthermore, in the transistor of this embodiment, the oxide semiconductor layer 208 is surrounded by the insulating layers 206 and 212 each including an aluminum oxide film containing excess oxygen. This allows sufficient oxygen to be supplied to the oxide semiconductor layer 208 surrounded by the insulating layers 206 and 212, and minimizes removal of oxygen from the oxide semiconductor layer 208 and entry of impurities such as hydrogen in the oxide semiconductor layer 208.

[0156]

It is more effective that the oxide semiconductor layer 208 be surrounded by the insulating layers including an aluminum oxide film containing excess oxygen while the oxide semiconductor layer 208 be in contact with the oxide layers including at least one of metal elements contained in the oxide semiconductor layer 208. In that case, carrier scattering which might occur at the interface of the oxide semiconductor layer 208 including the channel can be further reduced.

[0157]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0158]

[Embodiment 3]

Described in this embodiment is an example of an oxide semiconductor layer that can be applied to the transistors of Embodiment 1 or 2.

[0159]

An oxide semiconductor layer is classified roughly into a non-single-crystal oxide semiconductor layer and a single crystal oxide semiconductor layer. The non-single-crystal oxide semiconductor layer includes a c-axis aligned crystalline oxide semiconductor (CAAC-OS) layer, a polycrystalline oxide semiconductor layer, a microcrystalline oxide semiconductor layer, an amorphous oxide semiconductor layer, and the like.

[0160]

First, a CAAC-OS film is described.

[0161]

The CAAC-OS film is one of oxide semiconductor layers including a plurality of c-axis aligned crystal parts

[0162]

In a transmission electron microscope (TEM) image of the CAAC-OS film, it is difficult to clearly observe a boundary between crystal parts, that is, a grain boundary. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0163]

According to the TEM image of the CAAC-OS film observed in a direction substantially parallel to a sample surface (cross-sectional TEM image), metal atoms are arranged in a layered manner in the crystal parts. Each metal atom layer has a morphology reflected by a surface over which the CAAC-OS film is formed (hereinafter, a surface over which the CAAC-OS film is formed is referred to as a formation surface) or a top surface of the CAAC-OS film, and is arranged in parallel to the formation surface or the top surface of the CAAC-OS film.

[0164]

On the other hand, according to the TEM image of the CAAC-OS film observed in a direction substantially perpendicular to the sample surface (plan TEM image), metal atoms are arranged in a triangular or hexagonal configuration in the crystal parts. However, there is no regularity of arrangement of metal atoms between different crystal parts.

[0165]

From the results of the cross-sectional TEM image and the plan TEM image, alignment is found in the crystal parts in the CAAC-OS film.

[0166]

Most of the crystal parts included in the CAAC-OS film each fit inside a cube whose one side is less than 100 nm. Thus, there is a case where a crystal part included in the CAAC-OS film fits inside a cube whose one side is less than 10 nm, less than 5 nm, or less than 3 nm. Note that when a plurality of crystal parts included in the CAAC-OS film are connected to each other, one large crystal region is formed in some cases. For example, a crystal region with an area of 2500 nm^2 or more, 5 μm^2 or more, or 1000 μm^2 or more is observed in some cases in the plan TEM image.

[0167]

A CAAC-OS film is subjected to structural analysis with an X-ray diffraction

(XRD) apparatus. For example, when the CAAC-OS film including an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak appears frequently when the diffraction angle (2θ) is around 31°. This peak is derived from the (009) plane of the $InGaZnO_4$ crystal, which indicates that crystals in the CAAC-OS film have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS film.

[0168]

On the other hand, when the CAAC-OS film is analyzed by an in-plane method in which an X-ray enters a sample in a direction substantially perpendicular to the c-axis, a peak appears frequently when 2θ is around 56°. This peak is derived from the (110) plane of the $InGaZnO_4$ crystal. Here, analysis (ϕ scan) is performed under conditions where the sample is rotated around a normal vector of a sample surface as an axis (ϕ axis) with 2θ fixed at around 56°. In the case where the sample is a single crystal oxide semiconductor film of $InGaZnO_4$, six peaks appear. The six peaks are derived from crystal planes equivalent to the (110) plane. On the other hand, in the case of a CAAC-OS film, a peak is not clearly observed even when ϕscan is performed with 2θ fixed at around 56°.

[0169]

According to the above results, in the CAAC-OS film having c-axis alignment, while the directions of a-axes and b-axes are different between crystal parts, the c-axes are aligned in a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, each metal atom layer arranged in a layered manner observed in the cross-sectional TEM image corresponds to a plane parallel to the a-b plane of the crystal.

[0170]

Note that the crystal part is formed concurrently with deposition of the CAAC-OS film or is formed through crystallization treatment such as heat treatment. As described above, the c-axis of the crystal is aligned with a direction parallel to a normal vector of a formation surface or a normal vector of a top surface. Thus, for example, in the case where a shape of the CAAC-OS film is changed by etching or the like, the c-axis might not be necessarily parallel to a normal vector of a formation surface or a normal vector of a top surface of the CAAC-OS film.

[0171]

Further, distribution of c-axis aligned crystal parts in the CAAC-OS film is not necessarily uniform. For example, in the case where crystal growth leading to the crystal parts of the CAAC-OS film occurs from the vicinity of the top surface of the CAAC-OS film, the proportion of the c-axis aligned crystal parts in the vicinity of the top surface is higher than that in the vicinity of the formation surface in some cases. Furthermore, when an impurity is added to the CAAC-OS film, a region to which the impurity is added is altered, and the proportion of the c-axis aligned crystal parts in the CAAC-OS film varies depending on regions, in some cases.

[0172]

Note that when the CAAC-OS film with an $InGaZnO_4$ crystal is analyzed by an out-of-plane method, a peak of 2θ may also be observed at around 36°, in addition to the peak of 2θ at around 31°. The peak of 2θ at around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS film. It is preferable that in the CAAC-OS film, a peak of 2θ appear at around 31° and a peak of 2θ do not appear at around 36°.

[0173]

The CAAC-OS film is an oxide semiconductor layer having low impurity concentration. The impurity is an element other than the main components of the oxide semiconductor layer, such as hydrogen, carbon, silicon, or a transition metal element. In particular, an element (e.g., silicon) that has higher bonding strength to oxygen than a metal element included in the oxide semiconductor layer disturbs the atomic arrangement of the oxide semiconductor layer by depriving the oxide semiconductor layer of oxygen and causes a decrease in crystallinity. In addition, a heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor layer and causes a decrease in crystallinity when it is contained in the oxide semiconductor layer. Note that the impurity contained in the oxide semiconductor layer might serve as a carrier trap or a carrier generation source.

[0174]

The CAAC-OS film is an oxide semiconductor layer having a low density of defect states. For example, oxygen vacancies in the oxide semiconductor layer serve as

carrier traps or serve as carrier generation sources when hydrogen is captured therein.

[0175]

An oxide semiconductor layer having a low impurity concentration and a low density of defect states (having few oxygen vacancies), in other words, a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor layer has few carrier generation sources, and thus can have a low carrier density. Thus, a transistor using the oxide semiconductor layer rarely has negative threshold voltage (is rarely normally on). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor layer has few carrier traps. Accordingly, the transistor using the oxide semiconductor layer has little variation in electrical characteristics and high reliability. Note that charges trapped by the carrier traps in the oxide semiconductor layer take a long time to be released and may behave like fixed charges. Thus, the transistor using the oxide semiconductor layer with a high impurity concentration and a high density of defect states has unstable electrical characteristics in some cases.

[0176]

A transistor using the CAAC-OS film has little variation in electrical characteristics due to irradiation with visible light or ultraviolet light.

[0177]

Next, a microcrystalline oxide semiconductor layer will be described.

[0178]

In an image obtained with a TEM, crystal parts cannot be found clearly in the microcrystalline oxide semiconductor layer in some cases. In most cases, the size of a crystal part included in the microcrystalline oxide semiconductor layer is greater than or equal to 1 nm and less than or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. A microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as nanocrystal (nc). An oxide semiconductor layer including nanocrystal is referred to as an nc-OS (nanocrystalline oxide semiconductor) film. In an image of the nc-OS film obtained with a TEM, for example, a boundary between crystal parts is not clearly observed in some cases.

[0179]

In the nc-OS film, a microscopic region (e.g., a region with a size greater than or

equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic order. The nc-OS film does not have regularity of crystal orientation between different crystal parts. Thus, the orientation of the whole film is not observed. Accordingly, in some cases, the nc-OS film cannot be distinguished from an amorphous oxide semiconductor layer depending on an analysis method. For example, when the nc-OS film is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a diameter larger than that of a crystal part, a peak which shows a crystal plane does not appear. Furthermore, a halo pattern is shown in an electron diffraction pattern (also referred to as a selected-area electron diffraction pattern) of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 50 nm) larger than the diameter of a crystal part. Meanwhile, spots are shown in a nanobeam electron diffraction pattern of the nc-OS film obtained by using an electron beam having a probe diameter (e.g., larger than or equal to 1 nm and smaller than or equal to 30 nm) close to, or smaller than the diameter of a crystal part. Furthermore, in a nanobeam electron diffraction pattern of the nc-OS film regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS film, a plurality of spots are shown in a ring-like region in some cases.

[0180]

Since the nc-OS film is an oxide semiconductor layer having more regularity than the amorphous oxide semiconductor layer, the nc-OS film has a lower density of defect states than the amorphous oxide semiconductor layer. However, there is no regularity of crystal orientation between different crystal parts in the nc-OS film; hence, the nc-OS film has a higher density of defect states than the CAAC-OS film.

[0181]

Note that an oxide semiconductor layer may be a stacked film including two or more layers of an amorphous oxide semiconductor layer, a microcrystalline oxide semiconductor layer, and a CAAC-OS film, for example.

[0182]

An example of a method for forming a CAAC-OS film will be described under.

[0183]

For example, the CAAC-OS film is formed by a sputtering method using a

polycrystalline oxide semiconductor sputtering target. When ions collide with the sputtering target, a crystal region included in the sputtering target may be separated from the target along an a-b plane; in other words, a sputtered particle having a plane parallel to an a-b plane (flat-plate-like sputtered particle or pellet-like sputtered particle) may flake off from the sputtering target. In that case, the flat-plate-like sputtered particle or the pellet-like sputtered particle reaches a substrate while maintaining their crystal state, whereby the CAAC-OS film can be formed.

[0184]

The flat-plate-like sputtered particle or the pellet-like sputtered particle has, for example, an equivalent circle diameter of a plane parallel to the a-b plane of greater than or equal to 3 nm and less than or equal to 10 nm, and a thickness (length in the direction perpendicular to the a-b plane) of greater than or equal to 0.7 nm and less than 1 nm. Note that in the flat-plate-like sputtered particle or the pellet-like sputtered particle, the plane parallel to the a-b plane may be a regular triangle or a regular hexagon. Here, the term "equivalent circle diameter of a plane" refers to the diameter of a perfect circle having the same area as the plane.

[0185]

For the deposition of the CAAC-OS film, the following conditions are preferably used.

[0186]

By increasing the substrate temperature during the deposition, migration of sputtered particles is likely to occur after the sputtered particles reach a substrate surface. Specifically, the substrate temperature during the deposition is higher than or equal to 100 °C and lower than or equal to 740 °C. By increasing the substrate temperature during the deposition, when the flat-plate-like sputtered particles or the pellet-like sputtered particles reach the substrate, migration occurs on the substrate surface, so that a flat plane of the sputtered particles is attached to the substrate. At this time, the sputtered particle is charged positively, whereby sputtered particles are attached to the substrate while repelling each other; thus, the sputtered particles do not overlap with each other randomly, and a CAAC-OS film with a uniform thickness can be deposited. When the temperature for deposition is too high, zinc contained in a target might be sublimed; therefore, the substrate temperature is higher than or equal to 200 °C and lower than or equal to 500 °C,

preferably higher than or equal to 200 °C and lower than or equal to 350 °C.

[0187]

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being broken by the impurities. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) that exist in the deposition chamber may be reduced. Furthermore, the concentration of impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is −80 °C or lower, preferably −100 °C or lower is used.

[0188]

Furthermore, it is preferable that the proportion of oxygen in the deposition gas be increased and the power be optimized in order to reduce plasma damage at the deposition. The proportion of oxygen in the deposition gas is higher than or equal to 30 vol%, preferably 100 vol%.

[0189]

Alternatively, the CAAC-OS film is formed by the following method.

[0190]

First, a first oxide semiconductor film is formed to a thickness greater than or equal to 1 nm and less than 10 nm. The first oxide semiconductor film is formed by a sputtering method. Specifically, the substrate temperature is higher than or equal to 100 °C and lower than or equal to 500 °C, preferably higher than or equal to 150 °C and lower than or equal to 450 °C, and the proportion of oxygen in a deposition gas is higher than or equal to 30 vol%, preferably 100 vol%.

[0191]

Then, the first oxide semiconductor film is subjected to heat treatment to be a first CAAC-OS film with high crystallinity. The temperature of the heat treatment is higher than or equal to 350 °C and lower than or equal to 740 °C, preferably higher than or equal to 450 °C and lower than or equal to 650 °C. The heat treatment time is longer than or equal to 1 minute and shorter than or equal to 24 hours, preferably longer than or equal to 6 minutes and shorter than or equal to 4 hours. The heat treatment may be performed in an inert atmosphere or an oxidation atmosphere. It is preferable to perform heat treatment in an inert atmosphere and then perform heat treatment in an oxidation atmosphere. The heat treatment in an inert atmosphere can reduce the concentration of

impurities in the first oxide semiconductor film in a short time. At the same time, the heat treatment in an inert atmosphere may generate oxygen vacancies in the first oxide semiconductor film. In such a case, the heat treatment in an oxidation atmosphere can reduce the oxygen vacancies. Note that the heat treatment may be performed under a reduced pressure, such as 1000 Pa or lower, 100 Pa or lower, 10 Pa or lower, or 1 Pa or lower. The heat treatment under the reduced pressure can reduce the concentration of impurities in the first oxide semiconductor film in a shorter time.

[0192]

The first oxide semiconductor film with a thickness greater than or equal to 1 nm and less than 10 nm can be easily crystallized by heat treatment as compared to the case where the first oxide semiconductor film has a thickness greater than or equal to 10 nm.

[0193]

Next, a second oxide semiconductor film having the same composition as the first oxide semiconductor film is formed to a thickness greater than or equal to 10 nm and less than or equal to 50 nm. The second oxide semiconductor film is formed by a sputtering method. Specifically, the substrate temperature is set to higher than or equal to 100 °C and lower than or equal to 500 °C, preferably higher than or equal to 150°C and lower than or equal to 450 °C, and the proportion of oxygen in a deposition gas is set to higher than or equal to 30 vol%, preferably 100 vol%.

[0194]

Next, heat treatment is performed so that solid phase growth of the second oxide semiconductor film is performed using the first CAAC-OS film, thereby forming a second CAAC-OS film with high crystallinity. The temperature of the heat treatment is higher than or equal to 350 °C and lower than or equal to 740 °C, preferably higher than or equal to 450 °C and lower than or equal to 650 °C. The heat treatment time is longer than or equal to 1 minute and shorter than or equal to 24 hours, preferably longer than or equal to 6 minutes and shorter than or equal to 4 hours. The heat treatment may be performed in an inert atmosphere or an oxidation atmosphere. It is preferable to perform heat treatment in an inert atmosphere and then perform heat treatment in an oxidation atmosphere. The heat treatment in an inert atmosphere can reduce the concentration of impurities in the second oxide semiconductor film in a short time. At the same time, the heat treatment in an inert atmosphere may generate oxygen vacancies in the second oxide

semiconductor film. In such a case, the heat treatment in an oxidation atmosphere can reduce the oxygen vacancies. Note that the heat treatment may be performed under a reduced pressure, such as 1000 Pa or lower, 100 Pa or lower, 10 Pa or lower, or 1 Pa or lower. The heat treatment under the reduced pressure can reduce the concentration of impurities in the second oxide semiconductor film in a shorter time.

[0195]

In the above manner, a CAAC-OS film with a total thickness greater than or equal to 10 nm can be obtained. The CAAC-OS film can be favorably used as the oxide semiconductor layer in the oxide stack.

[0196]

Described next is a method for forming an oxide film in the case where a formation surface has a low temperature because, for example, the substrate is not heated is described (for example, the temperature is lower than 130 °C, lower than 100 °C, lower than 70 °C or at room temperatures (20 °C to 25 °C)).

[0197]

In the case where the formation surface has a low temperature, sputtered particles fall irregularly to the formation surface. For example, migration does not occur; therefore, the sputtered particles are randomly deposited on the deposition surface including a region where other sputtered particles have been deposited. That is, an oxide film obtained by the deposition might have a non-uniform thickness and a disordered crystal alignment. The oxide film obtained in the above manner maintains the crystallinity of the sputtered particles to a certain degree and thus has a crystal part (nanocrystal).

[0198]

For example, in the case where the pressure at the deposition is high, the frequency with which the flying sputtered particle collides with another particle (e.g., an atom, a molecule, an ion, or a radical) of argon or the like is increased. When the flying sputtered particle collides with another particle (resputtered), the crystal structure of the sputtered particle might be broken. For example, when the sputtered particle collides with another particle, the plate-like or pellet-like shape of the sputtered particle cannot be kept, and the sputtered particle might be broken into parts (e.g., atomized). At this time, when atoms obtained from the sputtered particle are deposited on the formation surface, an

amorphous oxide semiconductor film might be formed.

[0199]

In the case where not a sputtering method using a target including polycrystalline oxide but a deposition method using liquid or a method for depositing a film by vaporizing a solid such as a target is used, the atoms separately fly to be deposited over the formation surface; therefore, an amorphous oxide film might be formed. For example, by a laser ablation method, atoms, molecules, ions, radials, clusters, or the like released from the target fly to be deposited over the formation surface; therefore, an amorphous oxide film might be formed.

[0200]

In the case where an oxide semiconductor layer is interposed between oxide layers in a transistor of one embodiment of the present invention, the first oxide layer, the oxide semiconductor layer, and the second oxide layer may each have any of the above crystal states. Note that it is preferable to use a CAAC-OS film as the oxide semiconductor layer serving as a channel.

[0201]

The structures, the methods, and the like described in this embodiment can be combined as appropriate with any of the structures, the methods, and the like described in the other embodiments.

[0202]

[Embodiment 4]

In this embodiment, examples of a circuit using the transistor shown in Embodiment 1 or 2 will be described with reference to FIGS. 11A to 11C.

[0203]

FIG. 11A is a circuit diagram of a semiconductor device and FIG. 11C is a cross-sectional view of the semiconductor device. The left side of FIG. 11C is a cross-sectional view of the transistor 260 in the channel length direction and the right side is a cross-sectional view of the transistor 260 in the channel width direction. In the circuit diagram, OS denotes a transistor including an oxide semiconductor.

[0204]

In the semiconductor device illustrated in FIG. 11C, a transistor 2200 including a first semiconductor material is provided in a lower portion and a transistor including a

second semiconductor material is provided in an upper portion. Described here is an example of using the transistor 260 shown in Embodiment 1 as the transistor including the second semiconductor material.

[0205]

Here, the first semiconductor material and the second semiconductor material preferably have different band gaps. For example, the first semiconductor material can be a semiconductor material (such as silicon, germanium, silicon germanium, silicon carbide, or gallium arsenide) other than an oxide semiconductor, and the second semiconductor material can be any of the oxide semiconductors described in Embodiment 1. A transistor including, for example, single crystal silicon as a material other than an oxide semiconductor can operate at high speed easily. On the other hand, a transistor including an oxide semiconductor has a low off-state current.

[0206]

Although the transistor 2200 is a p-channel transistor here, it is needless to say that an n-channel transistor can be used to form a circuit having a different configuration. The specific structure of the semiconductor device, such as a material used for the semiconductor device and the structure of the semiconductor device, does not need to be limited to that described here except for the use of the transistor including an oxide semiconductor described in Embodiment 1 or 2.

[0207]

FIGS. 11A and 11C illustrate a configuration example of what is called a CMOS circuit, in which a p-channel transistor and an n-channel transistor are connected in series and gates of the transistors are connected.

[0208]

As illustrated in FIG. 11C, the transistor 260 is stacked over the transistor 2200. The stack of the two transistors reduces the area occupied by the circuit, allowing a plurality of circuits to be highly integrated. In addition, the first gate electrode of the transistor 260 can be used in common with a gate electrode layer of the transistor 2200. This is effective for higher integration of the semiconductor device and shortening of manufacturing process of the semiconductor device.

[0209]

In FIG. 11C, one of the source and the drain of the transistor 260 is electrically

connected to one of a source and a drain of the transistor 2200 via a plug.

[0210]

The transistor including the oxide semiconductor of one embodiment of the present invention has an increased on-state current, which enables high speed operation of the circuit.

[0211]

When the connection between the electrodes of the transistor 260 and the transistor 2200 is changed from that in the configuration illustrated in FIG. 11C, a variety of circuits can be formed. For example, as illustrated in FIG. 11B, one of the source and the drain of the transistor 260 is connected to one of the source and the drain of the transistor 2200 and the other of the source and the drain of the transistor 260 is connected to the other of the source and the drain of the transistor 260, whereby what is called an analog switch can be obtained.

[0212]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0213]

[Embodiment 5]

In this embodiment, an example of a semiconductor device (memory device) using the transistor shown in Embodiment 1 or 2 will be described with reference to drawings. The semiconductor device (memory device) can retain data even when not powered, and has an unlimited number of write cycles.

[0214]

FIG. 7 is a circuit diagram of the semiconductor device.

[0215]

The semiconductor device illustrated in FIG. 7 includes a transistor 3200 using a first semiconductor material, a transistor 3300 using a second semiconductor material, and a capacitor 3400. Note that the transistor shown in Embodiment 1 or 2 can be used as the transistor 3300. In FIG. 7, "OS" is written beside the transistor 3300 so as to identify the transistor 3300 as including an oxide semiconductor.

[0216]

The transistor 3300 includes a channel formed in a semiconductor layer including

an oxide semiconductor. Since the off-state current of the transistor 3300 is low, stored data can be retained for a long period using such a transistor. In other words, it is possible to obtain a semiconductor memory device that does not need refresh operation or has an extremely low frequency of refresh operation, and thus has a sufficiently low power consumption.

[0217]

In FIG. 7, a first wiring 3001 is electrically connected to a source electrode of the transistor 3200. A second wiring 3002 is electrically connected to a drain electrode of the transistor 3200. A third wiring 3003 is electrically connected to one of a source electrode and a drain electrode of the transistor 3300. A fourth wiring 3004 is electrically connected to a gate electrode of the transistor 3300. A gate electrode of the transistor 3200 and the other of the source electrode and the drain electrode of the transistor 3300 are electrically connected to one electrode of the capacitor 3400. A fifth wiring 3005 is electrically connected to the other electrode of the capacitor 3400.

[0218]

In the semiconductor device in FIG. 7, the potential of the gate electrode of the transistor 3200 can be retained, whereby writing, retaining, and reading of data can be performed as follows.

[0219]

Writing and retaining of data are described. First, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned on, so that the transistor 3300 is turned on. Accordingly, the potential of the third wiring 3003 is supplied to the gate electrode of the transistor 3200 and the capacitor 3400. That is, a predetermined charge is supplied to the gate electrode of the transistor 3200 (writing). Here, one of two kinds of charges providing different potential levels (hereinafter referred to as a low-level charge and a high-level charge) is supplied. After that, the potential of the fourth wiring 3004 is set to a potential at which the transistor 3300 is turned off, so that the transistor 3300 is turned off. Thus, the charge supplied to the gate electrode of the transistor 3200 is retained (retaining).

[0220]

Since the off-state current of the transistor 3300 is extremely low, the charge of the gate electrode of the transistor 3200 is held for a long time.

[0221]

Next, reading of data is described. An appropriate potential (a reading potential) is supplied to the fifth wiring 3005 while a predetermined potential (a constant potential) is supplied to the first wiring 3001, whereby the potential of the second wiring 3002 varies depending on the amount of charge retained in the gate electrode of the transistor 3200. This is because in general, in the case of using an n-channel transistor as the transistor 3200, an apparent threshold voltage V_{th_H} at the time when the high-level charge is given to the gate electrode of the transistor 3200 is lower than an apparent threshold voltage V_{th_L} at the time when the low-level charge is given to the gate electrode of the transistor 3200. Here, an apparent threshold voltage refers to the potential of the fifth wiring 3005 which is needed to turn on the transistor 3200. Thus, the potential of the fifth wiring 3005 is set to a potential V_0 which is between V_{th_H} and V_{th_L}, whereby charge supplied to the gate electrode of the transistor 3200 can be determined. For example, in the case where the high-level charge is supplied in writing and the potential of the fifth wiring 3005 is V_0 ($> V_{th_H}$), the transistor 3200 is turned on. In the case where the low-level charge is supplied in writing, even when the potential of the fifth wiring 3005 is V_0 ($< V_{th_L}$), the transistor 3200 remains off. Thus, the data retained in the gate electrode can be read by determining the potential of the second wiring 3002.

[0222]

Note that in the case where memory cells are arrayed, it is necessary that only data of a desired memory cell be able to be read. In the case where data is not read, the fifth wiring 3005 may be supplied with a potential at which the transistor 3200 is turned off regardless of the state of the gate electrode, that is, a potential lower than V_{th_H}. Alternatively, the fifth wiring 3005 may be supplied with a potential at which the transistor 3200 is turned on regardless of the state of the gate electrode, that is, a potential higher than V_{th_L}.

[0223]

The semiconductor device described in this embodiment includes a transistor having a channel formation region using an oxide semiconductor and thus having an extremely low off-state current; accordingly, data can be retained for an extremely long time. In other words, it is possible to obtain a semiconductor device that does not need refresh operation or has an extremely low frequency of refresh operation, and thus has a

sufficiently low power consumption. Moreover, stored data can be retained for a long time even when power is not supplied (note that a potential is preferably fixed).

[0224]

Furthermore, in the semiconductor device of this embodiment, high voltage is not needed for writing data and there is no problem of deterioration of elements. Unlike in a conventional nonvolatile memory, for example, it is not necessary to inject and extract electrons into and from a floating gate; thus, a problem such as deterioration of a gate insulating layer does not occur. That is, in the semiconductor device of the disclosed invention, there is no limitation on the number of times of rewritting unlike in a conventional nonvolatile memory. As a result, the reliability of the semiconductor device is drastically improved. Moreover, data is written depending on the state of the transistor (on or off), whereby high-speed operation can be easily achieved.

[0225]

As described above, a miniaturized and highly integrated semiconductor device having high electrical characteristics can be provided.

[0226]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0227]

[Embodiment 6]

Described in this embodiment is a CPU which can employ the transistor shown in Embodiment 1 or 2 and includes the memory device described in the above embodiment.

[0228]

FIG. 8 is a block diagram illustrating a configuration example of a CPU at least partly including the transistor shown in Embodiment 1 or 2.

[0229]

The CPU illustrated in FIG. 8 includes, over a substrate 1190, an arithmetic logic unit (ALU) 1191, an ALU controller 1192, an instruction decoder 1193, an interrupt controller 1194, a timing controller 1195, a register 1196, a register controller 1197, a bus interface (Bus I/F) 1198, a rewritable ROM 1199, and an ROM interface ROM I/F) 1189. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 1190. The rewritable ROM 1199 and the ROM interface 1189 may be provided

over a separate chip. Needless to say, the CPU in FIG. 8 is just an example in which the configuration has been simplified, and an actual CPU may have various configurations depending on the application. For example, the CPU may have the following configuration: a structure including the CPU illustrated in FIG. 8 or an arithmetic circuit is considered as one core; a plurality of the cores are included; and the cores operate in parallel. The number of bits that the CPU can process in an internal arithmetic circuit or in a data bus can be 8, 16, 32, or 64, for example.

[0230]

An instruction that is input to the CPU through the bus interface 1198 is input to the instruction decoder 1193 and decoded therein, and then, input to the ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195.

[0231]

The ALU controller 1192, the interrupt controller 1194, the register controller 1197, and the timing controller 1195 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 1192 generates signals for controlling the operation of the ALU 1191. While the CPU is executing a program, the interrupt controller 1194 judges an interrupt request from an external input/output device or a peripheral circuit on the basis of its priority or a mask state, and processes the request. The register controller 1197 generates an address of the register 1196, and reads/writes data from/to the register 1196 in accordance with the state of the CPU.

[0232]

The timing controller 1195 generates signals for controlling operation timings of the ALU 1191, the ALU controller 1192, the instruction decoder 1193, the interrupt controller 1194, and the register controller 1197. For example, the timing controller 1195 includes an internal clock generator for generating an internal clock signal CLK2 based on a reference clock signal CLK1, and supplies the internal clock signal CLK2 to the above circuits.

[0233]

In the CPU illustrated in FIG. 8, a memory cell is provided in the register 1196. As the memory cell of the register 1196, the transistor described in the above embodiment can be used.

[0234]

In the CPU illustrated in FIG. 8, the register controller 1197 selects operation of retaining data in the register 1196 in accordance with an instruction from the ALU 1191. That is, the register controller 1197 selects whether data is retained by a flip-flop or by a capacitor in the memory cell included in the register 1196. When data retaining by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register 1196. When data retaining by the capacitor is selected, the data is rewritten in the capacitor, and supply of power supply voltage to the memory cell in the register 1196 can be stopped.

[0235]

FIG. 9 is an example of a circuit diagram of a memory element that can be used as the register 1196. A memory element 700 includes a circuit 701 in which stored data is volatile when power supply is stopped, a circuit 702 in which stored data is nonvolatile even when power supply is stopped, a switch 703, a switch 704, a logic element 706, a capacitor 707, and a circuit 720 having a selecting function. The circuit 702 includes a capacitor 708, a transistor 709, and a transistor 710. Note that the memory element 700 may further include another element such as a diode, a resistor, or an inductor, as needed.

[0236]

Here, the memory device described in the above embodiment can be used as the circuit 702. When supply of a power supply voltage to the memory element 700 is stopped, a ground potential (0 V) or a potential at which the transistor 709 in the circuit 702 is turned off continues to be input to a gate of the transistor 709. For example, the gate of the transistor 709 is grounded through a load such as a resistor.

[0237]

Shown here is an example in which the switch 703 is a transistor 713 having one conductivity type (e.g., an n-channel transistor) and the switch 704 is a transistor 714 having a conductivity type opposite to the one conductivity type (e.g., a p-channel transistor). A first terminal of the switch 703 corresponds to one of a source and a drain of the transistor 713, a second terminal of the switch 703 corresponds to the other of the source and the drain of the transistor 713, and conduction or non-conduction between the first terminal and the second terminal of the switch 703 (i.e., the on/off state of the transistor 713) is selected by a control signal RD input to a gate of the transistor 713. A

first terminal of the switch 704 corresponds to one of a source and a drain of the transistor 714, a second terminal of the switch 704 corresponds to the other of the source and the drain of the transistor 714, and conduction or non-conduction between the first terminal and the second terminal of the switch 704 (i.e., the on/off state of the transistor 714) is selected by the control signal RD input to a gate of the transistor 714.

[0238]

One of a source and a drain of the transistor 709 is electrically connected to one of a pair of electrodes of the capacitor 708 and a gate of the transistor 710. Here, the connection portion is referred to as a node M2. One of a source and a drain of the transistor 710 is electrically connected to a line which can supply a low power supply potential (e.g., a GND line), and the other thereof is electrically connected to the first terminal of the switch 703 (the one of the source and the drain of the transistor 713). The second terminal of the switch 703 (the other of the source and the drain of the transistor 713) is electrically connected to the first terminal of the switch 704 (the one of the source and the drain of the transistor 714). The second terminal of the switch 704 (the other of the source and the drain of the transistor 714) is electrically connected to a line which can supply a power supply potential VDD. The second terminal of the switch 703 (the other of the source and the drain of the transistor 713), the first terminal of the switch 704 (the one of the source and the drain of the transistor 714), an input terminal of the logic element 706, and one of a pair of electrodes of the capacitor 707 are electrically connected to each other. Here, the connection portion is referred to as a node M1. The other of the pair of electrodes of the capacitor 707 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 707 can be supplied with a low power supply potential (e.g., GND) or a high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 707 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line). The other of the pair of electrodes of the capacitor 708 can be supplied with a constant potential. For example, the other of the pair of electrodes of the capacitor 708 can be supplied with the low power supply potential (e.g., GND) or the high power supply potential (e.g., VDD). The other of the pair of electrodes of the capacitor 708 is electrically connected to the line which can supply a low power supply potential (e.g., a GND line).

[0239]

The capacitor 707 and the capacitor 708 are not necessarily provided as long as the parasitic capacitance of the transistor, the wiring, or the like is actively utilized.

[0240]

A control signal WE is input to the first gate (first gate electrode) of the transistor 709. As for each of the switch 703 and the switch 704, a conduction state or a non-conduction state between the first terminal and the second terminal is selected by the control signal RD which is different from the control signal WE. When the first terminal and the second terminal of one of the switches are in the conduction state, the first terminal and the second terminal of the other of the switches are in the non-conduction state.

[0241]

A signal corresponding to data retained in the circuit 701 is input to the other of the source and the drain of the transistor 709. FIG. 9 illustrates an example in which a signal output from the circuit 701 is input to the other of the source and the drain of the transistor 709. The logic value of a signal output from the second terminal of the switch 703 (the other of the source and the drain of the transistor 713) is inverted by the logic element 706, and the inverted signal is input to the circuit 701 through the circuit 720.

[0242]

In the example of FIG. 9, a signal output from the second terminal of the switch 703 (the other of the source and the drain of the transistor 713) is input to the circuit 701 through the logic element 706 and the circuit 720; however, this embodiment is not limited thereto. The signal output from the second terminal of the switch 703 (the other of the source and the drain of the transistor 713) may be input to the circuit 701 without its logic value being inverted. For example, in the case where the circuit 701 includes a node in which a signal obtained by inversion of the logic value of a signal input from the input terminal is retained, the signal output from the second terminal of the switch 703 (the other of the source and the drain of the transistor 713) can be input to the node.

[0243]

As the transistor 709 in FIG. 9, the transistor described in Embodiment 1 or 2 can be used. The control signal WE can be input to a first gate and the control signal WE2 can be input to a second gate. The control signal WE2 is a signal having a constant potential. As the constant potential, for example, a ground potential GND or a potential

lower than a source potential of the transistor 709 is selected. The control signal WE2 is a potential signal for controlling the threshold voltage of the transistor 709, and Icut of the transistor 709 can be further reduced.

[0244]

In FIG. 9, the transistors included in the memory element 700 except for the transistor 709 can each be a transistor in which a channel is formed in a layer formed using a semiconductor other than an oxide semiconductor or in the substrate 1190. For example, a channel of transistor can be formed in a silicon layer or a silicon substrate. Alternatively, all the transistors in the memory element 700 may be a transistor in which a channel is formed in an oxide semiconductor layer. Further alternatively, in the memory element 700, a transistor in which a channel is formed in an oxide semiconductor layer can be included besides the transistor 709, and a transistor in which a channel is formed in a layer or the substrate 1190 including a semiconductor other than an oxide semiconductor can be used for the rest of the transistors.

[0245]

As the circuit 701 in FIG. 9, for example, a flip-flop circuit can be used. As the logic element 706, for example, an inverter or a clocked inverter can be used.

[0246]

In a period during which the memory element 700 is not supplied with the power supply voltage, the semiconductor device of one embodiment of the present invention can retain data stored in the circuit 701 by the capacitor 708 which is provided in the circuit 702.

[0247]

The off-state current of a transistor in which a channel is formed in an oxide semiconductor layer is extremely low. For example, the off-state current of a transistor in which a channel is formed in an oxide semiconductor layer is significantly lower than that of a transistor in which a channel is formed in silicon having crystallinity. Thus, when such a transistor including an oxide semiconductor is used for the transistor 709, a signal held in the capacitor 708 is retained for a long time also in a period during which the power supply voltage is not supplied to the memory element 700. The memory element 700 can accordingly retain the stored content (data) also in a period during which the supply of the power supply voltage is stopped.

[0248]

The memory element 700 performs pre-charge operation with the switch 703 and the switch 704, shortening the time required for the circuit 701 to retain original data again after the supply of the power supply voltage is restarted.

[0249]

In the circuit 702, a signal retained by the capacitor 708 is input to the gate of the transistor 710. Therefore, after supply of the power supply voltage to the memory element 700 is restarted, the signal retained by the capacitor 708 can be converted into the one corresponding to the state (the on state or the off state) of the transistor 710 to be read from the circuit 702. Consequently, an original signal can be accurately read even when a potential corresponding to the signal retained by the capacitor 708 varies to some degree.

[0250]

By applying the above-described memory element 700 to a memory device such as a register or a cache memory included in a processor, data in the memory device can be prevented from being lost owing to the stop of the supply of the power supply voltage. Furthermore, shortly after the supply of the power supply voltage is restarted, the memory device can be returned to the same state as that before the power supply is stopped. Therefore, the power supply can be stopped even for a short time in the processor or one or a plurality of logic circuits included in the processor, resulting in lower power consumption.

[0251]

Although the memory element 700 is used in a CPU in this embodiment, the memory element 700 can also be used in an LSI such as a digital signal processor (DSP), a custom LSI, or a programmable logic device (PLD), and a radio frequency identification (RF-ID).

[0252]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0253]

[Embodiment 7]

Described in this embodiment is a semiconductor device having an image sensor function for reading data of an object and including a transistor shown in Embodiment 1

or 2.

[0254]

FIG. 10 illustrates an example of an equivalent circuit of a semiconductor device having an image sensor function.

[0255]

One electrode of a photodiode 602 is electrically connected to a photodiode reset signal line 658, and the other electrode is electrically connected to a gate of a transistor 640. One of a source and a drain of the transistor 640 is electrically connected to a photosensor reference signal line 672, and the other of the source and the drain thereof is electrically connected to one of a source and a drain of a transistor 656. A gate of the transistor 656 is electrically connected to a gate signal line 659, and the other of the source and the drain thereof is electrically connected to a photosensor output signal line 671.

[0256]

The photodiode 602 can be, for example, a pin photodiode in which a p-type semiconductor layer, a high-resistance (i-type) semiconductor layer, and an n-type semiconductor layer.

[0257]

With detection of light that enters the photodiode 602, data of an object can be read. Note that a light source such as a backlight can be used at the time of reading data of an object.

[0258]

Note that the transistor shown in Embodiment 1 or 2, which includes a cannel formed in an oxide semiconductor, can be used as the transistor 640 and the transistor 656. In FIG. 10, "OS" is written beside the transistors 640 and 656 so as to identify the transistors as including an oxide semiconductor.

[0259]

Each of the transistors 640 and 656 is the one shown in the above embodiments, in which the oxide semiconductor layer including the channel is surrounded by the insulating layers including an aluminum oxide film containing excess oxygen. In addition, the oxide semiconductor layer is preferably electrically covered with the gate electrode layer. As a result, the transistors 640 and 656 have little variation in electrical characteristics and are electrically stable. With use of these transistors, the

semiconductor device having an image sensor function illustrated in FIG. 10 can have high reliability.

[0260]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

[0261]

[Embodiment 8]

Described in this embodiment are examples of an electronic device to which the transistor, the memory device, or the CPU and the like (including a DSP, a custom LSI, a PLD, and an RF-ID) described in the above embodiments can be applied to.

[0262]

The transistor, the memory device, the CPU, and the like described in the above embodiments can be applied to a variety of electronic devices (including game machines). Examples of the electronic devices include display devices of televisions, monitors, and the like, lighting devices, personal computers, word processors, image reproduction devices, portable audio players, radios, tape recorders, stereos, phones, cordless phones, mobile phones, car phones, transceivers, wireless devices, game machines, calculators, portable information terminals, electronic notebooks, e-book readers, electronic translators, audio input devices, video cameras, digital still cameras, electric shavers, IC chips, high-frequency heating appliances such as microwave ovens, electric rice cookers, electric washing machines, electric vacuum cleaners, air-conditioning systems such as air conditioners, dishwashers, dish dryers, clothes dryers, futon dryers, electric refrigerators, electric freezers, electric refrigerator-freezers, freezers for preserving DNA, radiation counters, and medical equipment such as dialyzers and X-ray diagnostic equipment. In addition, the examples of the electronic devices include alarm devices such as smoke detectors, heat detectors, gas alarm devices, and security alarm devices. Furthermore, the examples of the electronic devices also include industrial equipment such as guide lights, traffic lights, belt conveyors, elevators, escalators, industrial robots, and power storage systems. In addition, moving objects and the like driven by fuel engines and electric motors using power from non-aqueous secondary batteries are also included in the category of electronic devices. Examples of the moving objects include electric vehicles (EV), hybrid electric vehicles (HEV) which include both an internal-combustion engine

and a motor, plug-in hybrid electric vehicles (PHEV), tracked vehicles in which caterpillar tracks are substituted for wheels of these vehicles, motorized bicycles including motor-assisted bicycles, motorcycles, electric wheelchairs, golf carts, boats or ships, submarines, helicopters, aircrafts, rockets, artificial satellites, space probes, planetary probes, and spacecrafts. Some specific examples of these electronic devices are illustrated in FIGS. 12A to 12C.

[0263]

In a television set 8000 illustrated in FIG. 12A, a display portion 8002 is incorporated in a housing 8001. The display portion 8002 can display an image and a speaker portion 8003 can output sound. Any of the transistors described in the above embodiments can be used in a pixel or a driver circuit for operating the display portion 8002 incorporated in the housing 8001.

[0264]

A semiconductor display device such as a liquid crystal display device, a light-emitting device in which a light-emitting element such as an organic EL element is provided in each pixel, an electrophoretic display device, a digital micromirror device (DMD), or a plasma display panel (PDP) can be used for the display portion 8002.

[0265]

The television set 8000 may be provided with a receiver, a modem, and the like. With the receiver, a general television broadcast can be received. Furthermore, when the television set 8000 is connected to a communication network by wired or wireless connection via the modem, one-way (from a transmitter to a receiver) or two-way (between a transmitter and a receiver, between receivers, or the like) data communication can be performed.

[0266]

In addition, the television set 8000 may include a CPU 8004 for performing information communication or a memory. Any of the transistors, the memory device, and the CPU described in the above embodiments is used for the CPU 8004 or the memory, whereby power consumption can be reduced.

[0267]

An alarm device 8100 illustrated in FIG. 12A is a residential fire alarm, which includes a sensor portion 8102 for smoke or heat and a microcomputer 8101. Note that

the microcomputer 8101 includes the transistor, the memory device, or the CPU described in any of the above embodiments.

[0268]

An air conditioner which includes an indoor unit 8200 and an outdoor unit 8204 illustrated in FIG. 12A is an example of an electronic device including the transistor, the memory device, the CPU, or the like described in any of the above embodiments. Specifically, the indoor unit 8200 includes a housing 8201, an air outlet 8202, a CPU 8203, and the like. Although the CPU 8203 is provided in the indoor unit 8200 in FIG. 12A, the CPU 8203 may be provided in the outdoor unit 8204. Alternatively, the CPU 8203 may be provided in both the indoor unit 8200 and the outdoor unit 8204. By using the transistor described in any of the above embodiments for the CPU in the air conditioner, a reduction in the power consumption of the air conditioner can be achieved.

[0269]

An electronic refrigerator-freezer 8300 illustrated in FIG. 12A is an example of an electronic device including the transistor, the memory device, the CPU, or the like described in any of the above embodiments. Specifically, the electric refrigerator-freezer 8300 includes a housing 8301, a door for a refrigerator 8302, a door for a freezer 8303, a CPU 8304, and the like. In FIG. 12A, the CPU 8304 is provided in the housing 8301. When the transistor described in any of the above embodiments is used in the CPU 8304 of the electric refrigerator-freezer 8300, a reduction in the power consumption of the electric refrigerator-freezer 8300 can be achieved.

[0270]

FIGS. 12B and 12C illustrate an example of an electric vehicle which is an example of an electronic device. An electric vehicle 9700 is equipped with a secondary battery 9701. The output of the electric power of the secondary battery 9701 is adjusted by a circuit 9702 and the electric power is supplied to a driving device 9703. The circuit 9702 is controlled by a processing unit 9704 including a ROM, a RAM, a CPU, or the like which is not illustrated. When any of the transistors described in the above embodiments is used for the CPU in the electric vehicle 9700, a reduction in the power consumption of the electric vehicle 9700 can be achieved.

[0271]

The driving device 9703 includes a DC motor or an AC motor either alone or in

combination with an internal-combustion engine. The processing unit 9704 outputs a control signal to the circuit 9702 in accordance with input data such as data of operation (e.g., acceleration, deceleration, or stop) by a driver or data during driving (e.g., data on an upgrade or a downgrade, or data on a load on a driving wheel) of the electric vehicle 9700. The circuit 9702 adjusts the electric energy supplied from the secondary battery 9701 in accordance with the control signal of the processing unit 9704 to control the output of the driving device 9703. In the case where the AC motor is mounted, although not illustrated, an inverter which converts a direct current into an alternate current is also incorporated.

[0272]

This embodiment can be combined with any of the other embodiments in this specification as appropriate.

EXPLANATION OF REFERENCE

[0273]

200: substrate 202: gate electrode layer 204: insulating layer 205: insulating layer 205a: insulating film 206: insulating layer 207: oxide layer 208: oxide semiconductor layer 209: oxide layer 210a: source electrode layer 210b: drain electrode layer 212: insulating layer 214: insulating layer 214a: insulating film 216: gate electrode layer 260: transistor 270: transistor 280: transistor 602: photodiode 640: transistor 656: transistor 658: photodiode reset signal line 659: gate signal line 671: photosensor output signal line 672: photosensor reference signal line 700: memory element 701: circuit 702: circuit 703: switch 704: switch 706: logic element 707: capacitor 708: capacitor 709: transistor 710: transistor 713: transistor 714: transistor 720: circuit 1189: ROM interface 1190: substrate 1191: ALU 1192: ALU controller 1193: instruction decoder 1194: interrupt controller 1195: timing controller 1196: register 1197: register controller 1198: bus interface 1199: ROM 2200: transistor 3001: wiring 3002: wiring 3003: wiring 3004: wiring 3005: wiring 3200: transistor 3300: transistor 3400: capacitor 8000: television set 8001: housing 8002: display portion 8003: speaker portion 8004: CPU 8100: alarm device 8101: microcomputer 8102: sensor portion 8200: indoor unit 8201: housing 8203: CPU 8204: outdoor unit 8300: electric refrigerator-freezer 8301: housing 8302: door for a refrigerator 8303: door for a

freezer 8304: CPU 9700: electric vehicle 9701: secondary battery 9702: circuit 9703: driving device 9704: processing unit

This application is based on Japanese Patent Application serial No. 2013-106331 filed with Japan Patent Office on May 20, 2013, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

a first layer over a substrate;

a second layer over the first layer;

a third layer in contact with a top surface and a side surface of the second layer and with a side surface of the first layer;

a gate electrode layer over the third layer with a gate insulating layer interposed therebetween; and

an aluminum oxide film over the gate electrode layer,

wherein each of the first layer, the second layer and the third layer contains indium, gallium and zinc.

2. The semiconductor device according to claim 1, wherein each of the first layer and the third layer has a higher proportion of gallium in atomic ratio than the second layer.

3. The semiconductor device according to claim 1, wherein the second layer is thicker than the first layer and the third layer.

4. The semiconductor device according to claim 1, further comprising another gate electrode layer below the first layer.

5. The semiconductor device according to claim 1, further comprising a source electrode layer and a drain electrode layer in contact with another side surface of the second layer.

6. The semiconductor device according to claim 1, wherein the semiconductor device is incorporated in one selected from the group consisting of a television set, an alarm device, an air conditioner, a refrigerator, and an electric vehicle.

7. A semiconductor device comprising:

a first layer over a substrate;

a second layer over the first layer;

a third layer in contact with a top surface and a side surface of the second layer

and with a side surface of the first layer;

a gate electrode layer over the third layer with a gate insulating layer interposed therebetween; and

an aluminum oxide film over the gate electrode layer,

wherein each of the first layer, the second layer and the third layer contains indium, gallium and zinc, and

wherein the gate electrode layer covers the top surface and the side surface of the second layer.

8. The semiconductor device according to claim 7, wherein each of the first layer and the third layer has a higher proportion of gallium in atomic ratio than the second layer.

9. The semiconductor device according to claim 7, wherein the second layer is thicker than the first layer and the third layer.

10. The semiconductor device according to claim 7, further comprising another gate electrode layer below the first layer.

11. The semiconductor device according to claim 7, further comprising a source electrode layer and a drain electrode layer in contact with another side surface of the second layer.

12. The semiconductor device according to claim 7, wherein the semiconductor device is incorporated in one selected from the group consisting of a television set, an alarm device, an air conditioner, a refrigerator, and an electric vehicle.

13. The semiconductor device according to claim 1, wherein the aluminum oxide film contains excess oxygen.

14. The semiconductor device according to claim 7, wherein the aluminum oxide film contains excess oxygen.

15. A semiconductor device comprising:

a first layer over a substrate;

a second layer over the first layer;

a third layer over the second layer;

a gate electrode layer over the third layer with a gate insulating layer interposed therebetween;

an aluminum oxide film over the gate electrode layer; and

a source electrode layer and a drain electrode layer partly interposed between the second layer and the third layer,

wherein each of the first layer, the second layer and the third layer contains indium, gallium and zinc.

16. The semiconductor device according to claim 15, wherein each of the first layer and the third layer has a higher proportion of gallium in atomic ratio than the second layer.

17. The semiconductor device according to claim 15, wherein the second layer is thicker than the first layer and the third layer.

18. The semiconductor device according to claim 15, further comprising another gate electrode layer below the first layer.

19. The semiconductor device according to claim 15, wherein the semiconductor device is incorporated in one selected from the group consisting of a television set, an alarm device, an air conditioner, a refrigerator, and an electric vehicle.

20. The semiconductor device according to claim 15, wherein the aluminum oxide film contains excess oxygen.

21. A semiconductor device comprising:

a first layer over a substrate;

a second layer over the first layer;

a third layer over the second layer;

a gate electrode layer over the third layer with a gate insulating layer interposed therebetween;

an aluminum oxide film over the gate electrode layer; and

a source electrode layer and a drain electrode layer partly interposed between

the second layer and the third layer,

wherein each of the first layer, the second layer and the third layer contains indium, gallium and zinc, and

wherein the gate electrode layer covers the top surface and the side surface of the second layer.

22. The semiconductor device according to claim 21, wherein each of the first layer and the third layer has a higher proportion of gallium in atomic ratio than the second layer.

23. The semiconductor device according to claim 21, wherein the second layer is thicker than the first layer and the third layer.

24. The semiconductor device according to claim 21, further comprising another gate electrode layer below the first layer.

25. The semiconductor device according to claim 21, wherein the semiconductor device is incorporated in one selected from the group consisting of a television set, an alarm device, an air conditioner, a refrigerator, and an electric vehicle.

26. The semiconductor device according to claim 21, wherein the aluminum oxide film contains excess oxygen.