What Is Claimed Is:

1. A three-dimensional semiconductor device, comprising:

a conductive layer disposed on a substrate and including a first conductivity-type impurity;

an insulating base layer disposed on the conductive layer;

a stack structure including a lower insulating film disposed on the insulating base layer, and a plurality of gate electrodes and a plurality of mold insulating layers alternately stacked on the lower insulating film, wherein the insulating base layer includes a high dielectric material;

a vertical structure including a vertical channel layer penetrating through the stack structure and a vertical insulating layer disposed between the vertical channel layer and the plurality of gate electrodes, the vertical structure having an extended area extending in a width direction in the insulating base layer; and

an isolation structure penetrating through the stack structure, the insulating base layer and the conductive layer, and extending in a direction parallel to an upper surface of the substrate,

wherein the conductive layer is in contact with a bottom surface of the vertical channel layer and has an extension portion extending from the bottom surface of the vertical channel layer along a side surface of the vertical channel layer in the extended area of the vertical structure.

2. The three-dimensional semiconductor device of claim 1, wherein a portion of the vertical channel layer adjacent to the extension portion has a higher concentration of the first conductivity-type impurity than a portion of the vertical

channel layer adjacent to the plurality of gate electrodes.

3. The three-dimensional semiconductor device of claim 1 or claim 2, wherein a portion of the vertical channel layer adjacent to a lowermost gate electrode of the plurality of gate electrodes has a higher concentration of the first conductivity-type impurity than a portion of the vertical channel layer adjacent to an uppermost gate electrode of the plurality of gate electrodes.

4. The three-dimensional semiconductor device any one of claims 1 to 3, wherein the conductive layer comprises polysilicon having an n-type impurity.

5. The three-dimensional semiconductor device of any one of claims 1 to 4, wherein the extended area each have a convex side.

6. The three-dimensional semiconductor device of any one of claims 1 to 5, wherein the extension portion extends to an upper half of the extended area.

7. The three-dimensional semiconductor device of any one of claims 1 to 6, wherein an upper end of the extension portion is located below the lower insulating film.

8. The three-dimensional semiconductor device of any one of claims 1 to 6, wherein an upper end of the extension portion is connected to a lower end of the vertical insulating layer.

9. The three-dimensional semiconductor device of any one of claims 1 to 8, wherein the insulating base layer has a support region in contact with the substrate.

10. The three-dimensional semiconductor device of any one of claims 1 to 9, wherein deviations of a maximum width of the extended area and a thickness of the insulating base layer are within a range of ± 30%.

11. The three-dimensional semiconductor device of claim 10, wherein the thickness of the insulating base layer is 30 nm to 50 nm, and the maximum width of the extended area is 30 nm to 60 nm.

12. The three-dimensional semiconductor device of any one of claims 1 to 11, wherein the insulating base layer comprises aluminum oxide (Al_2O_3), tantalum oxide (Ta_2O_3), titanium oxide (TiO_2), yttrium oxide (Y_2O_3), zirconium oxide (ZrO_2), zirconium silicon oxide ($ZrSi_xO_y$), hafnium oxide (HfO_2), hafnium silicon oxide ($HfSi_xO_y$), lanthanum oxide (La_2O_3), lanthanum aluminum oxide ($LaAl_xO_y$), lanthanum hafnium oxide ($LaHf_xO_y$), hafnium aluminum oxide ($HfAl_xO_y$), or praseodymium oxide (Pr_2O_3).

13. The three-dimensional semiconductor device of any one of claims 1 to 12, wherein the vertical structure further comprises an insulating core disposed in a direction perpendicular to the upper surface of the substrate in the vertical channel layer,

wherein the insulating core has an extended area extending in the width direction in the insulating base layer.

14. The three-dimensional semiconductor device of any one of claims 1 to 13, wherein the isolation structure is in contact with the substrate.

15. A three-dimensional semiconductor device, comprising:

a conductive layer disposed on a substrate;

an insulating base layer disposed on the conductive layer and having a plurality of support regions in contact with the substrate;

a stack structure having a plurality of gate electrodes and a plurality of mold insulating layers alternately disposed on the insulating base layer;

a vertical structure including a vertical channel layer penetrating through the stack structure, and a vertical insulating layer disposed between the vertical channel layer and the plurality of gate electrodes, the vertical structure having a first extended area extending in a width direction in the insulating base layer and having a convex side; and

an isolation structure penetrating through the stack structure, the insulating base layer and the conductive layer, extending in a first direction parallel to an upper surface of the substrate, and having a second extended area extending in a second direction intersecting the first direction and parallel to the upper surface of the substrate in the insulating base layer,

wherein the conductive layer is in contact with a bottom surface of the vertical channel layer and has an extension portion extending from the bottom surface of the vertical channel layer along a side surface of the vertical channel layer in the first extended area of the vertical structure, and an upper end of the extension portion is connected to a lower end of the vertical insulating layer on the side surface of the vertical channel layer in the first extended area of the vertical structure.

16. The three-dimensional semiconductor device of claim 15, wherein the insulating base layer comprises a high dielectric material.

17. The three-dimensional semiconductor device of claim 15 or claim 16, wherein the conductive layer and the vertical channel layer include polysilicon.

18. The three-dimensional semiconductor device of any one of claims 15 to 17, wherein a lower end of the vertical channel layer is located below a lower surface of the insulating base layer.

19. A three-dimensional semiconductor device, comprising:

a conductive layer disposed on a substrate and including a first conductivity-type impurity;

an insulating layer disposed on the conductive layer;

a stack structure including a lower insulating film disposed on the insulating layer, and a plurality of gate electrodes and a plurality of mold insulating layers alternately stacked on the lower insulating film, wherein the insulating layer includes a high dielectric material;

a vertical structure including a vertical channel layer penetrating through the stack structure and a vertical insulating layer disposed between the vertical channel layer and the plurality of gate electrodes, the vertical structure having a first area in the insulating layer, wherein a side of the first area in the insulating layer overlaps a lowermost gate electrode of the gate electrodes in a direction perpendicular to an upper surface of the substrate, wherein the conductive layer is in contact with a bottom surface

of the vertical channel layer; and

a conductive film extending from the conductive layer, extending from the bottom surface of the vertical channel layer along a side surface of the vertical channel layer, and covering at least a portion of the vertical channel layer in the first area, wherein the conductive film includes the first conductivity-type impurity.