Method for connecting an integrated circuit to a substrate and corresponding circuit arrangement

The present invention relates to a method for connecting an integrated circuit to a substrate and a corresponding circuit arrangement.

Although applicable in principle to any desired integrated circuits, the present invention and also the problem area on which it is based are explained with regard to chips with integrated circuits in silicon technology.

Known CSP (Chip Size Package) or WLP (Wafer Level Package) solutions for connecting an integrated circuit to a substrate have reliability problems in the event of temperature changes particularly in the case of large circuit arrangements, to be precise particularly in the context of ever decreasing distances between substrate and packaged chip. The different thermal expansion coefficients of packaged circuit arrangement and substrate give rise to different linear expansions of the two components during the temperature changes.

In the case of chip size packages and wafer level packages, essentially two types of connecting structures between the chip and the substrate have been disclosed heretofore.

The first customary solution for connecting an integrated circuit to a substrate is the use of ball grid arrays with rigid solder balls or bumps for mechanical connection with the additional use of an underfill in order to increase the stability. In the case of this solution, the mismatch of the thermal properties of the chip and of the substrate, in particular of the thermal expansion coefficient, leads

to major reliability risks. The solder balls may be sheared away in the event of temperature changes. This considerably restricts the reliability, particularly in the case of large chips.

In order to prevent such undesirable defects, various types of interposer layers have been developed, which serve as stress buffers between the chip having a low thermal expansion coefficient and the substrate having a high thermal expansion coefficient. Such solutions increase the height of the construction, the number of connections and at least the costs.

Figure 4 shows a diagrammatic view of a part of an interposer-type circuit arrangement for elucidating the problem area on which the invention is based.

In figure 4, reference symbol 100 designates a circuit substrate, for example in the form of a module board. Reference symbol 1a designates in combinative fashion a package of an integrated circuit, which is a chip 5 in the present case. The chip 5 has contact pads 6, at which electrical connections of the circuit situated therein are routed toward the outside. An interposer 15 is applied on the front side VS of the chip 5 by means of an adhesive layer 10, which interposer has, in the center, a feedthrough through which leads 7 are routed in a manner sealed by an adhesive 8, which are connected to the contact pads 6 at one of their ends and to connection regions 140 at their other end, the latter being provided on the connection side AS of the package 1a. The connection regions 140 are connected to a rewiring having a plurality of connection regions 50 which are provided for connection to a corresponding number of connection regions 110 on the circuit substrate 100.

This mechanical and electrical connection is realized by corresponding solder balls 30 between the connection regions 110, 150, an underfill agent 50 in the form of an adhesive additionally being introduced between circuit substrate 100 and interposer 15.

An encapsulation 20, for example made of nontransparent epoxy resin, is provided on the rear side of the chip 5. The broken lines in Figure 4 designate a flexure influence V on account of thermal mismatches, which has the effect that, in the case of a geometry of this type, the edge regions, in particular, are subject to a high stress ST. This stress ST is ultimately the reason why the outer solder balls are often sheared away or torn away in the event of temperature changes.

Figure 5 shows a diagrammatic view of a part of a chip-size-type circuit arrangement for elucidating the problem area on which the invention is based.

In contrast to the arrangement in accordance with Figure 4, no interposer is provided in the case of the arrangement in accordance with figure 5. Rather, a dielectric layer 25 is situated there on the front side VS of the chip 5, on which dielectric layer there are provided connection regions 150 connected to the contact pads 6 via the rewiring. Analogously to the example according to Figure 4, solder balls 30 are provided, which provide a mechanical and electrical connection between the package 1b with the chip 5 and the circuit substrate 100. In order to provide [sic] an undesirable flowing away of solder, a solder resist layer of 120 is furthermore provided on the connection side AS, which layer has the effect that the solder balls 30 are maintained at the locations provided and do not flow away. In this example, too, an underfill layer 50 in the form of an adhesive layer is provided for stabilization.

A further solution for connecting an integrated circuit to a substrate is the use of elastic elevations, which is disclosed in WO 00/79589 A1. The latter discloses an electronic component having flexible raised portions made of an insulating material on a surface, an electrical contact being arranged on the flexible elevation and a conduction path being arranged on the surface or in the interior of the flexible elevation between the electrical contact and the electronic circuit. The advantage of this solution is a smaller construction height, a higher reliability and lower costs. In this connection, it is known to solder or adhesively bond the elastic contact elements onto the substrate.

One disadvantage of this solution is that the dissipation of heat from the integrated circuit is significantly poorer in the case of flexible plastic contact elements than in the case of solder balls. A further disadvantage resides in poorer mechanical fixing.

One object of the present invention is to provide a simple and cost-effective method for connecting an integrated circuit to a substrate and a corresponding circuit arrangement which remains largely uninfluenced by thermal mismatch but nevertheless has good heat dissipation properties.

According to this invention, this object is achieved by means of the method for connecting an integrated circuit to a substrate according to Claim 1 and the corresponding circuit arrangement according to Claim 11.

The idea on which the present invention is based resides in configuring the elevated contact regions in

such a way that the first group of contact regions form a rigid connection and the second group of contact regions form an elastic connection between the package and the substrate. By virtue of suitable arrangement, it is thus possible, on the one hand, to elastically compensate for the thermal mismatch, but on the other hand to maintain a good dissipation of heat and fixed mechanical linking. In this connection, it should be mentioned that the contact regions need not necessarily have an electrical contact function, but rather may at least partly have only a thermal/mechanical function.

It was found in the conception of the present invention that the effect of different linear expansions is greater, the greater the distance from a neutral point of the circuit arrangement. Starting from a specific distance from such a neutral point, the stress that arises during temperature changes can no longer be cushioned by the package, and the weakest components - generally the solder balls - are destroyed, since the solder connection is not very elastic and tears away above a specific shear force.

The specific location of a neutral point depends on the geometrical construction of the packaged integrated circuit and the substrate.

Advantageous developments and improvements of the respective subject matter of the invention are found in the subclaims.

In accordance with one preferred development, the first group of contact regions is arranged in a near region surrounding a point of the connection side, and the second group of contact regions is arranged outside in a far region surrounding the near region.

In accordance with a further preferred development, the point lies approximately in the center of an extent in a predetermined direction of the package.

In accordance with a further preferred development, the contact regions of the first group comprise solder elements and the contact regions of the second group comprise plastic elements.

In accordance with a further preferred development, the plastic elements comprise electrically conductive polymer and/or adhesive and/or silicone.

In accordance with a further preferred development, the plastic elements are provided with a solderable metal coating at their side to be connected.

In accordance with a further preferred development, the plastic elements comprise electrically nonconductive polymer and/or adhesive and/or silicone and are provided with a metallic interconnect at their side to be connected, said interconnect being electrically connected to the integrated circuit.

In accordance with a further preferred development, the package has an interposer on the front side of the integrated circuit, the connection regions of the package being provided on that side of said interposer which is remote from the integrated circuit.

In accordance with a further preferred development, the package has an insulating layer on the front side of the integrated circuit, the connection regions of the package being provided on that side of said insulating layer which is remote from the integrated circuit.

In accordance with a further preferred development, the package is provided at least on the rear side of the integrated circuit an encapsulation [sic].

Exemplary embodiments of the invention is [sic] illustrated in the drawings and explained in more detail in the description below.

In the figures:

Figures 1a,b show a diagrammatic view of a part of a circuit arrangement in accordance with a first embodiment of the present invention;

Figure 2 shows a diagrammatic view of a part of a circuit arrangement in accordance with a second embodiment of the present invention;

Figure 3 shows a diagrammatic view of a part of a circuit arrangement in accordance with a third embodiment of the present invention;

Figure 4 shows a diagrammatic view of a part of an interposer-type circuit arrangement for elucidating the problem area on which the invention is based; and

Figure 5 shows a diagrammatic view of a part of a chip-size-type circuit arrangement for elucidating the problem area on which the invention is based.

In the figures, identical reference symbols designate identical or functionally identical constituent parts.

Figures 1a, b show a diagrammatic view of a part of a circuit arrangement in accordance with a first embodiment of the present invention.

In Figure 1a, reference symbol 1a' designates a modified package which differs from the example in Figure 4 by the fact that, on the connection side AS, solder balls 30 are provided only on connection areas 150 located within a specific near region IR with regard to a neutral point NP.

Said neutral point NP is, for the x direction, the point at which the thermal mismatch of the different components has the least influence. In other words, no stresses or only very small stresses occur here. These stresses increase with increasing distance from the neutral point NP. Within the near region IR, said stresses are restricted to a magnitude which does not lead to destructive alterations in the case of the desired temperature change range. Accordingly, contact regions for connection to the circuit substrate 100 are solder balls 30 there.

By contrast, the stresses in the far region OR are so large that they cannot be endured by solder balls 30. Correspondingly, in this embodiment, elastic conductive plastic elements 35 are provided there at the corresponding connection areas 150, which plastic elements have a metalization region 38 of a solderable metal at their connecting side, i.e. the side for connection to the circuit substrate 100.

With reference to Figure 1b, the connection to the circuit substrate 100 is effected in the region of the solder balls 30 in a customary manner and in the region of the plastic elements 35 with the aid of additional solder 39, which, in this example, is applied to the

corresponding connection areas 110 of the circuit substrate.

The resulting connection between the package 1a' with the chip 5 and the circuit substrate 100 is significantly less susceptible to the stresses ST which arise on account of the thermal mismatches. This is because said elastic plastic elements 35 can be compressed, dilated and distorted to a significantly greater extent.

Although all the contact regions 30, 35 have an electrical function in this exemplary embodiment, this is not absolutely necessary; it is possible, by way of example, to provide additional contact regions 30, 35 having only a mechanical or thermal/mechanical function.

Figure 2 shows a diagrammatic view of a part of a circuit arrangement in accordance with a second embodiment of the present invention.

The embodiment in accordance with Figure 2 corresponds to the known circuit arrangement explained above with reference to Figure 5. Here, too, the contact elements have been retained in the form of solder balls 30 in the near region IR of the neutral point NP. By contrast, elastic plastic elements made of a nonconductive material have been provided in the connection regions 150' located in the far region OR. The connection regions 150' are not conductive here, but rather serve only for mechanical connection.

In order to produce a conductive connection to the rewiring which is connected to the contact pads 6 of the chip 5, interconnects 150', have been routed to the surface of the elastic plastic elements 35. Consequently, as in the first embodiment mentioned

above, the package 1b' with the chip 5 can be adhesively bonded or soldered onto the circuit substrate 100, and it is possible to achieve the same advantages as in the first embodiment.

Figure 3 shows a diagrammatic view of a part of a circuit arrangement in accordance with a third embodiment of the present invention.

The embodiment in accordance with Figure 3 differs from the embodiment in accordance with Figure 2 only insofar as the region of the rewiring is lengthened over the side edges of the chip, which is usually also referred to as fan-out.

Although the present invention has been described above on the basis of preferred exemplary embodiments, it is not restricted thereto, but rather can be modified in diverse ways.

In particular, the present invention can be employed not only for chips but also for hybrids, wafers or other integrated circuits. Moreover, the invention is not restricted to the materials specified.

List of reference symbols

100	Circuit substrate
20	Encapsulation
110,150, 140,150'	Connection regions
7	Lines
8	Adhesive composition
AS	Connection side
VS	Front side
RS	Rear side
5	Chip
10	Adhesive layer
15	Interposer
30	Solder balls
35	Plastic elements
6	Contact pads
38	Metalization
IR	Near region
OR	Far region
1a,1b, 1a',1b', 1c'	Package including chip
NP	Neutral point
ST	Stress
V	Flexure effect
39	Solder
150''	Interconnect
25	Dielectric
120 s	Solder resist layer

Patent Claims

1. Method for connecting an integrated circuit (5), in particular from a chip or a wafer or a hybrid, to a substrate (100), which has the following steps:

provision of a package (1a'; 1b'; 1c') for the integrated circuit, which has a connection side (AS), on which there are provided a plurality of connection regions (150; 150, 150') for connection to the substrate (100);

provision of a corresponding plurality of connection regions (110) on the substrate (100);

provision of elevated contact regions (30; 35) on the connection regions (150; 150, 150') of the package (1a'; 1b'; 1c') and/or the connection regions (110) of the substrate (100);

the elevated contact regions (30; 35) comprising a first group of contact regions (30) and a second group of contact regions (35);

creation of a connection of the package (1a'; 1b'; 1c') to the substrate (100) via the elevated contact regions (30; 35);

the elevated contact regions (30; 35) being configured in such a way that the first group of contact regions (30) form a rigid connection and the second group of contact regions (35) form an elastic connection between the package (1a'; 1b'; 1c') and the substrate (100).

2. Method according to Claim 1,
characterized
in that the first group of contact regions (30) is arranged in a near region (IR) surrounding a point (NP)

of the connection side (AS), and the second group of contact regions (35) is arranged outside in a far region (OR) surrounding the near region (IR).

3. Method according to Claim 2, characterized in that the point (NP) lies approximately in the center of an extent in a predetermined direction (x) of the package (1a'; 1b'; 1c').

4. Method according to Claims 1, 2 or 3, characterized in that the contact regions (30) of the first group comprise solder elements and the contact regions (35) of the second group comprise plastic elements.

5. Method according to Claim 4, characterized in that the plastic elements comprise electrically conductive polymer and/or adhesive and/or silicone.

6. Method according to Claim 5, characterized in that the plastic elements are provided with a solderable metal coating (38) at their side to be connected.

7. Method according to Claim 4, characterized in that the plastic elements comprise electrically nonconductive polymer and/or adhesive and/or silicone and are provided with a metallic interconnect (150'') at their side to be connected, said interconnect being electrically connected to the integrated circuit (5).

8. Method according to one of the preceding claims, characterized

in that the package (1a') has an interposer (15) on the front side (VS) of the integrated circuit (5), the connection regions (150) of the package (1a') being provided on that side of said interposer which is remote from the integrated circuit (5).

9. Method according to one of the preceding Claims 1 to 7,
characterized
in that the package (1b'; 1c') has an insulating layer (25) on the front side (VS) of the integrated circuit (5), the connection regions (150) of the package (1b'; 1c') being provided on on [sic] that side of said insulating layer which is remote from the integrated circuit (5).

10. Method according to one of the preceding claims,
characterized
in that the package (1b'; 1c') is provided at least on the rear side (VS) [sic] of the integrated circuit (5) an encapsulation (20) [sic].

11. Circuit arrangement having a connection of an integrated circuit (5), in particular from a chip or a wafer or a hybrid, to a substrate (100), having:

a package (1a'; 1b'; 1c') of the integrated circuit, which has a connection side (AS), on which there are provided a plurality of connection regions (150; 150, 150') for connection to the substrate (100);

a corresponding plurality of connection regions (110), on the substrate (100); and

elevated contact regions (30; 35); which connect the connection regions (150; 150, 150') of the package (1a'; 1b'; 1c') to the connection regions (110) of the substrate (100);

the elevated contact regions (30; 35) comprising a first group of contact regions (30) and a second group of contact regions (35), which are configured in such a way that the first group of contact regions (30) form a rigid connection and the second group of contact regions (35) form an elastic connection between the package (1a'; 1b'; 1c') and the substrate (100).

12. Method according to Claim 11,
characterized
in that the first group of contact regions (30) is arranged in a near region (IR) surrounding a point (NP) of the connection side (AS), and the second group of contact regions (35) is arranged outside in a far region (OR) surrounding the near region (IR).

13. Method according to Claim 12,
characterized
in that the point (NP) lies approximately in the center of an extent in a predetermined direction (x) of the package (1a'; 1b'; 1c').

14. Method according to Claims 11, 12 or 13,
characterized
in that the contact regions (30) of the first group comprise solder elements and the contact regions (35) of the second group comprise plastic elements.

15. Method according to Claim 14,
characterized
in that the plastic elements comprise electrically conductive polymer and/or adhesive and/or silicone.

16. Method according to Claim 15,
characterized

in that the plastic elements are provided with a solderable metal coating (38) at their side to be connected.

17. Method according to Claim 14,
characterized
in that the plastic elements comprise electrically nonconductive polymer and/or adhesive and/or silicone and are provided with a metallic interconnect (150') at their side to be connected, said interconnect being electrically connected to the integrated circuit (5).

18. Method according to one of the preceding Claims 11 to 17,
characterized
in that the package (1a') has an interposer (15) on the front side (VS) of the integrated circuit (5), the connection regions (150) of the package (1a') being provided on that side of said interposer which is remote from the integrated circuit (5).

19. Method according to one of the preceding Claims 11 to 17,
characterized
in that the package (1b'; 1c') has an insulating layer (25) on the front side (VS) of the integrated circuit (5), the connection regions (150) of the package (1b'; 1c') being provided on that side of said insulating layer which is remote from the integrated circuit (5).

20. Method according to one of the preceding Claims 11 to 19,
characterized
in that the package (1b'; 1c') is provided at least on the rear side (VS) [sic] of the integrated circuit (5) an encapsulation (20) [sic].