

APPARATUS AND METHODS FOR CONTROLLING ION ENERGY DISTRIBUTION

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to apparatus and methods for plasma processing of a substrate, and specifically to apparatus and methods for controlling an ion energy distribution during plasma processing.

Description of the Related Art

[0002] During plasma processing of a substrate, ions play a key role for substrate surface treatment, etching, and deposition. Ions impinging the substrate surface can have a variety of energies which is described by an ion energy distribution function (IEDF). Control over the IEDF can be an important factor for various substrate processing schemes. Controlling the IEDF, however, remains a challenge. For example, when periodic alternating voltage is applied to electrode(s) of a chamber, a plasma sheath can develop above the substrate. The ions flowing towards the substrate are accelerated by the plasma sheath voltage which correlates with the voltage applied to the electrode. At the same time, ion current can charge the substrate and alter the substrate potential, which in turn affects the plasma sheath voltage such that the IEDF at the substrate surface is also affected, e.g., broadened. State-of-the-art methods to control the IEDF in such instances, and others, are based on inefficient iteration loops.

[0003] There is a need for new and improved methods for controlling the IEDF.

SUMMARY

[0004] Embodiments of the present disclosure generally relate to apparatus and methods for plasma processing of a substrate, and specifically to apparatus and methods for controlling an ion energy distribution during plasma processing.

[0005] In an embodiment, a method of controlling an ion energy distribution function (IEDF) is provided. The method includes introducing a voltage to an

electrode of a processing chamber by activating a main pulser, the main pulser coupled to an IEDF width control module, and measuring a current of the IEDF width control module and a voltage or a voltage derivative of the IEDF width control module. The method further includes calculating an ion current of the processing chamber and a capacitance of the processing chamber based on the current and the voltage or voltage derivative of the IEDF width control module. The method further includes determining a setpoint for a DC voltage of the main pulser, a setpoint for a voltage or a voltage derivative of the IEDF width control module, or both, and adjusting the DC voltage of the main pulser, the voltage or voltage derivative of the IEDF width control module, or both, to the determined setpoints to control the width of the IEDF.

[0006] In another embodiment, an apparatus for controlling an ion energy distribution is provided. The apparatus includes a substrate support that has a body having a substrate support portion having a substrate electrode embedded therein for applying a substrate voltage to a substrate. The body further includes an edge ring portion disposed adjacent to the substrate support portion, the edge ring portion having an edge ring electrode embedded therein for applying an edge ring voltage to an edge ring. The apparatus further includes a substrate voltage control circuit coupled to the substrate electrode and an edge ring voltage control circuit coupled to the edge ring electrode. The substrate electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the substrate, or the edge ring electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the edge ring, or a combination thereof. The substrate voltage control circuit, the edge ring voltage control circuit, or both comprises a main pulser coupled to a current return path, the current return path coupled to the power module and to a processing chamber, wherein the power module comprises a voltage source, a current source, or a combination thereof

[0007] In another embodiment, an apparatus for controlling an ion energy distribution is provided. The apparatus includes a substrate support that has a body having a substrate support portion having a substrate electrode embedded therein for applying a substrate voltage to a substrate. The body further includes an edge

ring portion disposed adjacent to the substrate support portion, the edge ring portion having an edge ring electrode embedded therein for applying an edge ring voltage to an edge ring. The apparatus further includes a substrate voltage control circuit coupled to the substrate electrode and an edge ring voltage control circuit coupled to the edge ring electrode. The substrate electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the substrate, or the edge ring electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the edge ring, or a combination thereof. The substrate voltage control circuit, the edge ring voltage control circuit, or both comprises a main pulser coupled to the power module, the power module coupled to a processing chamber, the power module comprising a voltage source, a current source, or a combination thereof.

[0008] In another embodiment, an apparatus for controlling an ion energy distribution is provided. The apparatus includes a substrate support that has a body having a substrate support portion having a substrate electrode embedded therein for applying a substrate voltage to a substrate. The body further includes an edge ring portion disposed adjacent to the substrate support portion, the edge ring portion having an edge ring electrode embedded therein for applying an edge ring voltage to an edge ring. The apparatus further includes a substrate voltage control circuit coupled to the substrate electrode and an edge ring voltage control circuit coupled to the edge ring electrode. The substrate electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the substrate, or the edge ring electrode is coupled to a power module configured to actively control an energy distribution function width of ions reaching the edge ring, or a combination thereof. The substrate voltage control circuit, the edge ring voltage control circuit, or both comprises a main pulser coupled to the power module, the power module coupled to a processing chamber, wherein the power module is in parallel with a substrate chucking and bias compensation module, and wherein the power module comprises a voltage source, a current source, or a combination thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0010] FIG. 1 is a schematic sectional view of an example processing chamber according to at least one embodiment of the present disclosure.

[0011] FIG. 2 is a schematic overview of an example processing chamber according to at least one embodiment of the present disclosure.

[0012] FIG. 3A is an exemplary graph showing three different bias voltage waveforms on a substrate according to at least one embodiment of the present disclosure.

[0013] FIG. 3B is an exemplary plot of IEDF versus ion energy for the three different bias voltage waveforms on a substrate shown in FIG. 3A according to at least one embodiment of the present disclosure.

[0014] FIG. 4A is a schematic overview of an example circuit according to at least one embodiment of the present disclosure.

[0015] FIG. 4B is a schematic overview of an example circuit according to at least one embodiment of the present disclosure.

[0016] FIG. 4C is a schematic overview of an example circuit according to at least one embodiment of the present disclosure.

[0017] FIG. 4D is a schematic overview of an example circuit according to at least one embodiment of the present disclosure.

[0018] FIG. 5A is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0019] FIG. 5B is an exemplary plot of V2 voltage waveform and substrate voltage waveform for the example schematic circuit diagram shown in FIG. 5A according to at least one embodiment of the present disclosure.

[0020] FIG. 5C is an example control circuit according to at least one embodiment of the present disclosure.

[0021] FIG. 5D is an example control circuit according to at least one embodiment of the present disclosure.

[0022] FIG. 5E shows exemplary saw-shaped voltage outputs according to at least one embodiment of the present disclosure.

[0023] FIG. 6A is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0024] FIG. 6B is an example control circuit according to at least one embodiment of the present disclosure.

[0025] FIG. 6C is an example control circuit according to at least one embodiment of the present disclosure.

[0026] FIG. 7A is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0027] FIG. 8 is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0028] FIG. 9 is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0029] FIG. 10 is an example schematic circuit diagram illustrating the IEDF width control circuit for driving the electrodes of the substrate support assembly according to at least one embodiment of the present disclosure.

[0030] FIG. 11 is a flowchart of a method of controlling IEDF width according to at least one embodiment of the present disclosure.

[0031] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0032] Embodiments of the present disclosure generally relate to apparatus and methods for plasma processing of a substrate, and specifically to apparatus and methods for controlling an ion energy distribution during plasma processing. The methods and apparatus, e.g., circuits, described herein enable control over the shape (e.g., narrow, or adjustable width) of the voltage waveform of a pulsed DC power supply. Embodiments described herein further enable, e.g., control over the ion energy distribution function (IEDF) including monoenergetic ion acceleration.

[0033] The IEDF is a parameter for etching high aspect ratio features. Typically, pulsed DC biases can provide a narrower IEDF as compared to sine wave RF biases according to the following mechanism. Because ions are accelerated by a less time-varying electric field within a pulsed DC period, the energy gained by the ions within the sheath also exhibits a lower time variance than when varying sine wave RF bias. As a result, ions accelerated by the pulsed DC bias have a narrower IEDF than sine wave RF bias. However, an ion current from the bulk plasma to the substrate distorts the voltage waveform at the substrate and broadens the ion energy distribution. Methods and apparatus described herein can, e.g., compensate this ion current and actively control the width of the ion energy distribution.

[0034] Conventional methods and apparatus use an iteration control loop to control the width of the ion energy distribution. Before convergence of the control algorithm, estimation of the plasma parameters (e.g., ion current, sheath thickness,

and IEDF width) are inaccurate. Moreover, controlling the width of the IEDF by using iterations is slow and can result in non-convergence of the control algorithm.

[0035] In contrast, the methods and apparatus described herein utilize one loop, without iteration, to determine the ion current and the compensation current to achieve a given IEDF width. Accordingly, the methods and apparatus described herein reach a desired state of the IEDF, e.g., a narrow IEDF, faster than the state-of-the-art. This is due to, e.g., not using an iteration in determining the solution of the compensation current.

[0036] Briefly, and in some embodiments, a substrate support includes a body, the body including a substrate support portion and/or an edge ring portion. A substrate electrode is embedded in the substrate support portion for applying a substrate voltage to a substrate. A substrate voltage control circuit is coupled to the substrate electrode. The edge ring portion includes an edge ring electrode embedded therein for applying an edge ring voltage to an edge ring. An edge ring voltage control circuit is coupled to the edge ring electrode. At least one shaped DC pulse source is coupled to the substrate voltage control circuit and/or the edge ring voltage control circuit. The substrate voltage circuit and/or the edge ring voltage control circuit is tunable. Adjustment of the voltage amplitude via, e.g., tuning the substrate voltage control circuit and/or the edge ring voltage control circuit results in adjustment and control of the ion energy distribution.

[0037] In some embodiments, a control circuit of the IEDF width is coupled to the substrate support. The control circuit of the IEDF width can be integrated inside a main pulsed DC power supply, or as a separate module, or as an integrated module with a bias compensation module.

Example Processing System Configurations

[0038] FIG. 1 is a schematic sectional view of a processing chamber 100 according to at least one embodiment of the present disclosure. The processing chamber 100 is configured to practice the schemes described herein. In this embodiment, the processing chamber is a plasma processing chamber, such as a reactive ion etch (RIE) plasma chamber. In some other embodiments, the processing chamber is a plasma-enhanced deposition chamber, for example a

plasma-enhanced chemical vapor deposition (PECVD) chamber, a plasma enhanced physical vapor deposition (PEPVD) chamber, or a plasma-enhanced atomic layer deposition (PEALD) chamber. In some other embodiments, the processing chamber is a plasma treatment chamber, or a plasma based ion implant chamber, for example a plasma doping (PLAD) chamber.

[0039] The processing chamber 100 includes a chamber body 101 and a lid 102 disposed thereon that together define an internal volume 124. The chamber body 101 is typically coupled to an electrical ground 103. A substrate support assembly 104 is disposed within the inner volume to support a substrate 105 thereon during processing. An edge ring 106 is positioned on the substrate support assembly 104 and surrounds the periphery of the substrate 105. The processing chamber 100 also includes an inductively coupled plasma apparatus 107 for generating a plasma of reactive species within the processing chamber 100, and a controller 108 adapted to control systems and subsystems of the processing chamber 100. In some embodiments, the inductively coupled plasma apparatus 107 can be replaced by a grounded shower head and RF power is delivered from an electrode underneath the substrate to generate capacitively coupled plasma.

[0040] The substrate support assembly 104 is disposed in the internal volume 124. The substrate support assembly 104 generally includes a substrate support 152. The substrate support 152 includes an electrostatic chuck 150 comprising a substrate support portion 154 configured to underlay and support the substrate 105 to be processed and an edge ring portion 156 configured to support an edge ring 106. The substrate support assembly 104 can additionally include a heater assembly 169. The substrate support assembly 104 can also include a cooling base 131. The cooling base 131 can alternately be separate from the substrate support assembly 104. The substrate support assembly 104 can be removably coupled to a support pedestal 125. The support pedestal 125 is mounted to the chamber body 101. The support pedestal 125 can optionally include a facility plate 180. The substrate support assembly 104 may be periodically removed from the support pedestal 125 to allow for refurbishment of one or more components of the substrate support assembly 104. Lifting pins 146 are disposed through the substrate support assembly 104 as conventionally known to facilitate substrate transfer.

[0041] The facility plate 180 is configured to accommodate a plurality of fluid connections from the electrostatic chuck 150 and the cooling base 131. The facility plate 180 is also configured to accommodate the plurality of electrical connections from the electrostatic chuck 150 and the heater assembly 169. The plurality of electrical connections can run externally or internally of the substrate support assembly 104, while the facility plate 180 provides an interface for the connections to a respective terminus.

[0042] A substrate electrode 109 is embedded within the substrate support portion 154 of the electrostatic chuck 150 for applying a substrate voltage to a substrate 105 disposed on an upper surface 160 of the substrate support assembly 104. The edge ring portion 156 has an edge ring electrode 111 embedded therein for applying an edge ring voltage to the edge ring 106. An edge ring IEDF width control circuit 155 is coupled to the edge ring electrode 111. A substrate IEDF width control circuit 158 is coupled to the substrate electrode 109. In one embodiment, a first shaped DC pulse voltage source 159 is coupled to one or both of the edge ring IEDF width control circuit 155 and the substrate IEDF width control circuit 158. In another embodiment, as shown in FIG. 1, the first shaped DC voltage source 159 is coupled to the edge ring IEDF width control circuit 155 and a second shaped DC voltage source 161 is coupled to the substrate IEDF width control circuit 158. The edge ring IEDF width control circuit 155 and the substrate IEDF width control circuit 158 are independently tunable. The substrate electrode 109 is further coupled to a chucking power source 115 to facilitate chucking of the substrate 105 to the upper surface 160 with the electrostatic chuck 150 during processing.

[0043] The inductively coupled plasma apparatus 107 is disposed above the lid 102 and is configured to inductively couple RF power to gases within the processing chamber 100 to generate a plasma 116. The inductively coupled plasma apparatus 107 includes first coil 118 and second coil 120 disposed above the lid 102. The relative position, ratio of diameters of each coil 118, 120, and/or the number of turns in each coil 118, 120 can each be adjusted as desired to control the profile or density of the plasma 116 being formed. Each of the first and second coils 118, 120 is coupled to an RF power supply 121 through a matching network 122 via an RF feed structure 123. The RF power supply 121 can illustratively be capable of

producing up to about 4000 W (but not limited to about 4000 W) at a tunable frequency in a range from 50 kHz to 13.56 MHz, although other frequencies and powers can be utilized as desired for particular applications.

[0044] In some examples, a power divider 126, such as a dividing capacitor, can be provided between the RF feed structure 123 and the RF power supply 121 to control the relative quantity of RF power provided to the respective first and second coils 118, 120. In other embodiments, a capacitively coupled plasma apparatus (not shown) can be used above the lid 102. A heater element 128 can be disposed on the lid 102 to facilitate heating the interior of the processing chamber 100. The heater element 128 can be disposed between the lid 102 and the first and second coils 118, 120. In some examples, the heater element 128 includes a resistive heating element and is coupled to a power supply 130, such as an AC power supply, configured to provide sufficient energy to control the temperature of the heater element 128 within a desired range.

[0045] During operation, the substrate 105, such as a semiconductor substrate or other substrate suitable for plasma processing, is placed on the substrate support assembly 104. Substrate lift pins 146 are movably disposed in the substrate support assembly 104 to assist in transfer of the substrate 105 onto the substrate support assembly 104. After positioning of the substrate 105, process gases are supplied from a gas panel 132 through entry ports 134 into the internal volume 124 of the chamber body 101. The process gases are ignited into a plasma 116 in the processing chamber 100 by applying power from the RF power supply 121 to the first and second coils 118, 120. The pressure within the internal volume 124 of the processing chamber 100 can be controlled using a valve 136 and a vacuum pump 138.

[0046] The processing chamber 100 includes the controller 108 to control the operation of the processing chamber 100 during processing. The controller 108 comprises a central processing unit (CPU) 140, a memory 142, and support circuits 144 for the CPU 140 and facilitates control of the components of the processing chamber 100. The controller 108 can be one of any form of general-purpose computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The memory 142 stores software (source or object

code) that can be executed or invoked to control the operation of the processing chamber 100 in the manner described herein. The controller 108 is configured to control the first shaped DC voltage source 159, the second shaped DC voltage source 161, the edge ring IEDF width control circuit 155, and the substrate IEDF width control circuit 158.

[0047] FIG. 2 is a schematic overview of a processing chamber 200 according to at least one embodiment of the present disclosure. The processing chamber 200 is configured to practice the schemes described herein. As with processing chamber 100, processing chamber 200 is a plasma processing chamber, such as those described above.

[0048] The processing chamber 200 includes a substrate 105 disposed on a substrate support assembly 104 as described in FIG. 1. An edge ring 106 is positioned on the substrate support assembly 104 and surrounds the periphery of the substrate 105. Although not shown, a capacitively coupled plasma apparatus is disposed above the substrate (typically above a chamber lid). The capacitively coupled plasma apparatus can include an ion suppressor and a showerhead where RF power is delivered from an electrode underneath the substrate to generate capacitively coupled plasma. A controller 108 is adapted to control systems and subsystems of the processing chamber. The controller 108 comprises a central processing unit (CPU) 140, a memory 142, and support circuits 144 for the CPU 140 and facilitates control of the components of the processing chamber 100. The controller 108 can be one of any form of general-purpose computer processor that can be used in an industrial setting for controlling various chambers and sub-processors. The memory 142 stores software (source or object code) that can be executed or invoked to control the operation of the processing chamber 100 in the manner described herein. The controller 108 is configured to control the first shaped DC voltage source 159, the second shaped DC voltage source 161, the edge ring IEDF width control circuit 155, and/or the substrate IEDF width control circuit 158. FIG.S 4A-4D, discussed below, show different configurations of connecting the IEDF width control module to the pulsers.

[0049] The substrate support assembly 104, facility plate 180, substrate electrode 109, and edge ring electrode 111 can be the same as that discussed in

FIG. 1. An edge ring IEDF width control circuit 155 is coupled to the edge ring electrode 111. A substrate IEDF width control circuit 158 is coupled to the substrate electrode 109. In one embodiment, a first shaped DC pulse voltage source 159 is coupled to one or both of the edge ring IEDF width control circuit 155 and the substrate IEDF width control circuit 158. In another embodiment, the first shaped DC voltage source 159 is coupled to the edge ring IEDF width control circuit 155 and a second shaped DC voltage source 161 is coupled to the substrate IEDF width control circuit 158. The edge ring IEDF width control circuit 155 and the substrate IEDF width control circuit 158 are independently tunable. The substrate electrode 109 is further coupled to a chucking power source 115 to facilitate chucking of the substrate 105 to the upper surface 160 with the electrostatic chuck 150 during processing.

[0050] Operation of the processing chamber 200 and processing of the substrate 105 can be performed in a similar fashion as that of processing chamber 100. In some embodiments, the processing system configurations include an ion suppressor positioned inside a processing chamber to control the type and quantity of plasma excited species that reach the substrate. In some embodiments, the ion suppressor unit is a perforated plate that may also act as an electrode of the plasma generating unit. In these and other embodiments, the ion suppressor can be the showerhead that distributes gases and excited species to a reaction region in contact with the substrate. In some embodiments, ion suppression is realized by a perforated plate ion suppressor and a showerhead, both of which plasma excited species pass through to reach the reaction region.

[0051] When voltage is applied to the substrate (or wafer) by the shaped DC voltage source 159, a waveform develops. FIG. 3A shows different bias voltage waveforms. The waveform includes two stages: an ion current stage and a sheath collapse stage. At the beginning of the ion current stage, a drop of wafer voltage creates a high voltage sheath above the substrate which accelerates positive ions to the substrate. The positive ions deposit positive charge on the substrate surface and tend to gradually increase the substrate voltage positively. If a square wave is supplied by the shaped DC voltage source 159, the ion current towards the substrate creates a positive slope of the substrate voltage, as shown by trace 305.

The voltage difference between the beginning and end of the ion current phase determines the IEDF width. The larger the voltage difference, the wider the IEDF width (FIG. 3B). To achieve monoenergetic ions and a narrower IEDF width, operations are performed to flatten the substrate voltage waveform (e.g., trace 310) in the ion current phase. In some embodiments, a voltage can be applied in order to achieve a certain IEDF width, as shown by the substrate waveform of trace 315.

[0052] At the end of the ion current stage, the substrate voltage rises to the bulk plasma voltage and the sheath collapses, such that electrons travel from the plasma to the substrate surface and neutralizes the positive charges at the substrate surface. As a result, the surface of the substrate is reset for the next cycle.

[0053] In some embodiments, the first and second shaped DC voltage sources 159 and 161 are positive pulsers. Positive pulsers generate pulses of positive voltage which corresponds to the sheath collapse stage. When each positive pulse turns off, the ion current stage begins. In some embodiments, the first and second shaped DC voltage sources 159 and 161 are negative pulsers. Negative pulsers generate pulses of negative voltage which corresponds to the ion current stage. When each negative pulse turns off, the sheath collapse stage begins.

Example Circuits

[0054] FIG. 4A is a schematic overview of an example circuit 465. As described below, and in some embodiments, the example circuit illustrated in FIG. 4A corresponds to the circuit diagram of FIGS. 5A and 6A. FIGS. 5A and 6A differ by, e.g., the circuitry of the second power module.

[0055] The example circuit 465 includes a pulsed DC power supply 466 coupled to a second power module 470 through a series inductor 468 and a resistor 469 in series. The second power module 470 modulates the width of the ion energy distribution function (IEDF). An optional blocking capacitor 471 may exist between plasma chamber load 472 and the rest of the circuit 465. A controller, not shown, which may be realized by hardware, software, firmware, or a combination thereof, is utilized to control various components represented in FIG. 4A.

[0056] The shaped DC power supply 466 generates a voltage waveform with two voltage levels—a low voltage level and a high voltage level. The low voltage level corresponds to the ion current stage. The high voltage level corresponds to the sheath collapse stage. In the ion current stage, the second power module 470 modulates the slope of the voltage vs. time, shown in FIG. 3A as traces 305, 310, and 315. Different slopes result in different IEDF widths as shown in FIG. 3B. The flattest slope (trace 305, FIG. 3A) corresponds to the narrowest IEDF width in FIG. 3B.

[0057] FIG. 4B is a schematic overview of an example circuit 475. As shown, FIG. 4B differs from FIG. 4A by replacing the series inductor 468 and resistor 469 with a switch 479. The switch 479 is connected in series with a pulsed DC power supply 476 and a second power module 478. During the ion current stage, the switch 479 is closed. During the sheath collapse stage, the switch can be either open or closed. A controller, not shown, which may be realized by hardware, software, firmware, or a combination thereof, is utilized to control various components represented in FIG. 4B.

[0058] FIG. 4C is a schematic overview of an example circuit 485. As described below, and in some embodiments, the example circuit 485 illustrated in FIG. 4C corresponds to the circuit diagrams of FIGS. 7A and 8. The example circuit 485 includes a shaped DC voltage source 486 coupled to ground. An optional blocking capacitor 487 may exist between the shaped DC voltage source 486 and a second power module 488. The second power module 488 modulates the width of the IEDF. The second power module 488 is further coupled to a plasma chamber load 489. A controller, not shown, which may be realized by hardware, software, firmware, or a combination thereof, is utilized to control various components represented in FIG. 4C.

[0059] The shaped DC voltage source 486 generates a voltage waveform with two voltage levels—a low voltage level and a high voltage level. The low voltage level corresponds to the ion current stage. The high voltage level corresponds to the sheath collapse stage. In the ion current stage, the second power module 488 creates a voltage slope vs. time. The resulting voltage waveform on the substrate is the sum of the output voltage of the shaped DC voltage source 486 and the

second power module 488, which can be modulated, and thereby, the IEDF width is modulated.

[0060] FIG. 4D is a schematic overview of an example circuit 490 according to at least one embodiment of the present disclosure. As described below, and in some embodiments, example circuit 490 corresponds to the circuit diagrams of FIGS. 9 and 10. The example circuit 490 includes a shaped DC voltage source 491 coupled to ground, second power module 492, and substrate chucking and bias compensation module 493. A switch 495 is connected in series with the substrate chucking and bias compensation module 493. The second power module 492 and the substrate chucking and bias compensation module 493 are connected in parallel, with one end coupled to the shaped DC voltage source 491 and the other end coupled to a plasma chamber load 494. The second power module 492 modulates the width of the IEDF. The second power module 492 and the substrate chucking and bias compensation module 493 are further coupled to a plasma chamber load 494. A controller, not shown, which may be realized by hardware, software, firmware, or a combination thereof, is utilized to control various components represented in FIG. 4D.

[0061] The shaped DC voltage source 491 generates a voltage waveform with two voltage levels—a low voltage level and a high voltage level. The low voltage level corresponds to the ion current stage. The high voltage level corresponds to the sheath collapse stage. In the ion current stage, the second power module 492 creates a voltage slope vs. time. The resulting voltage waveform on the substrate is the sum of the output voltage of the shaped DC voltage source 491 and the second power module 492, which can be modulated, and thereby, the IEDF width is modulated. The switch 495 is open in the ion current stage, such that the chucking and bias compensation module 493 do not modulate the voltage of the plasma chamber load. In the sheath collapse stage, the switch 495 is closed, and the chucking and bias compensation module 493 resets the substrate chucking voltage to a setpoint.

[0062] FIG. 5A is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 500 for driving the substrate electrode 109 and/or the edge ring electrode 111 of substrate support

assembly 104. Circuit 500 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current phase. The main pulser 502 can be the first or second shaped DC voltage source 159, 161 coupled to ground 501. The main pulser 502 is coupled to a current return path 503. The current return path 503 includes an inductor 504 coupled in series with a resistor 506 to an IEDF width control module 508 (e.g., second power module in FIGS. 4A and 4B). The IEDF width control module 508 modulates the ion energy distribution function (IEDF) width.

[0063] The IEDF width control module 508 can be modeled as a circuit comprising a transistor-transistor logic (TTL) signal 510 coupled in parallel with a switch 512, an optional diode 514, an optional capacitance 516 coupled to ground 517, and a third shaped DC pulse voltage source 518. Diode 514 is a flyback diode for protecting the switch 512 and the third shaped DC pulse voltage source 518. In some embodiments, a capacitance 520 exists between the current return path 503 and a chamber capacitance 536. The capacitance 536 can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. In some embodiments, the capacitance is also coupled to a substrate chucking and bias compensation module 522.

[0064] The substrate chucking and bias compensation module 522 is a circuit that includes a diode 524 coupled in series to a resistor 526, and a DC voltage source 528, and a resistor 530 coupled in series to a capacitance 532 and ground 534. The capacitance 536 is further coupled to stray capacitance 538 and the plasma sheath 540. The substrate chucking and bias compensation module 522 is further coupled to stray capacitance 538. The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548. In some embodiments, the series inductor 504 and resistor 506 in the current return path can be replaced by a switch 179 (FIG. 4B). The switch 179 is closed during the ion current stage.

[0065] In use, and for the configuration illustrated in FIG. 5A, the third shaped DC pulse voltage source 518 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 512 is controlled by TTL

signal 510 synchronized with the main pulser 502, as shown in plot 550 of FIG. 5B. The switch 512 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 512 can be kept closed during the sheath collapse stage to connect the current return path 503 to ground. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 512 can be opened such that the third shaped DC pulse voltage source 518 is functioning to modulate the IEDF during the ion current stage. The optional capacitance 516 can be used to adjust the sensitivity of the substrate voltage waveform to the third shaped DC pulse voltage source 518. Capacitance 542 is a plasma sheath capacitance, which is different in different process conditions, and current source 544 is the ion current towards the substrate that is also a variable. Capacitance 536 and stray capacitance 538 are capacitances related to the chamber and are constant. Capacitance 520 is a blocking capacitor and is also constant.

[0066] As shown in FIG. 5C and FIG. 5D, during the ion current stage and when the IEDF width control module 508 (FIG. 5A) is controlling the substrate or edge ring waveform actively, the active components in the circuit model include the ion current 544 (I_0), the sheath capacitance 542 (C_1), the chamber capacitance 536 (C_2), the stray capacitance 538 (C_3), the blocking capacitance 520 (C_4), and the optional capacitance 516 (C_5) in parallel with the third shaped DC pulse voltage source 518 (V_1). Because the inductor 504 and the resistor 506 in the current return path have little impact on IEDF width modulation, the inductor 504 and the resistor 506 are treated as short in the control circuit 560 of FIG. 5C and the control circuit 570 of FIG. 5D.

[0067] The intrinsic factor to broaden the IEDF is the ion current, I_0 , depositing positive charges on the substrate such that the voltage of the substrate gradually increases and the ion energy bombarding the substrate drops (e.g., trace 305 of FIG. 3A). The amount of IEDF broadening depends on, e.g., the ion current I_0 , the sheath capacitance C_1 , and/or other capacitances associated with the chamber C_2 , C_3 and C_4 , and power supply module, V_1 and C_5 , in the control circuits 560, 570. In order to compensate the ion current effect of IEDF broadening and/or have active control of IEDF width, the values of all the components in this control circuit (FIG.

5C) are determined. The capacitances associated with the chamber and power supply module, C2 through C5, can be determined by the product specification sheet or estimation using chamber parts dimensions, or by prior measurement, such as direct measurement of the impedance using a multimeter, or extracting the capacitance value from S-parameter or Z-parameter measurements. The ion current I_0 and the sheath capacitance C1 vary at varying plasma process conditions and are determined via real-time measurement during the plasma process. The shaped DC pulse voltage source V1 has a saw-shaped voltage output (FIG. 5E). The slope of the voltage output, dV_1/dt , can be varied to determine the ion current I_0 and the sheath capacitance C1, and/or to modulate the IEDF width. In the configuration of FIG. 5A, the output voltage of the shaped DC pulse voltage source V1 in the sheath collapse stage is zero, as trace 584 shows. Traces 582 and 586 show other possible waveforms for the shaped DC pulse voltage source V1, as discussed below.

[0068] The method of IEDF modulation includes two parts: (1) determining the ion current I_0 and the sheath capacitance C1, and (2) determining the slope of the shaped DC pulse voltage source dV_1/dt to achieve a target IEDF width. With a saw-like voltage source V1 and shaped DC voltage source 159 or 161 supplying power to the substrate 105 or edge ring 106, the IEDF width at the substrate or edge ring is the change of substrate or edge ring voltage from the beginning to the end of the ion current stage (FIG. 3A and FIG. 3B). In the control circuit 560 FIG. 5C and the control circuit 570 FIG. 5D, the IEDF width corresponds to the change of voltage across the sheath capacitance C1 from the beginning to the end of the ion current stage, which is determined by the charging or discharging current, I_1 , through the sheath capacitance C1:

$$\Delta V = I_1 * T / C_1, \quad (1)$$

where ΔV is the IEDF width and T is the time duration of the ion current stage. In order to obtain the target IEDF width (ΔV), the sheath capacitance C1 and the desired current I_1 through the sheath capacitance are to be determined.

[0069] To determine the sheath capacitance C1 and the ion current I_0 , the relationships of the currents and voltages in the control circuit are analyzed. As

shown, the currents passing the capacitors C1 through C4 are referred to as I1 through I4, with the arrows in the circuit schematic pointing to the positive direction. Based on Kirchhoff's current law, the ion current I0 equals the sum of the currents through capacitors C1 and C2:

$$I_0 = I_1 + I_2. \quad (2)$$

[0070] The current through capacitor C2 equals the sum of the currents through capacitors C3 and C4:

$$I_2 = I_3 + I_4. \quad (3)$$

[0071] Based on Kirchhoff's voltage law, the voltage sum of the closed loop of C1, C2, and C3 is zero. The time derivative of the voltage sum of C1, C2, and C3 is also zero. Denote the voltage at the intersection of capacitors C2 and C3 as V3. The time derivative of the voltage across capacitor C3 is $dV_3/dt = I_3/C_3$. Similar relationships exist for capacitors C1 and C2, and Kirchhoff's voltage law provides equation (4):

$$I_1/C_1 = I_2/C_2 + I_3/C_3. \quad (4)$$

[0072] Applying Kirchhoff's voltage law to the closed loop of capacitors C3 and C4 and voltage source V1 provides equation (5):

$$I_3/C_3 = I_4/C_4 + dV_1/dt. \quad (5)$$

[0073] In equations (2)-(5), C2, C3, and C4 are prior determined by the product specification sheet or estimation based on chamber parts dimensions, or by prior measurement, such as direct measurement of the impedance using a multimeter, or extracting the capacitance value from S-parameter or Z-parameter measurements. The current I4 can be measured directly by sensors, such as current probes and/or integrated voltage-current (VI) sensors. Voltage V3 can be measured directly by sensors, such as voltage probes and/or integrated VI sensors. Current I3 can be calculated as $I_3 = C_3 \cdot dV_3/dt$. The voltage slope dV_1/dt is user-controlled and known, such as zero or 1 Volt/nanosecond (V/nsec). By setting the shaped DC pulse voltage source V1 at two different slopes dV_1/dt and dV_1'/dt , the currents I4, I4' and the time derivatives of the voltage dV_3/dt , dV_3'/dt can be determined. The

set of equations (2)-(5) at two slopes $dV1/dt$ and $dV1'/dt$ form eight equations that can be solved to give the sheath capacitance:

$$C1 = \frac{\left(1 + \frac{C3}{C4}\right)(I4 - I4') + C3\left(\frac{dV1}{dt} - \frac{dV1'}{dt}\right)}{\left(\frac{1}{C2} + \frac{1}{C4} + \frac{C3}{C2C4}\right)(I4 - I4') + \left(\frac{C3}{C2} + 1\right)\left(\frac{dV1}{dt} - \frac{dV1'}{dt}\right)}; \quad (6)$$

and the ion current:

$$I0 = \left(1 + \frac{C1}{C2} + \frac{C1}{C4} + \frac{C3}{C4} + \frac{C1C3}{C2C4}\right)I4 + \frac{C1C3}{C2} + C1 + C3 \frac{dV1}{dt} \quad (7)$$

[0074] To obtain the target IEDF width (ΔV), the total current through the sheath capacitor C1 is

$$I1 = C1 \cdot \Delta V / T. \quad (8)$$

[0075] Plugging equations (6)-(8) into equations (2)-(5) gives the voltage slope of the saw-like voltage source V1 for achieving the IEDF width ΔV :

$$\frac{dV1}{dt} = - \left(\frac{1}{C2} + \frac{1}{C4} + \frac{C3}{C2C4}\right)I0 + \left(\frac{1}{C1} + \frac{1}{C2} + \frac{1}{C4} + \frac{C3}{C1C4} + \frac{C3}{C2C4}\right)C1 \cdot \Delta V / T \quad (9)$$

[0076] In the case of the narrowest IEDF ($\Delta V=0$), the voltage slope of the saw-like voltage source V1 is

$$\frac{dV1}{dt} = - \left(\frac{1}{C2} + \frac{1}{C4} + \frac{C3}{C2C4}\right)I0 \quad (10)$$

[0077] FIG. 6A is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 600 for driving the substrate electrode 109 and/or the edge ring electrode 111 of substrate support assembly 104. Circuit 600 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current phase. The main pulser 502 can be a first or second shaped DC voltage source 159, 161 coupled to ground 501. The main pulser 502 is coupled to a current return

path 503. The current return path 503 includes an inductor 504 coupled in series with a resistor 506 to an IEDF width control module 602 (e.g., second power module in FIGS. 4A and 4B). The IEDF width control module 602 modulates IEDF width. The IEDF width control module 602, which differs from the configuration of FIG. 5A, may be modeled as a circuit comprising a TTL signal 510 coupled in parallel with a switch 512, a diode 514, an optional capacitance 516 coupled to ground 517, and a DC voltage source 604 coupled in series to resistor 606. Diode 514 is a flyback diode for protecting the switch 512 and the DC voltage source 604. In some embodiments, a blocking capacitance 520 exists between the current return path 503 and a chamber capacitance 536. The capacitance 536 can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. In some embodiments, a substrate chucking and bias compensation module 522 is also coupled to the blocking capacitance 520 and the chamber capacitance 536. The substrate chucking and bias compensation module 522 is further coupled to stray capacitance 538. The substrate chucking and bias compensation module 522 is a circuit that includes a diode 524 coupled in series to a resistor 526, and a DC voltage source 528, and a resistor 530 coupled in series to a capacitance 532 and ground 534.

[0078] The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548.

[0079] In use, and for the configuration illustrated in FIG. 6A, the DC voltage source 604 together with the resistor 606 acts as an active knob for controlling the slope of the substrate or edge ring voltage waveform in the ion current stage, as opposed to the configuration of FIG. 5A, where the third shaped DC pulse voltage source 518 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 512 can be controlled by TTL signal 510 synchronized with the main pulser 502, as shown in FIG. 5B. The switch 512 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 512 can be kept closed during the sheath collapse stage to connect the current return path 503 to ground. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 512 can be opened,

such that the DC voltage source 604 is functioning to modulate IEDF in the ion current stage. The optional capacitance 516 can be used to adjust the sensitivity of the substrate voltage waveform to the DC voltage source 604. Capacitance 542 is a plasma sheath capacitance and is variable. Current source 544 is an ion current towards the substrate and also varies. Capacitance 536 can be, for example, the capacitance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. Capacitance 538 can be the capacitance the substrate electrode 109 and ground, or between the edge ring electrode 111 and ground. Capacitance 520 is a blocking capacitor and is also constant.

[0080] As shown in FIG. 6B and FIG. 6C, during the ion current stage and when the IEDF width control module 602 (FIG. 6A) is controlling the substrate or edge ring waveform actively, the active components in the circuit model include the ion current 544 (I_0), the sheath capacitance 542 (C_1), the chamber capacitance 536 (C_2), the stray capacitance 538 (C_3), the blocking capacitance 520 (C_4), and the optional capacitance 516 (C_5) in parallel with the DC voltage source 604 (V_0) and resistor 606 (R). Because the inductor 504 and the resistor 506 in the current return path have little impact on IEDF width modulation, the inductor 504 and the resistor 506 are treated as short in the control circuit 650 of FIG. 6B and the control circuit 660 of FIG. 6C. The control circuit of FIG. 6A is shown in FIG. 6B, while the control circuit of FIG. 7A, described below, is shown in FIG. 6C.

[0081] The intrinsic factor to broaden IEDF is the ion current I_0 depositing positive charges on the substrate such that the voltage of the substrate gradually increases and the ion energy bombarding the substrate drops (trace 305 of FIG. 3A). The amount of IEDF broadening depends on, e.g., the ion current I_0 , the sheath capacitance C_1 , and other capacitances associated with chamber (C_2 , C_3 , and C_4), and the power supply module (V_0 , R , and C_5) in control circuit 650 and control circuit 660 of FIG. 6B and FIG. 6C, respectively. In order to compensate the ion current effect of IEDF broadening and have active control of IEDF width, the values of all the components in control circuit 650 and control circuit 660 are determined. The capacitances associated with the chamber and power supply module, C_2 through C_5 , can be determined by the product specification sheet or

estimation using chamber parts dimensions, or by prior measurement, such as direct measurement of the impedance using a multimeter, or extracting the capacitance value from S-parameter or Z-parameter measurements. The resistor R is also prior determined by the product specification sheet or by direct measurement utilizing a multimeter. The ion current I₀ and the sheath capacitance C₁ vary at varying plasma process conditions are determined by real-time measurement during the plasma process. The DC voltage source V₀ is the active control knob and can be varied to determine the ion current I₀, to determine the sheath capacitance C₁, and/or to modulate the IEDF width.

[0082] The method of IEDF modulation includes two parts: (1) determining the ion current I₀ and the sheath capacitance C₁, and (2) determining the DC voltage V₀ to achieve the target IEDF width. The IEDF width is the spread of the substrate or edge ring voltage from the beginning to the end of the ion current stage (FIG. 3A and FIG. 3B). In the control circuit 650 of FIG. 6B and the control circuit 660 of FIG. 6C, the IEDF width corresponds to the change of the voltage across the sheath capacitance C₁ from the beginning to the end of the ion current stage, which is determined by the charging or discharging current, I₁, through the sheath capacitance C₁:

$$\Delta V = \frac{1}{C_1} \int_0^T I_1 d\tau, \quad (11)$$

where ΔV is the IEDF width and T is the time duration of the ion current stage. In order to obtain the target IEDF width (ΔV), the sheath capacitance C₁ and the desired current I₁ through the sheath capacitance are to be determined.

[0083] To determine the sheath capacitance C₁ and the ion current I₀, the relationships of the currents and voltages in the control circuit are analyzed. Here, for example, the currents passing the capacitors C₁ through C₅ are referred to as I₁ through I₅, with the arrows in the circuit schematic pointing to the positive direction. The voltage at the intersection of capacitors C₂ and C₃ is V₃. There is a threshold voltage for the DC voltage source V₀, denoted as V_{th}, below which the diode D₃ bypasses the series of the DC voltage source V₀ and the resistor R such that the output voltage of the IEDF width control module is zero. V_{th} is plasma-condition

dependent and can be determined experimentally by, e.g., gradually increasing the DC voltage V_0 up to the point that the current I_4 or voltage V_3 is affected by the DC voltage output V_0 .

[0084] In the case of $V_0 \leq V_{th}$, based on Kirchhoff's current law, the ion current I_0 equals the sum of the currents through capacitors C_1 and C_2 :

$$I_0 = I_1 + I_2. \quad (12)$$

[0085] The current through capacitor C_2 equals the sum of the currents through capacitors C_3 and C_4 :

$$I_2 = I_3 + I_4. \quad (13)$$

[0086] Based on Kirchhoff's voltage law, the voltage sum of the closed loop of C_1 , C_2 , and C_3 is zero. The time derivative of the voltage sum of C_1 , C_2 , and C_3 is also zero. The time derivative of the voltage across capacitor C_3 is $dV_3/dt = I_3/C_3$. The same relationships hold for capacitors C_1 and C_2 . Using Kirchhoff's voltage law on capacitors C_1 and C_2 provides equation (14):

$$I_1/C_1 = I_2/C_2 + I_3/C_3. \quad (14)$$

[0087] Applying Kirchhoff's voltage law to the closed loop of capacitors C_3 and C_4 , as well as the diode-bypassed IEDF width control module, provides equation (15):

$$I_3/C_3 = I_4/C_4. \quad (15)$$

[0088] In the case of $V_0 > V_{th}$, equations (12)-(14) still hold. Applying Kirchhoff's voltage law to the closed loop of capacitors C_3 , C_4 , and C_5 provides equation (16):

$$I_3/C_3 = I_4/C_4 + I_5/C_5. \quad (16)$$

[0089] Applying Kirchhoff's voltage law to the closed loop of capacitor C_5 , DC voltage source V_0 , and resistor R provides equation (17):

$$\frac{I_5}{C_5} = R \frac{d(I_4 - I_5)}{dt}, \quad (17)$$

where (I_4-I_5) is the current through the DC voltage source V_0 and the resistor R when the diode D_3 is inactive.

[0090] In some embodiments, there is no capacitor C_5 . In such cases, there is no equation (17) and equation (16) becomes

$$I_3/C_3 = I_4/C_4 + R \cdot dI_4/dt, \quad (18)$$

[0091] In equations (12)-(18), C_2 , C_3 , C_4 , and C_5 are prior determined by the product specification sheet or estimation based on chamber parts dimensions, or by prior measurement, such as direct measurement of the impedance using a multimeter, or extracting the capacitance value from S-parameter or Z-parameter measurements. The current I_4 can be measured directly by sensors, such as current probes and/or integrated VI sensors. Voltage V_3 can be measured directly by sensors, such as voltage probes and/or integrated VI sensors. Current I_3 can be calculated as $I_3 = C_3 \cdot dV_3/dt$. The DC voltage V_0 is user-controlled and known, such as setting the DC voltage output V_0 to a value from zero to a few kV. By setting the DC voltage V_0 at two different values V_0 and V_0' , with at least one of them above the threshold voltage V_{th} , the currents I_4 , I_4' and the time derivatives of the voltage dV_3/dt , dV_3'/dt can be determined. Solving the set of equations (12)-(18) gives the sheath capacitance C_1 :

$$C_1 = \frac{I_3 - I_3' + I_4 - I_4'}{\frac{I_3 - I_3' + I_4 - I_4'}{C_2} + \frac{I_3 - I_3'}{C_3}}; \quad (19)$$

and the ion current I_0 :

$$I_0 = (C_1/C_2 + C_1/C_3 + 1) \cdot I_3 + (C_1/C_2 + 1) \cdot I_4. \quad (20)$$

[0092] Plugging in the sheath capacitance C_1 and the ion current I_0 in the set of equations (12)-(18), the currents I_1 through I_5 can be calculated for any DC voltage V_0 .

[0093] Plugging in the expression of I_1 into equation (11) by the known capacitances C_1 through C_5 , the resistance R , and the DC voltage V_0 , the

relationship between the IEDF width (ΔV) and the DC voltage V_0 can be obtained. Accordingly, for a target IEDF width (ΔV), the required DC voltage V_0 is determined.

[0094] In some embodiments, the resistor R is large enough (e.g., about 10 k Ω), and the current through the DC voltage source V_0 is approximately time constant in the ion current stage and equal to V_0/R . In these embodiments, equation (17) becomes

$$I_4 = I_5 + V_0/R. \quad (21)$$

[0095] Solving equations (12), (13), (14), (16), and (21) gives the total current through the sheath capacitor C_1 as equation (22):

$$I_1 = \left[I_0 \left(\frac{1}{C_2} + \frac{C_4 + C_5}{k} \right) + \frac{C_3(C_4 + C_5)V_0}{kRC_5} \right] / \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{C_4 + C_5}{k} \right), \quad (22)$$

where

$$k = C_3C_4 + C_4C_5 + C_5C_3$$

[0096] Using equation (8) for this approximate case of constant current I_1 , the DC voltage V_0 utilized for obtaining the target IEDF width (ΔV) can be found using equation (23):

$$V_0 = \left[\frac{C_1 \Delta V}{T} \left(\frac{1}{C_1} + \frac{1}{C_2} + \frac{C_4 + C_5}{k} \right) - I_0 \left(\frac{1}{C_2} + \frac{C_4 + C_5}{k} \right) \right] / \frac{C_3(C_4 + C_5)}{kRC_5}. \quad (23)$$

[0097] In the case of narrowest IEDF ($\Delta V=0$), the DC voltage V_0 is

$$V_0 = -I_0 \left(\frac{1}{C_2} + \frac{C_4 + C_5}{k} \right) / \frac{C_3(C_4 + C_5)}{kRC_5}. \quad (24)$$

[0098] FIG. 7A is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 700 for driving the substrate electrode 109 and/or the edge ring electrode 111 of substrate support assembly 104. Circuit 700 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current

phase. The main pulser 502 can be the first or second shaped DC voltage source 159, 161 coupled to ground 501. The main pulser 502 is coupled to an IEDF width control module 702 (e.g., second power module in FIG. 4C) either directly or through a capacitance 701.

[0099] The IEDF width control module 702 may be modeled as a circuit comprising a TTL signal 704 coupled in parallel with a switch 706. The TTL signal 704 is coupled in series with ground 716. Switch 706 is coupled in parallel to diode 708, a DC voltage source 710, and an optional capacitance 714. The DC voltage source 710 is coupled in series to resistor 712. The IEDF width control module 702 is coupled to a chamber capacitance 536. The capacitance 536 can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. In some embodiments, the IEDF width control module 702 is also coupled to the substrate chucking and bias compensation module 522 discussed above. The substrate chucking and bias compensation module 522 is further coupled to stray capacitance 538. The substrate chucking and bias compensation module 522 is a circuit that includes a diode 524 coupled in series to a resistor 526, and a DC voltage source 528, and a resistor 530 coupled in series to a capacitance 532 and ground 534. The diode 708 is a flyback diode for protecting the switch 706 and DC voltage source 710.

[0100] The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548.

[0101] In use, and for the configuration shown in FIG. 7A, the DC voltage source 710 together with the resistor 712 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 706 can be controlled by TTL signal 704 synchronized with the main pulser 502, as shown in the plot of FIG. 5B. The switch 706 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 512 can be kept closed during the sheath collapse stage. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 706 can be opened such that the DC voltage source 710 is functioning to modulate IEDF in the ion current stage. The optional capacitance 714 can be used to adjust the sensitivity of the substrate voltage

waveform to the DC voltage source 710. The control mechanism of FIG. 7A is similar to the control mechanism of FIG. 6A. One difference is that the control circuit of FIG. 7A is shown in FIG. 6C, described above, and the control circuit of FIG. 6A is shown in FIG. 6B.

[0102] FIG. 8 is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 800 for driving the substrate electrode 109 and/or the edge ring electrode 111 of substrate support assembly 104. Circuit 800 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current phase. The main pulser 502 can be the first or second shaped DC voltage source 159, 161 coupled to ground 501. The main pulser 502 is coupled to an IEDF width control module 802 (e.g., second power module in FIG. 4C) either directly or through a capacitance 701.

[0103] The IEDF width control module 802 may be modeled as a circuit comprising a TTL signal 704 coupled in parallel with a switch 706. The TTL signal 704 is also coupled in series with ground 716. Switch 706 is coupled in parallel to diode 708, a third shaped DC pulse voltage source 804, and an optional capacitance 714. The IEDF width control module 802 is coupled to a chamber capacitance 536. The capacitance 536 can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. In some embodiments, the IEDF width control module 802 is also coupled to the substrate chucking and bias compensation module 522 discussed above. The substrate chucking and bias compensation module 522 is a circuit that includes a diode 524 coupled in series to a resistor 526, a DC voltage source 528, and a resistor 530 coupled in series to a capacitance 532 and ground 534. The diode 708 is a flyback diode for protecting the switch and the third shaped DC pulse voltage source 804.

[0104] The substrate chucking and bias compensation module 522 is further coupled to chamber capacitance 536. The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548.

[0105] In use, and for the configuration shown in FIG. 8, the third shaped DC pulse voltage source 804 acts as the active knob for controlling the slope of the voltage waveform in the ion current stage, as opposed to the configuration of FIG. 7A, where the DC voltage source 710 together with the resistor 712 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 706 can be controlled by TTL signal 704 synchronized with the main pulser 502, as shown in the plot of FIG. 5B. The switch 706 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 706 is kept closed during the sheath collapse stage. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 706 can be opened such that the third shaped DC pulse voltage source 804 is functioning to modulate IEDF in the ion current stage. The optional capacitance 714 can be used to adjust the sensitivity of the substrate voltage waveform to the third shaped DC pulse voltage source 804. The control mechanism of FIG. 8 is similar to that of FIG. 5A. One difference is that the control circuit of FIG. 8 is shown in FIG. 5D, described above, and the control circuit of FIG. 5A is shown in FIG. 5C.

[0106] For the configurations shown in FIGS. 5A, 6A, 7, and 8, it is contemplated that the substrate chucking and bias compensation module can be connected to the circuit in any suitable manner without departing from the scope of the embodiments described herein. It is also contemplated that the substrate chucking and bias compensation module can include additional or different components without departing from the scope of the embodiments described herein.

[0107] FIG. 9 is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 900 for driving the substrate electrode 109 and/or the edge ring electrode 111 of substrate support assembly 104. Circuit 900 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current phase. The main pulser 502 can be the first or second shaped DC pulse voltage source 159, 161 coupled to ground 501. The main pulser 502 is coupled to an IEDF width control module 902 (e.g., second power module in FIG. 4D).

[0108] The IEDF width control module 902 may be modeled as a circuit comprising a TTL signal 904 coupled in parallel with a switch 906. The TTL signal

904 is also coupled in series with ground 916. Switch 906 is coupled in parallel to diode 908. The combination of the TTL signal 904, the switch 906, and the diode 908 controls whether the substrate chucking and bias compensation module 920 is connected to another part of the circuit. The substrate chucking and bias compensation module 920 is a circuit that includes a capacitance 926 coupled in parallel to resistor 922 and a DC voltage source 924. The substrate chucking and bias compensation module 920 is coupled in series with the assembly of the TTL signal 904, the switch 906, and the diode 908. The substrate chucking and bias compensation module 920 and the switch 906, as a whole, is coupled in parallel to a DC voltage source 910 in series with a resistor 912, and also in parallel to an optional capacitor 914. The diode 908 is a flyback diode for protecting the switch 906 and DC voltage sources 910 and 924.

[0109] A capacitance 536 may exist between stray capacitance 538 and the plasma sheath 540, which can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. Both the IEDF width control module 902 and the substrate chucking and bias compensation module 920 are coupled to either the substrate electrode 109 and/or the edge ring electrode 111. The IEDF width control module 902 is also coupled to stray capacitance 538. The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548.

[0110] In use, and for the configuration illustrated in FIG. 9, the DC voltage source 910 together with the resistor 912 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 906 can be controlled by TTL signal 904 synchronized with the main pulser 502, as shown in FIG. 5B. The switch 906 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 512 can be kept closed during the sheath collapse stage such that the substrate chucking and bias compensation module 920 is connected to another part of the circuit and resets the substrate chucking voltage to a setpoint. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 906 can be opened such that

the DC voltage source 910 is functioning to modulate IEDF in the ion current stage. The optional capacitor 914 can be used to adjust the sensitivity of the substrate voltage waveform to the DC voltage source 910. The control mechanism of FIG. 9 is similar to that shown in FIG. 6B described above. One difference is the capacitor C4 being removed.

[0111] FIG. 10 is a schematic circuit diagram illustrating an embodiment of an edge ring voltage control circuit/substrate voltage control circuit 1000 for driving the electrodes 109, 111 of the substrate support assembly 104. Circuit 1000 includes a main pulser 502 to reset the substrate voltage (corresponding to the voltage droop in Fig. 3A) at the beginning of each ion current phase. The main pulser 502 can be the first or second shaped DC pulse voltage sources 159, 161 coupled to ground 501. The main pulser 502 is coupled to an IEDF width control module 1002 (e.g., second power module in FIG. 4D).

[0112] The IEDF width control module 1002 may be modeled as a circuit comprising a TTL signal 904 coupled in parallel with a switch 906. The TTL signal 904 is also coupled in series with ground 916. Switch 906 is coupled in parallel to diode 908. The combination of the TTL signal 904, the switch 906, and the diode 908 controls whether the substrate chucking and bias compensation module is connected to another part of the circuit. The substrate chucking and bias compensation module 920 is a circuit that includes a capacitance 926 coupled in parallel to resistor 922 and a DC voltage source 924. The diode 908 is a flyback diode for protecting the switch, the DC voltage source 910, and the DC voltage source 924. The substrate chucking and bias compensation module 920 is coupled in series with the assembly of the TTL signal 904, the switch 906, and the diode 908. The substrate chucking and bias compensation module 920 and the switch 906, as a whole, is coupled in parallel to a shaped DC pulse voltage source 1004, and also in parallel to an optional capacitor 914.

[0113] A capacitance 536 may exist between stray capacitance 538 and the plasma sheath 540, which can be, for example, the impedance between the substrate electrode 109 and the substrate, or between the edge ring electrode 111 and the edge ring. Both the IEDF width control module 1002 and the substrate chucking and bias compensation module 920 are coupled to either the substrate

electrode 109 and/or the edge ring electrode 111. The IEDF width control module 1002 is also coupled to stray capacitance 538. The plasma sheath 540 may be modeled (plasma sheath model) as a circuit comprising a sheath capacitance 542 coupled in parallel with a current source 544 and a diode 546 coupled to ground 548.

[0114] In use, and for the configuration illustrated in FIG. 10, the shaped DC pulse voltage source 1004 acts as the active knob for controlling the slope of the voltage waveform in the ion current stage, as opposed to the configuration of FIG. 9, where the DC voltage source 910 together with the resistor 912 acts as an active knob for controlling the slope of the voltage waveform in the ion current stage. The switch 906 can be controlled by TTL signal 904 synchronized with the main pulser 502, as shown in the plot of FIG. 5B. The switch 906 can be closed before the voltage of the main pulser 502 goes up to enter the sheath collapse stage. The switch 512 can be kept closed during the sheath collapse stage such that the substrate chucking and bias compensation module is connected to another part of the circuit and resets the substrate chucking voltage to a setpoint. After the voltage of the main pulser 502 goes down to enter the ion current stage, the switch 906 can be opened such that the DC voltage source 910 is functioning to modulate IEDF in the ion current stage. The optional capacitor 914 can be used to adjust the sensitivity of the substrate voltage waveform to the shaped DC pulse voltage source 1004.

[0115] The control mechanism of FIG. 10 is similar to that of FIG. 5A. One difference is the capacitor C4 being removed. Another difference is the output voltage of the shaped DC pulse voltage source 1004 in the sheath collapse stage is held at the output voltage of the substrate chucking and bias compensation module 920 instead of zero, as the trace 582 (positive chucking voltage) and trace 586 (negative chucking voltage) in FIG. 5E.

Example Method

[0116] FIG. 11 is a flowchart of a method 1100 of controlling the IEDF width using the edge ring IEDF width control circuit 155 and/or the substrate IEDF width control circuit 158 according to at least one embodiment of the present disclosure.

The method 1100 can be implemented using one or more of the circuit configurations illustrated in FIGS. 5-10. The method 1100 also provides a method of operating the processing chamber 100 or processing chamber 200.

[0117] The method 1100 begins with applying, or otherwise introducing, a voltage to a suitable processing chamber by activating, or turning on, a main pulser (e.g., main pulser 502) coupled to a power module (e.g., the IEDF width control module). Here, the voltage is introduced to the substrate electrode, e.g., substrate electrode 109, and/or the edge ring electrode, e.g., edge ring electrode 111. The bias voltage on the substrate electrode and/or the edge ring electrode develops in the ion current stage and accelerates ions at an energy of, e.g., the product of the sheath voltage multiplied by the charge of the ions. In the collisionless sheath model, most of the ions can reach this maximum energy when bombarding the substrate electrode and/or edge ring electrode. However, due to, e.g., the ion current depositing positive charge on the substrate electrode and/or edge ring electrode, the voltage of the substrate electrode and/or edge ring electrode increases over time, reducing the sheath voltage and resulting in a spread of the ion energy.

[0118] At operation 1110, a current of the power module (e.g., the IEDF width control module), and/or a voltage or a voltage derivative of the IEDF width control module are measured under two or more conditions to determine the sheath capacitance $C1$ and/or the ion current $I0$. Here the current measured can be the current $I4$, which is the current through the capacitor $C4$ in FIGS. 5A, 6A, 7 and 8. Additionally, or alternatively, the current measured can be the output current of the main pulser in FIGS. 9 and 10. The voltage derivative can be $dV3/dt$. The measurements can be performed in the ion current stage. The two or more conditions can be achieved by setting the active knob (e.g., the DC voltage source $V0$ and/or the shaped DC pulse voltage source $dV1/dt$) in the IEDF width control module to two different values.

[0119] As an example, and for the configurations of FIGS. 5, 8, and 10, the shaped DC pulse voltage source can be set to any two different slopes $dV1/dt$ in the ion current stage. As another example, and for the configurations of FIGS. 6, 7, and 9, the DC voltage $V0$ can be increased gradually while monitoring $I4$ up to a point when $I4$ is affected by the DC voltage $V0$. This DC voltage is the threshold voltage

V_{th}. At least one of the two setpoints for the DC voltage source V₀ is larger than V_{th}. That is, measuring the current of the IEDF width control module, the voltage or voltage derivative of the IEDF width control module, or both, includes setting the DC voltage source, the shaped DC pulse voltage source, or both to a first value; and setting the DC voltage source, the shaped DC pulse voltage source, or both to a second value.

[0120] At operation 1115, the ion current I₀ and the sheath capacitance C₁ are calculated based on equations (6) and (7) for the configurations of FIGS. 5, 8, and 10, or equations (19) and (20) for the configurations of FIGS. 6, 7, and 9. The input values for the calculations are: $I_3 = C_3 \cdot dV_3/dt$; $I_3' = C_3 \cdot dV_3'/dt$; and I₄, I_{4'}. The values of C₃ and C_{3'} are known, and the values of dV₃/dt, dV_{3'}/dt, I₄, and I_{4'} are measured at operation 1110. As such, I₃ and I_{3'} can be calculated.

[0121] At operation 1120, a desired setpoint for a DC voltage (V₀) of the main pulser, a desired setpoint for a voltage (V₁) or a voltage derivative (dV₁/dt) of the IEDF width control module, or both, are determined to achieve a targeted IEDF width (ΔV). This determination is based on, e.g., determining a desired setting of the IEDF width control module to achieve a user-specified ion energy distribution width (ΔV). The DC voltage (V₀) of the main pulser and the slope (dV₁/dt) of the shaped DC pulse voltage (V₁), can be determined from equations (23) and (9), respectively. At operation 1125, the DC voltage (V₀) and/or the voltage (V₁) or voltage derivative (dV₁/dt) of the IEDF width control module are adjusted to the determined setpoints.

[0122] In contrast to conventional processes for controlling the IEDF, the method described herein is free of looping to determine the desired setpoint of the IEDF width control module. However, and in some embodiments, looping can be used to determine the desired set point. In such embodiments, the controller can monitor I₄ and V₃ in the ion current stage to detect any changes in the plasma conditions and to adjust the setpoint of the IEDF width control module accordingly.

[0123] The methods and apparatus, e.g., circuits, described herein enable control over the shape (e.g., narrow, or adjustable width) of the waveform of a pulsed DC

substrate voltage. Embodiments described herein further enable, e.g., control over the ion energy distribution, including monoenergetic ion acceleration.

[0124] As is apparent from the foregoing general description and the specific embodiments, while forms of the present disclosure have been illustrated and described, various modifications can be made without departing from the spirit and scope of the present disclosure. Accordingly, it is not intended that the present disclosure be limited thereby. Likewise, the term “comprising” is considered synonymous with the term “including.” Likewise whenever a composition, an element or a group of elements is preceded with the transitional phrase “comprising,” it is understood that we also contemplate the same composition or group of elements with transitional phrases “consisting essentially of,” “consisting of,” “selected from the group of consisting of,” or “is” preceding the recitation of the composition, element, or elements and vice versa.

[0125] While the foregoing is directed to examples of the present disclosure, other and further examples of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.