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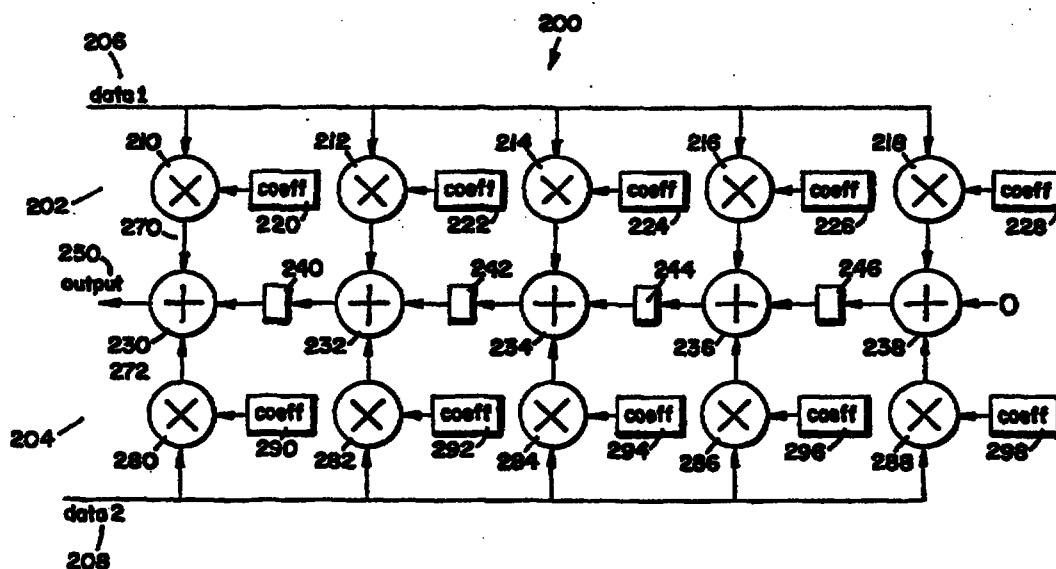


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| (21) International Application Number: PCT/US98/05854<br>(22) International Filing Date: 25 March 1998 (25.03.98)<br>(30) Priority Data:<br>60/042,469          25 March 1997 (25.03.97)          US<br>08/924,069          28 August 1997 (28.08.97)          US<br>(71) Applicant: LEVEL ONE COMMUNICATIONS, INC.<br>[US/US]; 9750 Goethe Road, Sacramento, CA 95827 (US).<br>(72) Inventor: RAO, Sailesh, Krishna; 8 Camby Drive, Colts Neck,<br>NJ 07722 (US).<br>(74) Agent: BOGUCKI, Raymond, A.; Merchant, Gould, Smith,<br>Edell, Welter & Schmidt, Suite 400, 11150 Santa Monica<br>Boulevard, Los Angeles, CA 90025 (US). |  | (81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ,<br>BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility<br>model), DE, DE (Utility model), DK, DK (Utility model),<br>EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE,<br>GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ,<br>LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW,<br>MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK<br>(Utility model), SL, TJ, TM, TR, TT, UA, UG, UZ, VN,<br>YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ,<br>UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD,<br>RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES,<br>FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent<br>(BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD,<br>TG).<br><br>Published<br>With international search report.<br>Before the expiration of the time limit for amending the<br>claims and to be republished in the event of the receipt of<br>amendments. |                                                                   |

(54) Title: COMBINED PARALLEL ADAPTIVE EQUALIZER/ECHO CANCELLER



(57) Abstract

A combined, parallel adaptive equalizer/echo canceller is disclosed. The equalizer/canceller receives at least one input signal which is split into  $n$  taps. The  $n$  taps are multiplied by corresponding  $n$  tap coefficients to produce  $n$  tap output signals. The  $n$  tap output signals are then processed through an additive pipeline to produce a filter output signal. The additive pipeline provides low latency by processing the  $n$ th most recent tap output signal  $n$  clock cycles from the filter output signal. The combined FIR filter structure is made fully adaptive using delayed LMS coefficient adaptation. Tap coefficients are updated using an error signal and delayed versions of the input signal. The error signal is a product of a calculated error and a negative adaptation factor. The delay is equal to a sum of  $n+1$  cycles.