COMPENSATING FOR REFERENCE MISALIGNMENT DURING INSPECTION OF PARTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of a co-pending U.S. Provisional Patent Application Serial Number 62/744,746 entitled “SUB MICRON INSPECTION” filed October 12, 2018, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

This patent relates to optical inspection and/or metrology of components such as semiconductor wafers, high-density circuit boards, multi-layer substrates, inner-layer substrates, chrome on glass masks, and other precision parts.

BACKGROUND

Consider an example precision part such as a multi-layer semiconductor or circuit boards with numerous die as shown in Figure 1A. Such parts are typically manufactured by laminating together multiple layers, each containing metallic conductors. Each layer is fabricated by first coating the layer with resist and then optically projecting, at different locations or sections of the layer, an image containing one or multiple die and then etching the metal to form the desired metallic circuit conductors. This procedure is typically referred to as a project, step and repeat process. Due to current manufacturing limitations, the placement of the projected patterns is known to vary slightly between the same layer design manufactured at different times or even between layers in the same manufacturing lot. This is especially true for large circuit panels manufactured on thin flexible organic substrates, some of which are currently on the order of 500 millimeters x 500 millimeters in size.

To facilitate the manufacture and optical inspection of all the die on the substrate, alignment marks are frequently placed in each individual die pattern. During the inspection process the substrate is typically scanned either by mechanically moving the substrate beneath an inspection camera or moving the camera over the substrate, or some combination thereof. Alignment marks, or unique conductor patterns within each die or die subsection, are located in the scanned images and used to align the scanned images to stored reference images of a good die or die subsection. Once aligned, the images are superimposed, and defects are reported in those locations where the stored reference and scanned camera images differ. As an example, Figure 1B illustrates a reference image of a conductor, shown in