SUMMARY OF THE INVENTION

One aim of the invention is to design an NCFET transistor that may allow better control of the electric current in the active layer, faster switching of the transistor, and improved coupling with the back gate, while at the same time having a simple structure and able to be fabricated using existing processes.

A first aspect of the invention provides an NCFET transistor comprising a semiconductor-on-insulator substrate for a fast-switching field-effect transistor, comprising, in succession from its base to its surface:

- a semiconductor support substrate,
- a single ferroelectric layer, arranged in direct contact with the semiconductor support substrate; and
- an active layer of a semiconductor material, suitable for forming a channel of the transistor, arranged in direct contact with the ferroelectric layer,

wherein the single ferroelectric layer is configured to be polarized by a bias voltage (Vbb) applied to a back gate of the NCFET transistor so as to form a negative capacitance,

said NCFET transistor furthermore comprising the channel arranged in the active layer, a source and a drain that are arranged in the active layer on either side of the channel, and a gate arranged on the channel, insulated from said channel by a gate dielectric.

"In succession from its base to its surface" should be understood to mean a stack of the layers in a direction perpendicular to the main surface of the support substrate, in the direction from the support substrate to the active layer.

"Direct contact" between two layers should be understood to mean direct contact over the extent of the interface between the layers in question.

The proposed architecture may make it possible to integrate the following in the ferroelectric layer, which forms the electrically insulating layer of the semiconductor-on-insulator substrate:

- electrical insulation properties, making it possible to obtain a transistor with a fully depleted active layer, and
- the ability to form a negative capacitance under the active layer, making it possible to control the threshold voltage of the transistor through the polarization of said ferroelectric layer.

The ferroelectric layer has a thickness of between 1 and 30 nm, and more advantageously of between 1 and 10 nm.

The ferroelectric layer has a relative dielectric permittivity greater than 10 and, particularly advantageously, a relative dielectric permittivity greater than 20. In some embodiments, the ferroelectric layer comprises hafnium oxide, zirconium oxide, yttrium oxide, lanthanum oxide, hafnium aluminate or an alloy comprising one or more of said materials.

The active layer has a thickness of between 1 nm and 100 nm. In some embodiments, the active layer comprises silicon, germanium, a silicon-germanium alloy, gallium arsenide, indium phosphide, gallium-indium arsenide, graphene or tungsten disulfide.

A second aspect of the invention provides a process for fabricating the negative-capacitance field-effect transistor of the first aspect, said process being primarily characterized in that it comprises the following steps:

- providing the semiconductor support substrate;
- providing a semiconductor donor substrate;
- forming at least one ferroelectric layer on a surface of the semiconductor support substrate and/or of the semiconductor donor substrate'
- forming a weakened zone in the semiconductor donor substrate, so as to delimit a semiconductor layer to be transferred;
- bonding the semiconductor donor substrate to the semiconductor support substrate, each ferroelectric layer being arranged at the bonding interface;
- detaching the semiconductor donor substrate along the weakened zone, after transferring the semiconductor layer onto the semiconductor support substrate, said semiconductor layer forming the active layer of the transistor,
- forming a channel in the active layer;
- forming a source and a drain in the active layer on either side of the channel; and
- depositing a gate dielectric on the channel and forming a gate on the channel, said gate being electrically insulated from said channel by said gate dielectric.

In some embodiments, said at least one ferroelectric layer is formed by thin atomic layer deposition or by pulsed laser ablation.

Preferably, the process comprises heat-treating said at least one ferroelectric layer before bonding. Advantageously, the heat treatment is carried out at a temperature of between 500°C and 1000°C. Advantageously, the heat treatment is carried out for a duration less than two hours.

In some embodiments, forming the weakened zone comprises implanting hydrogen and/or helium atoms into the donor substrate.

In some embodiments, the process comprises, before bonding, one or more surface treatments on said at least one ferroelectric layer, said treatments comprising cleaning, plasma treatment and/or chemical-mechanical polishing.

Advantageously, the process comprises, after the transfer step, annealing at a temperature less than or equal to 1000°C.

CLAIMS

1. An NCFET transistor comprising a semiconductor-on-insulator substrate for a field-effect transistor, comprising, in succession from its base to its surface:
   - o a semiconductor support substrate;
   - o a single ferroelectric layer, arranged in direct contact with the semiconductor support substrate; and
   - o an active layer of a semiconductor material, suitable for forming a channel of the transistor, arranged in direct contact with the ferroelectric layer,

   wherein the single ferroelectric layer is configured to be polarized by a bias voltage (Vbb) applied to a back gate of the NCFET transistor so as to form a negative capacitance,

   said NCFET transistor furthermore comprising the channel arranged in the active layer, a source and a drain that are arranged in the active layer on either side of the channel, and a gate arranged on the channel, insulated from said channel by a gate dielectric.

2. The NCFET transistor as claimed in claim 1, wherein the ferroelectric layer contained in the semiconductor-on-insulator substrate has a thickness of between 1 and 30 nm, and more advantageously of between 1 and 10 nm.

3. The NCFET transistor as claimed in claim 1 or claim 2, wherein the ferroelectric layer has a relative dielectric permittivity greater than 10, preferably greater than 20.

4. The NCFET transistor as claimed in one of the preceding claims, wherein the ferroelectric layer comprises hafnium oxide, zirconium oxide, yttrium oxide, lanthanum oxide, hafnium aluminate or an alloy comprising one or more of said materials.

5. The NCFET transistor as claimed in one of the preceding claims, wherein the active layer has a thickness of between 1 nm and 100 nm.

6. The NCFET transistor as claimed in one of the preceding claims, wherein the active layer contained in the semiconductor-on-insulator substrate comprises silicon, germanium, a silicon-germanium alloy, gallium arsenide, indium phosphide, gallium-indium arsenide, graphene or tungsten disulfide.

7. A process for fabricating an NCFET transistor as claimed in one of claims 1 to 6, said process comprising:
    - o providing the semiconductor support substrate;
    - o providing a semiconductor donor substrate;
    - o forming at least one ferroelectric layer on a surface of the semiconductor support substrate and/or of the semiconductor donor substrate;
    - o forming a weakened zone in the semiconductor donor substrate, so as to delimit a semiconductor layer to be transferred;
    - o bonding the semiconductor donor substrate to the semiconductor support substrate, each ferroelectric layer being arranged at the bonding interface;
    - o detaching the semiconductor donor substrate along the weakened zone, so as to transfer the semiconductor layer onto the semiconductor support substrate, said semiconductor layer forming the active layer of the transistor;
    - o forming a channel in the active layer;
    - o forming a source and a drain in the active layer on either side of the channel; and
    - o depositing a gate dielectric on the channel and forming a gate on the channel, said gate being electrically insulated from said channel by said gate dielectric.

8. The fabrication process as claimed in claim 7, wherein said at least one ferroelectric layer is formed by thin atomic layer deposition or by pulsed laser ablation.

9. The fabrication process as claimed in claim 7 or 8, comprising heat-treating said at least one ferroelectric layer before bonding.

10. The fabrication process as claimed in claim 9, wherein the heat treatment is carried out at a temperature of between 500°C and 1000°C.

11. The fabrication process as claimed in claim 9 or 10, wherein the heat treatment is carried out for a duration less than two hours.

12. The fabrication process as claimed in one of claims 7 to 11, wherein forming the weakened zone comprises implanting hydrogen and/or helium atoms into the donor substrate.

13. The fabrication process as claimed in one of claims 7 to 12, comprising, before bonding, one or more surface treatments on said at least one ferroelectric layer, said one or more surface treatments comprising cleaning, plasma treatment and/or chemical-mechanical polishing.

14. The fabrication process as claimed in one of claims 7 to 13, comprising, after transferring the semiconductor layer onto the support substrate, annealing at a temperature less than or equal to 1000°C.