Claims

1. A transistor comprising:

   a substrate;

   a first contact electrode over the substrate;

   a second contact electrode over the substrate;

   a two-dimensional semiconductor material layer above the substrate such that the first contact electrode is in contact with a first portion of the two-dimensional semiconductor material layer and the second contact electrode is in contact with a second portion of the two-dimensional semiconductor material layer;

   a first control gate over the two-dimensional semiconductor material layer such that the first portion of the two-dimensional semiconductor material layer is between the first control gate and the first contact electrode;

   a second control gate over the two-dimensional semiconductor material layer such that the second portion of the two-dimensional semiconductor material layer is between the second control gate and the second contact electrode;

   a main gate over a third portion of the two-dimensional semiconductor material layer, the third portion of the two-dimensional semiconductor material layer between the first portion of the two-dimensional semiconductor material layer and the second portion of the two-dimensional semiconductor material layer; and

   a dielectric layer separating the main gate, the first control gate and the second control gate from the two-dimensional semiconductor material layer.

2. The transistor according to claim 1, further comprising:

   one or more local gates such that the two-dimensional semiconductor material layer is over the one or more local gates; and

   a further dielectric layer in contact with the one or more local gates;

   wherein the two-dimensional semiconductor material layer is over the further dielectric layer.

3. The transistor according to claim 2,

wherein the dielectric layer and the further dielectric layer comprise an atomically thin insulating crystal material, a high-k dielectric material or a bulk dielectric material.

4. The transistor according to any one of claims 1 to 3,

wherein the two-dimensional semiconductor material layer comprises one or more monolayers of a suitable two-dimensional semiconductor material.

5. The transistor according to claim 4,

wherein the suitable two-dimensional semiconductor material is a transition-metal dichalcogenide material, graphene, a Group III-Group V chalcogenide material, or phosphorene.

6. The transistor according to claim 5,

wherein the suitable two-dimensional semiconductor material is the transition-metal dichalcogenide material; and

wherein the transition-metal dichalcogenide material is molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), rhemium diselenide ($ReSe_2$) or rhemium disulfide (ReS_2).

7. The transistor according to any one of claims 1 to 6,

wherein the main gate is arranged laterally between the first control gate and the second control gate.

8. The transistor according to any one of claims 1 to 6,

wherein a first portion of the main gate is over a portion of the first control gate; and

wherein a second portion of the main gate is over a portion of the second control gate.

9. The transistor according to claim 8, further comprising:

an embedding dielectric layer such that the main gate, the first control gate and the second control gate are in contact with the embedding dielectric layer;

wherein a first portion of the embedding dielectric layer separates the main gate from the first control gate; and

wherein a second portion of the embedding dielectric layer separates the main gate from the second control gate.

10. The transistor according to any one of claims 1 to 6,

wherein a portion of the first control gate is over a first portion of the main gate; and

wherein a portion of the second control gate is over a second portion of the main gate.

11. The transistor according to claim 10, further comprising:

an embedding dielectric layer such that the main gate, the first control gate and the second control gate are in contact with the embedding dielectric layer;

wherein a first portion of the embedding dielectric layer separates the main gate from the first control gate; and

wherein a second portion of the embedding dielectric layer separates the main gate from the second control gate.

12. A method of forming a transistor, the method comprising:

forming a first contact electrode over a substrate;

forming a second contact electrode over the substrate;

forming a two-dimensional semiconductor material layer above the substrate such that the first contact electrode is in contact with a first portion of the two-dimensional semiconductor material layer and the second contact electrode is in contact with a second portion of the two-dimensional semiconductor material layer;

forming a first control gate over the two-dimensional semiconductor material layer such that the first portion of the two-dimensional semiconductor material layer is between first control gate and the first contact electrode;

forming a second control gate over the two-dimensional semiconductor material layer such that the second portion of the two-dimensional semiconductor material layer is between second control gate and the second contact electrode;

forming a main gate over a third portion of the two-dimensional semiconductor material layer, the third portion of the two-dimensional semiconductor material layer between the first portion of the two-dimensional semiconductor material layer and the second portion of the two-dimensional semiconductor material layer; and

forming a dielectric layer separating the main gate, the first control gate and the second control gate from the two-dimensional semiconductor material layer.

13. The method according to claim 12, further comprising:

forming one or more local gates such that the two-dimensional semiconductor material layer is over the one or more local gates; and

forming a further dielectric layer in contact with the one or more local gates;

wherein the two-dimensional semiconductor material layer is over the further dielectric layer.

14. The method according to claim 13,

wherein the dielectric layer and the further dielectric layer comprise an atomically thin insulating crystal material, a high-k dielectric material or a bulk dielectric material.

15. The method according to any one of claims 12 to 14,

wherein the two-dimensional semiconductor material layer comprises one or more monolayers of a suitable two-dimensional semiconductor material.

16. The method according to claim 15,

Wherein the suitable two-dimensional semiconductor material is a transition-metal dichalcogenide material, graphene, a Group III-Group V chalcogenide material, or phosphorene.

17. The method according to claim 16,

wherein the suitable two-dimensional semiconductor material is the transition-metal dichalcogenide material; and

wherein the transition-metal dichalcogenide material is molybdenum disulfide (MoS_2), tungsten diselenide (WSe_2), molybdenum diselenide ($MoSe_2$), tungsten disulfide (WS_2), rhemium diselenide ($ReSe_2$) or rhemium disulfide (ReS_2).

18. The method according to any one of claims 12 to 17,

wherein the main gate is arranged laterally between the first control gate and the second control gate.

19. The method according to any one of claims 12 to 17,

wherein a first portion of the main gate is over a portion of the first control gate; and

wherein a second portion of the main gate is over a portion of the second control gate.

20. The method according to claim 19, further comprising:

forming an embedding dielectric layer such that the main gate, the first control gate and the second control gate are in contact with the embedding dielectric layer;

wherein a first portion of the embedding dielectric layer separates the main gate from the first control gate; and

wherein a second portion of the embedding dielectric layer separates the main gate from the second control gate.

21. The method according to any one of claims 12 to 17,

wherein a portion of the first control gate is over a first portion of the main gate; and

wherein a portion of the second control gate is over a second portion of the main gate.

22. The method according to claim 21, further comprising:

forming an embedding dielectric layer such that the main gate, the first control gate and the second control gate are in contact with the embedding dielectric layer;

wherein a first portion of the embedding dielectric layer separates the main gate from the first control gate; and

wherein a second portion of the embedding dielectric layer separates the main gate from the second control gate.

23. The method according to any one of claims 12 to 22,

wherein the first contact electrode and the second contact electrode are formed in a same lithographic step.

24. The method according to any one of claims 12 to 23,

wherein the dielectric layer is formed before forming the main gate, the first control gate and the second control gate.

25. The method according to any one of claims 12 to 24,

wherein the first control gate and the second control gate are formed in a same lithographic step.