

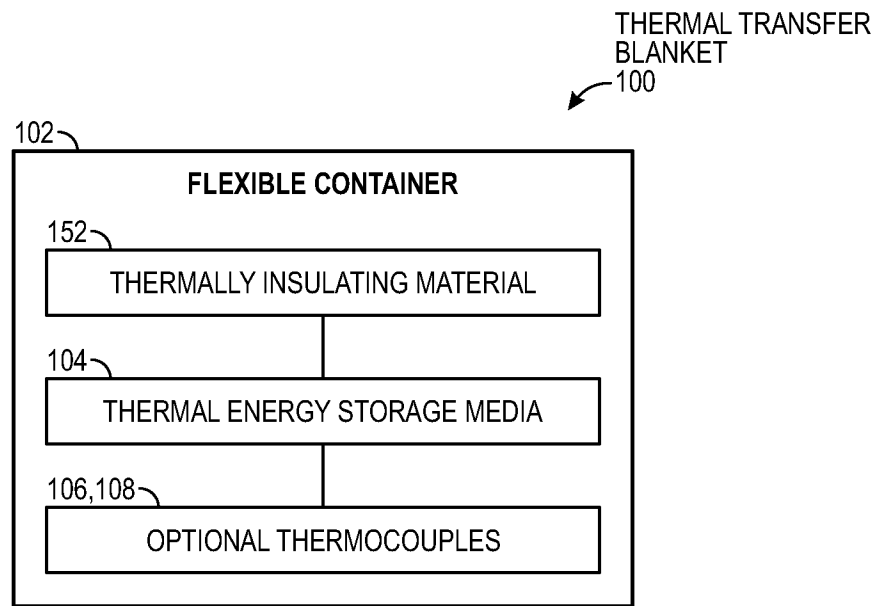
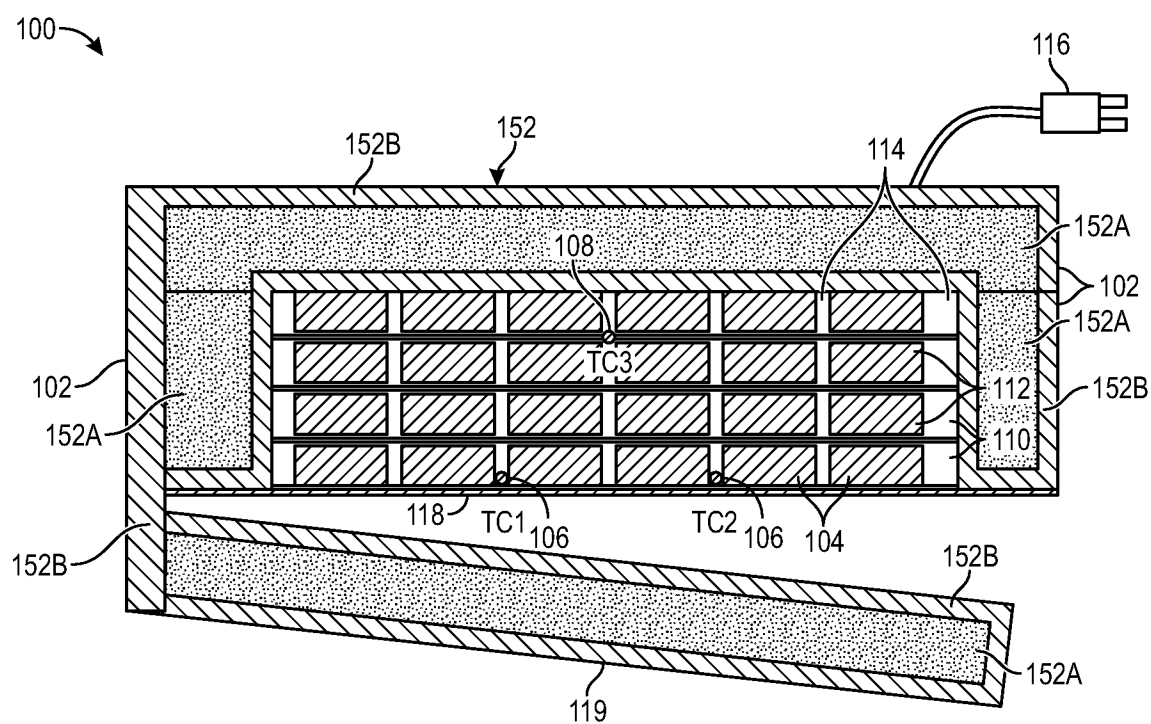
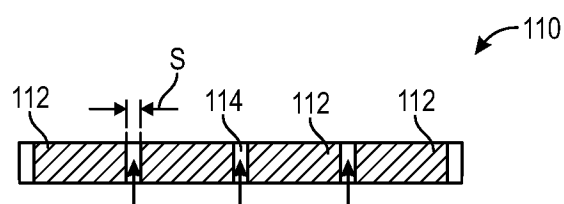
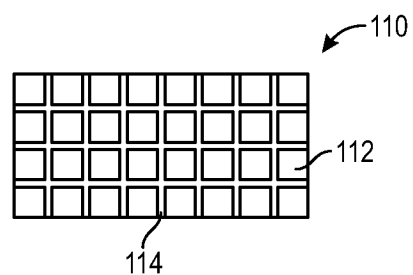


FIG. 1

**FIG. 2****FIG. 3****FIG. 4**

A cross-sectional view of a semiconductor device 100. The device consists of a substrate 110 with a bottom layer 111. A central region contains a stack of layers: a bottom layer 112, a middle layer 108, and a top layer 106. This central region is flanked by side regions 114. The entire structure is covered by a top layer 152. A horizontal dimension L_1 is indicated across the central region, and a vertical dimension L_2 is indicated for the top layer 152. A cable 116 is connected to the top layer 152. Other labels include 102 and 113 pointing to specific interfaces or features.

100

152

116

102

152

108

120

122

106

118

106

122

124

FIG. 7

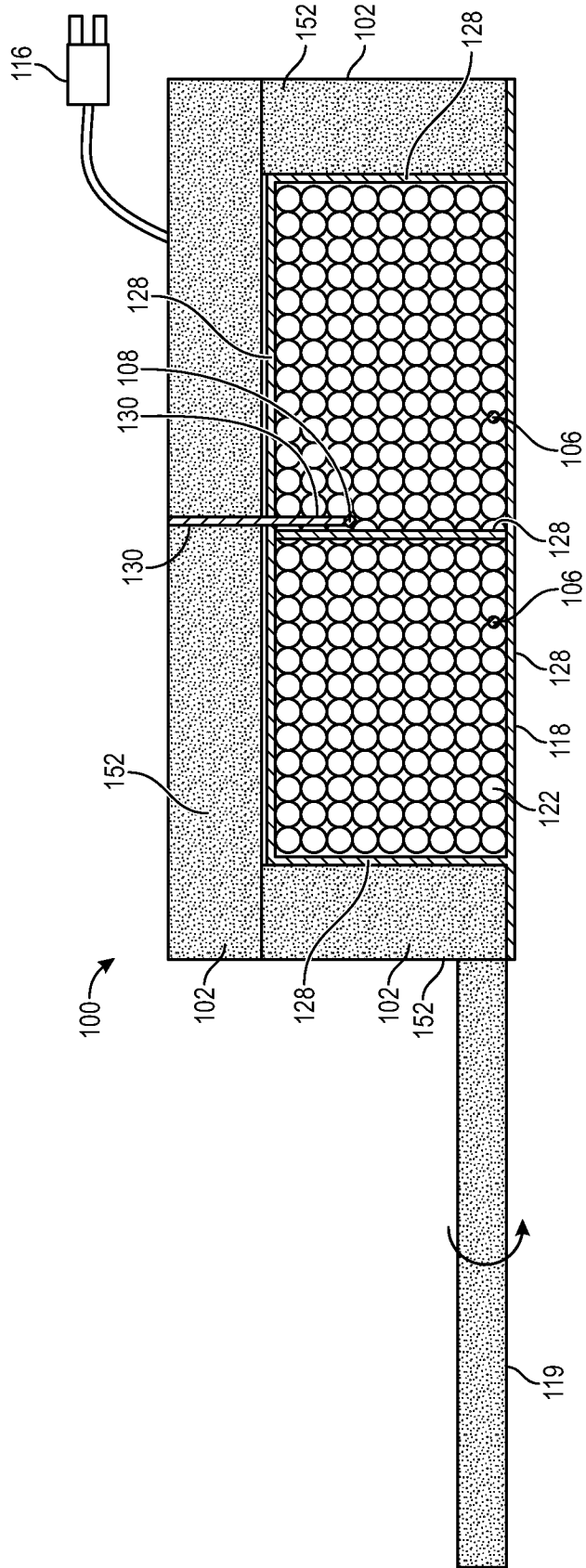


FIG. 8

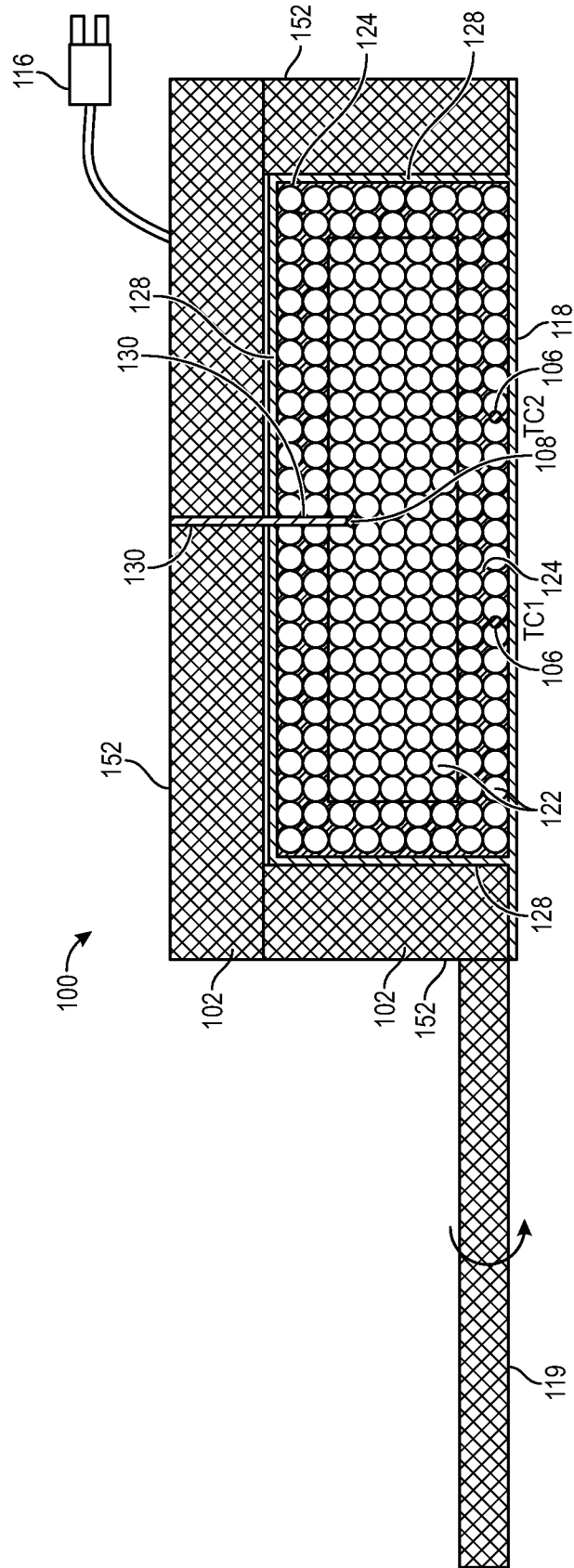


FIG. 9

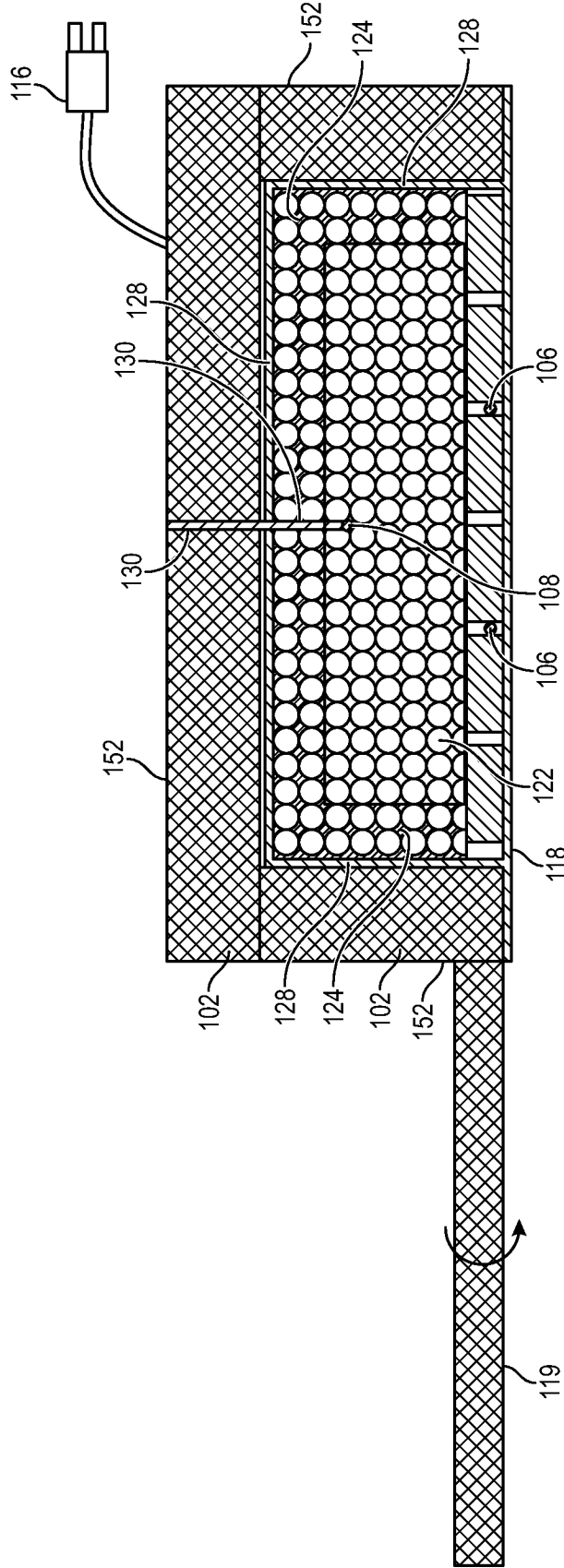


FIG. 10

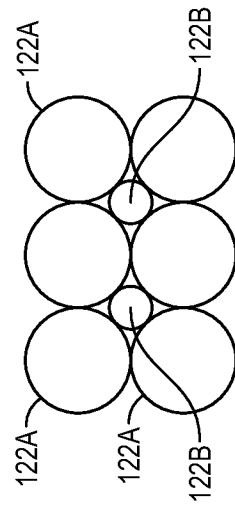
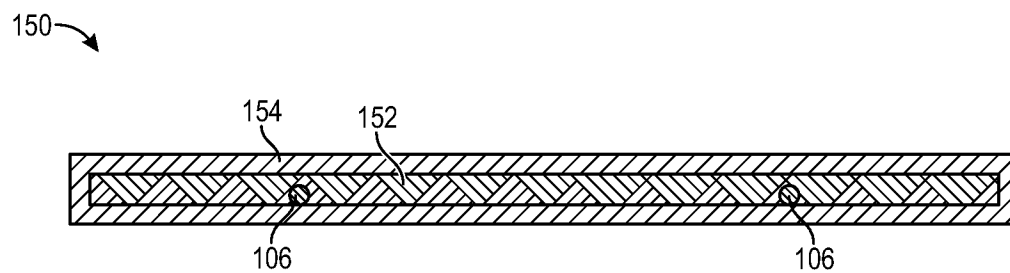
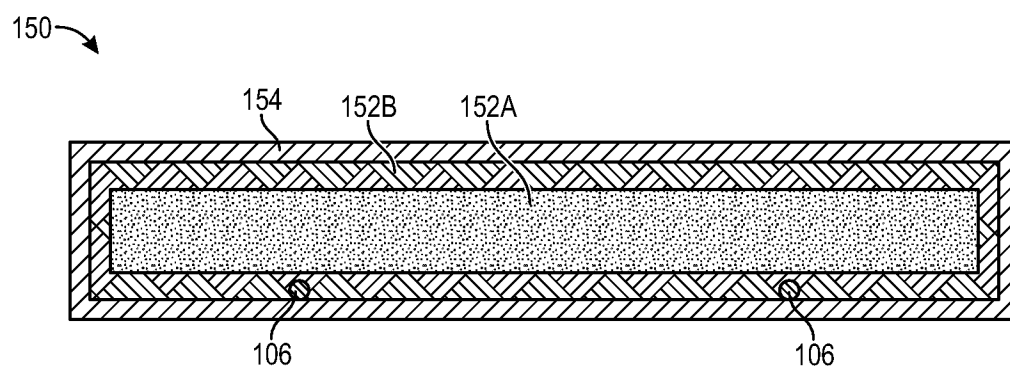
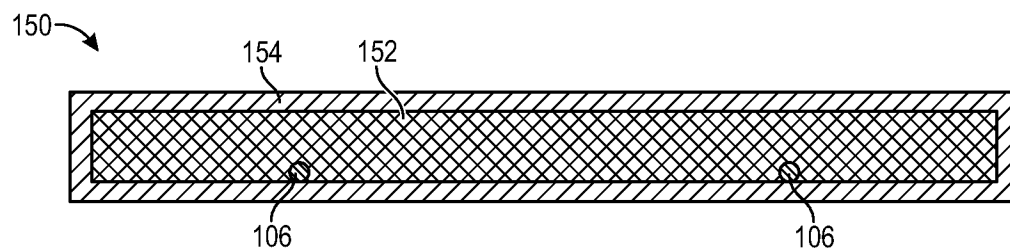
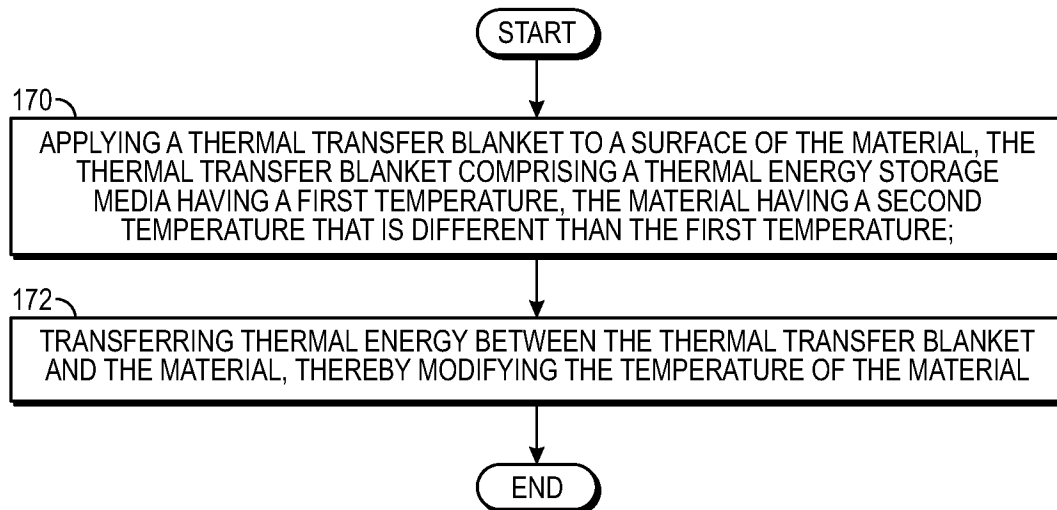
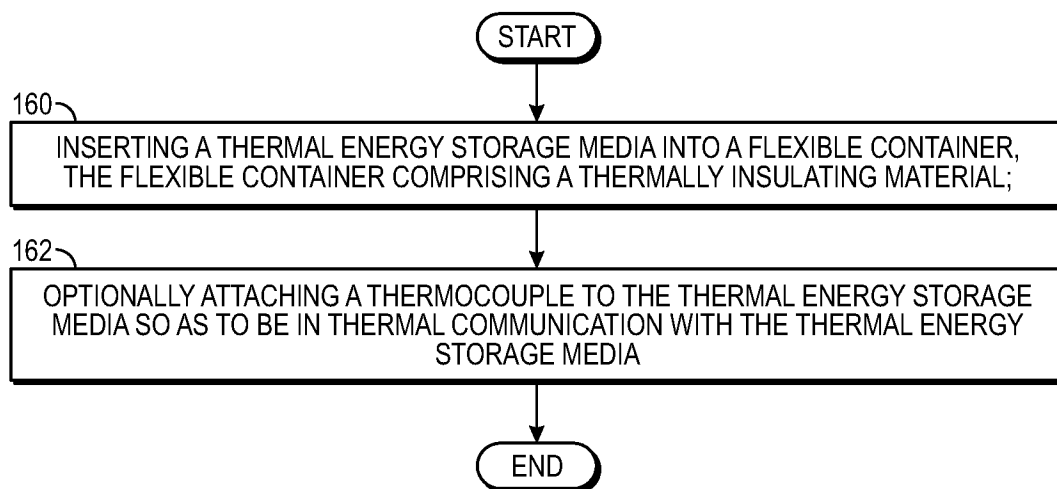


FIG. 11

**FIG. 12****FIG. 13****FIG. 14**

**FIG. 15****FIG. 16**

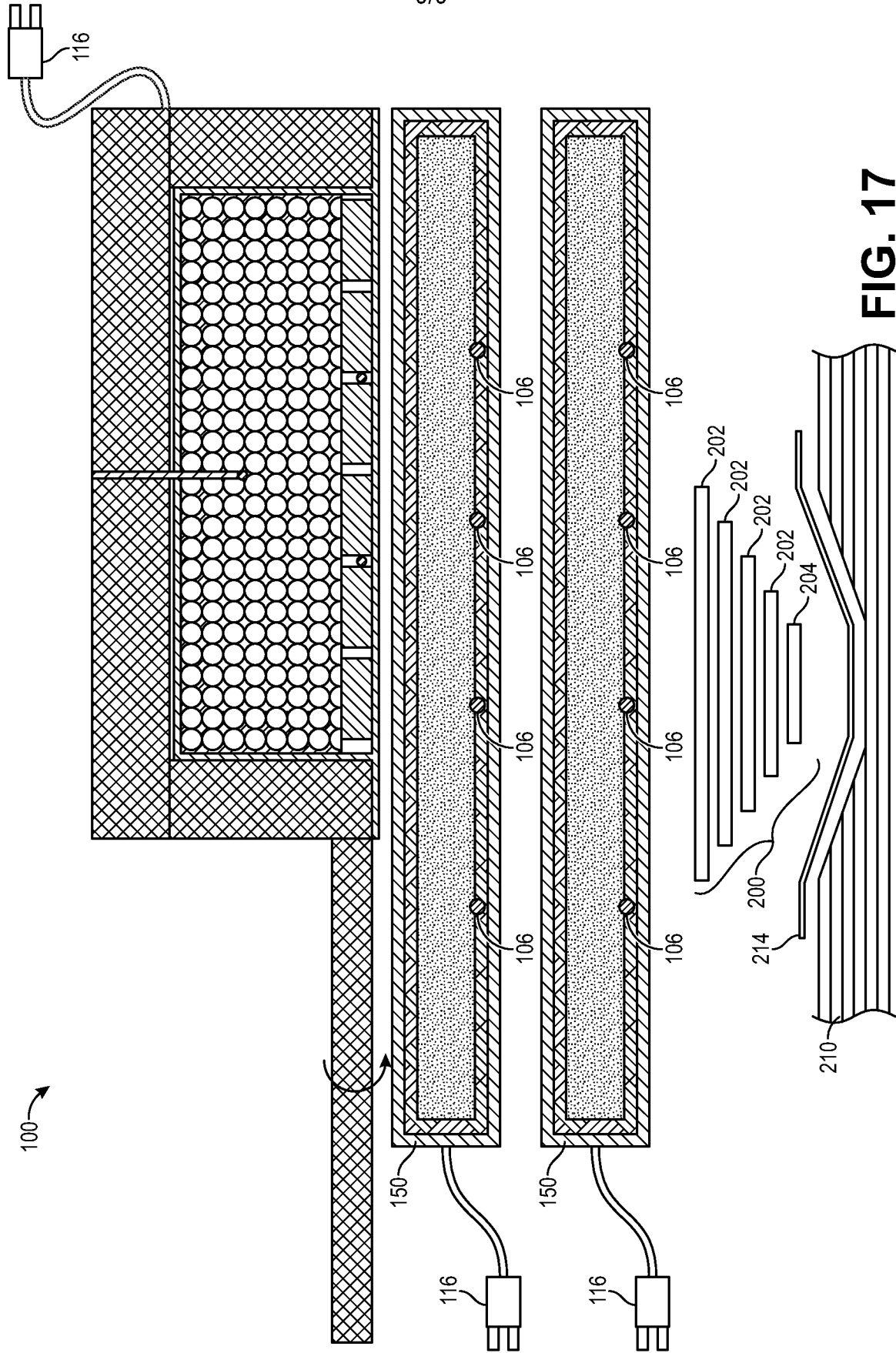


FIG. 17