CLAIMS

1. A semiconductor structure, comprising:

a source region and a drain region, the source region and the drain region being arranged at intervals on a substrate;

a gate oxide layer arranged between the source region and the drain region;

a gate structure arranged on the gate oxide layer; and

a conductive plug arranged at a corresponding position of the source region and a corresponding position of the drain region;

wherein the gate structure comprises a conductive layer having an inclined side surface facing toward the conductive plug.

2. The semiconductor structure according to claim 1, wherein the gate structure comprises a first conductive layer and a second conductive layer; and

the first conductive layer is arranged on the gate oxide layer, the second conductive layer being arranged on the first conductive layer, the second conductive layer comprising a plurality of metal layers stacked, at least one of the plurality of metal layers having an inclined side surface facing toward the conductive plug.

3. The semiconductor structure according to claim 2, wherein the first conductive layer comprises a polysilicon layer, the second conductive layer comprising a titanium nitride layer and a tungsten layer stacked from bottom to top, and the tungsten layer having an inclined side surface facing toward the conductive plug.

4. The semiconductor structure according to claim 1, wherein the gate structure comprises a first dielectric layer and a third conductive layer; and

the first dielectric layer is arranged on the gate oxide layer, the third conductive layer being arranged on the first dielectric layer, the third conductive layer being a metal layer having an inclined side surface facing toward the conductive plug.

5. The semiconductor structure according to claim 4, wherein the first dielectric layer comprises a high dielectric constant material, the third conductive layer comprising a tungsten layer.

6. The semiconductor structure according to claim 1, wherein a first distance from an upper edge of the inclined side surface to the conductive plug is less than a second distance from a lower edge of the inclined side surface to the conductive plug.

7. The semiconductor structure according to claim 1, wherein a first distance from an upper edge of the inclined side surface to the conductive plug is greater than a second distance from a lower edge of the inclined side surface to the conductive plug.

8. The semiconductor structure according to claim 6 or 7, wherein a surface of a middle position of the inclined side surface is planar, the middle position of the inclined side surface being positioned between the upper edge and the lower edge of the inclined side surface.

9. The semiconductor structure according to claim 6 or 7, wherein a surface of a middle position of the inclined side surface is stair-stepping, the middle position of the inclined side surface being positioned between the upper edge and the lower edge of the inclined side surface.

10. The semiconductor structure according to claim 1, wherein the semiconductor structure further comprises:

a second dielectric layer arranged on the substrate and the gate structure; and

a contact hole penetrating through the second dielectric layer and contacting with the

corresponding source region and the drain region, a bottom of the contact hole being a shallow trench structure, and the shallow trench structure being positioned in the corresponding source region and the drain region;

wherein the conductive plug comprises a metal plug filled in the contact hole and a barrier layer positioned between the metal plug and an inner wall of the contact hole.

11. The semiconductor structure according to claim 10, wherein a metal silicide is filled between the conductive plug and an inner wall of the shallow trench structure.

12. The semiconductor structure according to claim 1, wherein the gate structure further comprises a protection layer arranged on the gate structure.

13. The semiconductor structure according to claim 1 or 12, wherein the gate structure further comprises a side isolation structure affixed to two side surfaces of the gate structure facing toward the source region and the drain region.

14. The semiconductor structure according to claim 13, wherein the side isolation structure comprises a first isolation sidewall and a second isolation sidewall; and

the first isolation sidewall is affixed to a side surface of the gate structure, the second isolation sidewall being positioned at a periphery of the first isolation sidewall, a top of the second isolation sidewall extending to a top of the first isolation sidewall to form an enclosed space filled with a spacer medium,

wherein a material of the first isolation sidewall and a material of the second isolation sidewall comprise silicon nitride, the spacer medium comprising silicon oxide or air.

15. A method for fabricating a semiconductor structure, comprising:

forming a gate oxide layer;

forming a gate structure on the gate oxide layer;

forming a source region and a drain region on two sides of the gate structure; and

forming a conductive plug at a corresponding position of the source region and a corresponding position of the drain region, respectively;

wherein the gate structure comprises a conductive layer having an inclined side surface facing toward the conductive plug.

16. The method according to claim 15, wherein the forming a gate structure on the gate oxide layer comprises:

forming a first conductive layer on the gate oxide layer;

forming a second conductive layer on the first conductive layer, the second conductive layer comprising a plurality of metal layers stacked;

repeatedly performing following steps until the first conductive layer is exposed: if a current layer exposed in a first region is a predetermined metal layer, etching the predetermined metal layer in the first region and adjusting an etching direction and an etching rate until a next metal layer is exposed, such that the predetermined metal layer has an inclined side surface facing toward the source region and the drain region; and if the current layer exposed in the first region is not the predetermined metal layer, etching down the current layer in the first region or a region not covered by an upper layer until a next metal layer is exposed, wherein the first region is a region other than a region between the source region and the drain region; and

etching down the first conductive layer in the first region or the region not covered by the upper layer until the gate oxide layer is exposed to form the gate structure.

17. The method according to claim 15, wherein the forming a gate structure on the gate oxide layer comprises:

forming a first dielectric layer on the gate oxide layer;

forming a third conductive layer on the first dielectric layer, the third conductive layer being a metal layer;

etching the third conductive layer in a first region and adjusting an etching direction and an etching rate until the first dielectric layer is exposed, such that the third conductive layer has an inclined side surface facing toward the source region and the drain region, wherein the first region is a region other than a region between the source region and the drain region; and

etching down the first dielectric layer exposed in the first region or not covered by the third conductive layer until the gate oxide layer is exposed to form the gate structure.

18. The method according to claim 15, wherein the forming a conductive plug at a corresponding position of the source region and a corresponding position of the drain region comprises:

forming a second dielectric layer on a substrate and the gate structure;

forming a patterned etch protection layer on the second dielectric layer, the etch protection layer covering a surface of a dielectric layer except a partial region corresponding to the source region and a partial region corresponding to the drain region;

etching down from an exposed surface of the second dielectric layer until a surface of the source region and a surface of the drain region are exposed, and over-etching the surface of the source region and the surface of the drain region to form a contact hole with a shallow trench structure at a bottom thereof, the shallow trench structure being positioned in the corresponding source region and the drain region; and

forming a barrier layer on an inner wall of the contact hole, and filling a metal in the contact hole covered with the barrier layer to form the conductive plug,

wherein before the barrier layer is formed on the inner wall of the contact hole, the method further comprises:

forming a metal silicide on an inner wall of the shallow trench structure at the bottom of the contact hole.

19. The method according to claim 15, wherein the forming a gate structure on the gate oxide layer comprises:

forming a gate structure on the gate oxide layer, wherein a top layer of the gate structure is a protection layer.

20. The method according to claim 15 or 19, wherein after the gate structure is formed on the gate oxide layer, the method further comprises:

forming a side isolation structure on two side surfaces of the gate structure facing toward the source region and the drain region,

wherein the forming a side isolation structure on two side surfaces of the gate structure facing toward the source region and the drain region comprises:

forming a first isolation sidewall on the two side surfaces of the gate structure facing toward the source region and the drain region;

covering a spacer medium on an outer wall of the first isolation sidewall; and

forming a second isolation sidewall on the outer wall of the spacer medium, and a top of the second isolation sidewall extending to a top of the first isolation sidewall to form an enclosed space surrounding the spacer medium; or,

wherein the forming a side isolation structure on two side surfaces of the gate structure facing toward the source region and the drain region comprises:

forming a third isolation sidewall on two side surfaces of the gate structure facing toward the source region and the drain region;

covering a third dielectric layer on an outer wall of the third isolation sidewall;

forming a fourth isolation sidewall on an outer wall of the third dielectric layer, and a top of the fourth isolation sidewall extending to a top of the third isolation sidewall to form an enclosed space surrounding the third dielectric layer;

etching the top of the fourth isolation sidewall until a surface of the third dielectric layer is exposed to form an etching hole;

etching the third dielectric layer through the etching hole until reaching a surface of the gate oxide layer; and

enclosing the etching hole between the top of the fourth isolation sidewall and the top of the third isolation sidewall by means of a rapid deposition process to form an enclosed space filled with air.