CLAIMS

What is claimed is:

1. A method to locate and diagnose defects in an integrated circuit, comprising:

~~designing a defect under test (DUT) carrier unit comprising a plurality of logic devices;~~

designing a plurality of DUT structures within a defect under test (DUT) carrier unit, wherein a respective DUT structure comprises at least one process sensitive component;

designing a test structure by arranging the plurality of DUT structures within the DUT carrier unit, wherein a respective DUT structure forms a connection between an output of a first logic device and an input of a second logic device; and

simulating an expected output for a defect within the test structure, and storing the expected output in a look-up table (LUT)~~.~~;

applying heuristic yield analysis to the test structure to identify the defect within the test structure; and

utilizing the LUT to locate the defect without performing physical yield analysis (PFA).

~~2. The method of claim 1, further comprising:~~

~~applying heuristic yield analysis to the test structure to identify the defect within the test structure; and~~

~~utilizing the LUT to locate the defect without performing physical yield analysis (PFA).~~

~~3~~2. The method of claim 1, wherein a respective logic device within the DUT carrier unit has been yield-hardened through heuristic yield analysis and PFA to identify and correct defects.

~~4~~3. The method of claim 1, further comprising:

generating a multi-bit binary test vector for the test structure;

compiling a netlist of the test structure, the netlist comprising a definition of connections between ~~the~~ logic devices within the test structure formed by the plurality of DUT structures; and

simulating an expected output of applying the multi-bit binary test vector to the test structure along the connections formed by the DUT structures to define a possible failure location within the test structure.

~~5~~4. The method of claim ~~4~~3, further comprising:

applying the test vector to the test structure to generate a measured output; and

comparing the expected output stored in the LUT to the measured output to determine a failure location within the test structure.

~~6~~5. The method of claim ~~5~~4, wherein comparing an expected output to a measured output comprises:

obtaining a measured output comprising an output binary vector describing one or more connections of the test structure;

locating the output binary vector in the LUT; and

determining a failure location comprising a connection within the test structure by identifying a location corresponding to a failing bit in the output binary vector.

~~7~~6. The method of claim 1, further comprising:

performing PFA to the test structure at a failure location as defined by the LUT to determine a failure mode; and

cataloging the failure mode for future reference.

~~8~~7. The method of claim 1, further comprising arranging ~~the~~a plurality of logic devices within the DUT carrier unit to form a logic tree structure, wherein a respective connection formed between an output of a first logic device and an input of a second logic device comprises at least one process sensitive component within a respective DUT structure.

~~9~~8. The method of claim ~~8~~7, wherein the process sensitive component comprises a lithographic sensitive pattern formed on one or more of a front end of line gate material layer, a middle end of line interconnect layer, of back end of line metallization layer.

~~10~~9. The method of claim ~~9~~8, further comprising qualifying a discrete library of 2*n* – 1 allowable patterns through use of an *n*-to-1 XOR tree.

~~11~~10. A tool arrangement configured to locate and diagnose defects in an integrated circuit, comprising:

a test vector generator configured to define a test vector corresponding to a test structure;

a fault simulation tool configured to receive the test vector from the test vector generator and to simulate an expected output of applying the test vector to the test structure which corresponds to a failure location within the test structure.

a look-up table (LUT) configured to receive the expected output from the fault simulation tool and to store the expected output; and

a measurement and analysis tool configured to receive a measured output of applying the test vector to the test structure, and to compare the measured output to the expected output to determine a failure location within the test structure without performing physical failure analysis (PFA).

~~12~~11. The tool arrangement of claim ~~11~~10, further comprising:

a clock configured to control application of the test vector to the test structure;

a controller configured to control operation of the test vector generator and the clock;

a design tool configured to produce a design of the test structure; and

a netlist compiler configured to receive information about the design of the test structure, to compile a netlist of connections between a plurality of logic devices within the test structure, and to send the netlist to the fault simulation tool to simulate an expected output.

~~13~~12. The tool arrangement of claim ~~11~~10, the test structure comprising:

a first shift register controlled by a clock and configured to receive the test vector from the test vector generator;

a defect under test (DUT) carrier unit comprising a plurality of logic devices and a plurality of DUT structures, wherein a respective DUT structure forms a connection between an output of a first logic device and an input of a second logic device; and

a second shift register controlled by the clock and configured to receive a measured output from the DUT carrier unit, and to send the measured output to the measurement and analysis tool.

~~14~~13. The tool arrangement of claim ~~11~~10, further comprising a physical failure analysis (PFA) tool configured to receive the failure location from the measurement and analysis tool and assign a failure mode to a respective failure location.

~~15~~14. A yield learning circuit structure, comprising:

a defect under test (DUT) carrier unit comprising a plurality of logic devices arranged in a logic tree structure having a final DUT structure which outputs a measured value of the yield learning circuit structure, and an interior logic tree comprising a plurality of logic devices, wherein a respective logic device of the interior logic tree receives one or more inputs from a plurality of DUT structure, and sends its output to a single DUT structure~~, wherein a respective logic device has been yield-hardened through heuristic yield analysis and physical failure analysis (PFA) to identify and correct defects within the DUT carrier unit;~~ and

a plurality of DUT structures, a respective DUT structure comprising at least one process sensitive component which comprises a connection between an output of a first logic device and an input of a second logic device within the logic tree structure.

~~16. The yield learning circuit structure of claim 15, wherein the logic tree structure further comprises:~~

~~a final DUT structure which outputs a measured value of the yield learning circuit structure; and~~

~~an interior logic tree comprising a plurality of logic devices of one or more type, wherein a respective logic device of the interior logic tree receives one or more inputs from a plurality of DUT structures, and sends its output to a single DUT structure.~~

~~17~~15. The yield learning circuit structure of claim ~~15~~14, further comprising a shift register comprising a plurality of scan registers which are sequentially coupled and configured to receive a test vector as a serial data string and distribute the test vector in parallel format to the DUT carrier unit.

~~18~~16. The yield learning circuit structure of claim ~~17~~15, wherein the shift register is configured to receive a measured output from the DUT carrier unit and to distribute the measured output as a serial data string to a measurement and analysis tool.

~~19~~17. The yield learning circuit structure of claim ~~15~~14, wherein a respective logic device comprises one or more logic gates.

~~20~~18. The yield learning circuit structure of claim ~~15~~14, wherein the process sensitive component comprises a lithographic sensitive pattern formed on one or more of a front end of line gate material layer, a middle end of line interconnect layer, of back end of line metallization layer.

19. The tool arrangement of claim 10, further comprising:

a clock configured to control application of the test vector to the test structure; and

a controller configured to control operation of the test vector generator and the clock.

20. The yield learning circuit structure of claim 14, wherein a respective logic device has been yield-hardened through heuristic yield analysis and physical failure analysis (PFA) to identify and correct defects within the DUT carrier unit.