

MAGNETIC MEMORY STORAGE CELL AND PROCESS FOR READING AND WRITING DATA FROM AND TO SAME

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Field of the Invention

This invention relates to magnetic memory storage cells, particularly magnetic random access memory (MRAM) cells capable of storing multiple bits in a single memory cell. The invention further relates to methods for reading and writing bit
10 patterns to and from these types of storage cells.

Background of the invention

The first generation of MRAM based on anisotropic magnetoresistive (AMR) materials had relatively low storage density compared with other types of RAM (for example dynamic random access memory or DRAM). However, MRAM is popular for
15 military applications as it is non-volatile and radiation hard. MRAM typically uses an array of word and bit lines, with each bit line divided into n storage cells, and each cell composed of a trilayer. This trilayer comprises, for example, a ferromagnetic top layer, a non-magnetic middle layer and a ferromagnetic base layer. There are two stable magnetisation states for both top and base ferromagnetic layers (ie clockwise or
20 counterclockwise) corresponding with binary states one or zero.

The packing density and access time for AMR MRAM are relatively poor because the AMR effect is small, resulting in a magnetoresistance ratio in AMR materials of around 1-3%. However, since the discovery of the giant magnetoresistance (GMR) effect in 1988, there has been renewed interest in producing MRAM with higher storage
25 density and shorter access time, due to the desirable characteristics of MRAM being non-volatile and radiation hard. As the magnetoresistance ratio in GMR materials is much larger than that in AMR materials, there is the possibility of higher density and faster access magnetic storage. To date, however, feasible and practical designs have proven elusive.

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Summary of the Invention

The invention provides a magnetic random access memory (MRAM) storage cell characterised by a plurality of electrically connected magnetoresistive memory sub-units each having a plurality of sub-unit magnetisation states which in different combinations
5 provide said cell with a plurality of cell states.

Preferably, the memory sub-units are giant magnetoresistive (GMR) memory sub-units having a sandwich structure, and at least two different magnetic switching thresholds. Preferably all the ferromagnetic layers have different magnetic switching thresholds.

10 Preferably, the MRAM storage cell is used for storing a logic state in the MRAM storage cell by applying in sequence one or more magnetic fields to the MRAM storage cell,

characterised in that the magnitudes of the sequence of one or more magnetic fields are determined to successively modify, if necessary, the
15 magnetisation state of the cell to one of a non-increasing subset of possible magnetisation states of the cell and hence an associated bit pattern stored in the cell.

Preferably, the MRAM storage cell is also used for reading a logic state stored in the MRAM storage cell by applying in sequence one or more magnetic fields to the
20 MRAM storage cell,

characterised in that the magnitudes of the sequence of one or more magnetic fields are determined to successively modify, if necessary, the magnetisation state of the cell to one of a non-increasing subset of possible magnetisation states of the MRAM storage cell and hence an associated logic
25 state.

Brief Description of the Drawings

Figure 1(a) is a cross-sectional view of a conventional GMR cell 1 used as part of a preferred embodiment of the invention.

Figure 1(b) is a graph illustrating the magnetoresistive characteristics of the GMR cell 1 shown in Figure 1(a).

Figure 2(a) is a cross-sectional view of a GMR cell 2 similar to that shown in Figure 1(a).

Figure 2(b) is a graph illustrating the magnetoresistive characteristics of the GMR cell 2 shown in Figure 2(a).

Figure 3(a) is a cross-sectional schematic view of an MRAM cell 300 in accordance with an embodiment of the present invention, comprising a series connection of the GMR cells shown in Figures 1(a) and 2(a).

Figure 3(b) is a graph illustrating the magnetoresistance characteristics of the MRAM cell 300 shown in Figure 3(a).

Figure 4(a) is a cross-sectional schematic view of an MRAM cell 400 in accordance with another embodiment of the present invention, comprising a parallel connection of the GMR cells shown in Figures 1(a) and 2(a).

Figure 4(b) is a graph illustrating the magnetoresistance characteristics of the MRAM cell 400 shown in Figure 4(a).

Figures 5(a)-5(p) are graphs illustrating the response characteristics of the MRAM cell 300 shown in Figure 3(a) for logic states 0000-1111 from zero magnetic field to positive field and from zero magnetic field to negative magnetic field.

Figures 6(a)-6(p) are graphs illustrating the response characteristics of the MRAM cell 400 shown in Figure 4(a) for logic states 0000-1111 from zero magnetic field to positive field and from zero magnetic field to negative magnetic field.

Figure 7 is a table indicating a process for writing 16 different magnetic states to the MRAM cell 300 shown in Figure 3(a).

Figure 8 is a flow chart indicating a method for detecting a bit pattern stored in the MRAM cell 300 shown in Figure 3(a) in accordance with an embodiment of the present invention.

Figures 9(a)-9(h) are graphs illustrating the response characteristics for a modified application of the MRAM cell 300 in which the magnetisation vectors in one layer are pinned, storing bit patterns from 000-111 from zero magnetic field to positive magnetic field and from zero magnetic field to negative magnetic field.

Figure 10(a)-10(h) are graphs illustrating the response characteristics for a variation of the application for the MRAM cell 300 illustrated by Figures 9(a)-9(h), again storing bit patterns from 000-111 from zero magnetic field to positive magnetic field and from zero magnetic field to negative magnetic field.

Figure 11(a)-11(h) are graphs corresponding to figures 9(a)-9(h) but for a modified application of MRAM cell 400.

Figure 12(a)-12(h) are graphs corresponding to Figures 10(a)-10(h), but for the MRAM cell 400.

Figure 13 shows the process in accordance with an embodiment of the present invention for writing a three bit pattern into the MRAM cell 300 shown in Figure 3(a).

Figure 14 is a flow chart representing a method for reading a bit pattern stored in the MRAM cell 300 shown in Figure 3(a) in which the magnetisation vectors of the bottom ferromagnetic layer are pinned in the positive magnetic field direction.

Figure 15 is a flow chart representing a method for detecting or reading bit patterns stored in the MRAM cell 300 shown in Figure 3(a) in which the magnetisation vectors of the bottom ferromagnetic layer are pinned in the negative magnetic direction.

Description of the Preferred Embodiments

Referring to Figure 1(a), GMR cell 1 is a conventional memory cell comprised of three layers, two ferromagnetic layers 11 & 13 separated by non-magnetic middle layer 12. The materials used as the ferromagnetic layers can be single layers of magnetic materials, such as a layer of nickel, iron, cobalt or alloys thereof, including alloys having palladium or platinum. Alternatively either of the layers 11 or 13 can be composed of a magnetic composite layer such as a layer of nickel-iron-cobalt covering a layer of cobalt-iron and nickel-iron-cobalt or cobalt-iron with cobalt-iron at the interface between adjacent layers.

Materials suitable for layer 12 include most conductive materials, for example copper, copper alloys, chromium or chromium alloys.

Layers 11 and 13 each have a different magnetic switch threshold (i.e. they each switch states upon the application of magnetic fields of differing magnitude). A form of the cell suitable is disclosed in US patent 5703805. There, it is preferred that layer 11 has a thickness of approximately 4nm and layer 13 has a thickness of approximately 6nm if layers 11 and 13 are to be of the same material or materials of closely similar coercivity. Alternatively it may be preferable to use materials of different coercivity for layers 11 and 13 to allow the thickness of layers 11 and 13 to be adjusted to those appropriate to a given MRAM cell design.

The thickness of layer 12 should preferably be selected to ensure that layers 11 and 13 are ferromagnetically coupled in the absence of an external magnetic field.

Figure 1(b) shows the magnetoresistance of GMR cell 1 as shown in Figure 1(a) against the applied magnetic field produced by a sensing current. The X-ordinate indicates magnetic field direction and strength and the Y ordinate represents the magnetoresistance of GMR cell 1. At zero magnetic field, the ferromagnetic layers 11 and 13 are ferromagnetically coupled, and it is arbitrarily assumed that the magnetisation vectors are along the negative magnetic field direction.

The magnetisation vectors of layer 13 begin to rotate and increase the magnetoresistance as the applied total magnetic field strength increases from H_1 to H_2 . The magnetisation vectors of layer 11 continue switching to the other direction, increasing the magnetoresistance to a maximal value of R_H at a field strength of H_2 . The magnetoresistance keeps constant value of R_H until the magnetic field is increased to H_3 . At this point the magnetisation vectors of layer 13 begin to rotate and decrease the magnetoresistance as the magnetisation vectors of layer 13 switch to the other direction so that both of the ferromagnetic layers, 11 and 13 are in a parallel magnetic orientation. The magnetoresistance of the GMR cell 1 remains at a lower state of value of R_L in the absence of the sufficiently strong application of the magnetic field in the negative direction, owing to the characteristic hysteresis of ferromagnetic materials.

If a continuously increasing negative magnetic field is applied then similar changes in magnetoresistance are observed for increasingly negative magnitudes of applied magnetic field, as shown in the top left quadrant of Figure 1(b).

In Figure 1(b) (as in Figures 2(b), 3(b) and 4(b)) the curve representing magnetoresistance against positive applied magnetic field is shifted vertically a slight amount relative to the curve representing magnetoresistance against negative applied magnetic field, in order to differentiate the two curves. In practice, for any given cell, there is a common lower value magnetoresistance (R_L).

Figure 2(a) shows a GMR cell 2 similar to GMR cell 1 shown in Figure 1(a). Arrows 24 and 25 in layers 21 and 23 of GMR cell 2 are shown heavier than the corresponding arrows 14 and 15 in respective layers 11 and 13 of GMR cell 1 to indicate respectively higher magnetic switching thresholds. In all other respects the structure and principle of GMR cells 1 and 2 are the same.

Figure 3 shows a cross sectional schematic view of GMR cells 1 and 2 in series connection to form an MRAM cell 300. The magnetoresistance of the series connected cell 300 can be detected by applying a current from the word line through the storage cell

to the bit line. In this case, the measured magnetoresistance is in current-perpendicular-to-the-plane (cpp) configuration. The non-magnetic conductive layer 304 which connects GMR cell 1 and GMR cell 2 can be made of copper or copper alloys and the thickness of this layer should be thick enough so that there is no magnetic coupling between base
5 ferromagnetic layer 303 in GMR cell 1 and the top ferromagnetic layer 305 in GMR cell 2.

As mentioned earlier, the magnetic switching thresholds of the layers of GMR cell 1 are designed to be different (in this case, smaller) than those of the corresponding layers of GMR cell 2 so that when the GMR cells 1 and 2 are electrically connected there
10 are 16 different magnetisation states that depend on the orientation of the magnetisation vectors in the ferromagnetic layers of the cell. As discussed later, it is not necessary that each of the layers have a unique magnetic switching threshold. However, if certain layers have identical magnetic switching threshold (or if the magnetisation state of certain layers is disregarded as discussed later) then there are consequently less unique
15 magnetisation states which can correspond with an associated bit pattern.

The lowest magnetoresistance state occurs when all of the magnetisation vectors in the layers are ferromagnetically coupled while the highest magnetoresistance state occurs when the layers of GMR cell 1 as well as those of GMR cell 2 are anti-ferromagnetically coupled. Two intermediate different levels occur when the layers of
20 one cell are ferromagnetically coupled while the layers of the other cell are anti-ferromagnetically coupled. As GMR cell 2 has a generally higher magnetic switching threshold, the lower of these two intermediate levels occurs when the layers of GMR cell 1 are anti-ferromagnetically coupled, while the layers of GMR cell 2 are ferromagnetically coupled.

25 The magnetoresistance values of these states are determined by the magnetoresistance values of each individual cell, referred to in Figure 3(b).

$$R_1 = R_{L1} + R_{L2}$$

$$R_2 = R_{H1} + R_{L2}$$

$$R_3 = R_{L1} + R_{H1}$$

$$R_4 = R_{H1} + R_{H2}$$

- 5 Magnetoresistive value R_2 corresponds with parallel coupling in GMR cell 2 and anti-parallel coupling in GMR cell 1 while magnetoresistive value R_3 corresponds to parallel coupling in GMR cell 1 and anti-parallel coupling in GMR cell 2.

Figure 3(b) shows the magnetoresistance of the MRAM cell 300 against applied magnetic field. It is assumed for the top right quadrant that the magnetisation vectors initially point along the negative magnetic field direction for increasing positive magnetic field, and vice-versa for the top left quadrant. With applied positive magnetic field, the magnetisation vectors of layer 301 begin to rotate in the opposite (positive) direction to increase the magnetoresistance as the magnetisation vectors of layers 301 and 303 become anti-parallel. This behaviour is expected at H_1 to H_2 due to the characteristic curve in Figure 1(b). As magnetic field reaches H_2 the magnetoresistance of the cell becomes R_2 . It remains at this value as the magnetic field increases to H_3 at which the magnetisation vectors of layer 305 also begin to rotate in the opposite direction thus further increasing the magnetoresistance as layers 305 and 307 become anti-parallel. At H_4 this process is complete and the storage cell reaches its highest level of magnetoresistance, R_4 . As applied magnetic field increases through H_5 , H_6 , H_7 and H_8 , magnetoresistance decreases as the ever increasingly positive magnetic field brings layers 301 and 303, and 305 and 307 into parallel coupling.

Corresponding changes are observed when the applied magnetic field is decreased to zero (with the magnetisation vectors of the ferromagnetic layers remaining in the positive orientation due to the characteristic hysteresis of ferromagnetic materials) and increased for negative values. This is seen in the opposite quadrant of Figure 3(b).

Figure 4 shows an alternative embodiment of an MRAM cell 400 with two GMR cells 1 and 2 electrically connected in parallel. GMR cells 1 and 2 are separated by an insulator 404, such as the dielectric insulator SiO_2 or Si_3N_4 . The bit line is still along the length of the sensor.

5 The parallel connected MRAM cell 400 also has four distinct magnetoresistance states though these different states do not directly correspond with the same relative couplings of the ferromagnetic layers of cells 1 and 2. The smallest and largest states still occur when the respective layers of each GMR cell are coupled parallel or anti-parallel respectively. However, the two intermediate states are different. The higher of the two
10 intermediate states (R_3) occurs when the magnetisation vectors of the layers in cells 2 are parallel while those in cell 1 are anti-parallel. Conversely, the lower of the two intermediate states (R_2) occurs when the layers of cell 2 are anti-parallel and the layers of cell 1 are parallel. This difference is entirely due to the different nature of series and parallel connections. The magnetoresistance values of these four states are as follows
15 (where “//” means “in parallel with” eg $X//Y = XY/(X+Y)$):

$$R_1 = R_{L1} // R_{L2}$$

$$R_2 = R_{H2} // R_{L1}$$

$$R_3 = R_{H1} // R_{L2}$$

$$R_4 = R_{H1} // R_{H2}$$

20 Figures 5 and 6 show the response characteristics of the 16 magnetisation states possible

for MRAM cells 300 and 400. These response characteristics are determined by the changes in magnetoresistance that occur as applied magnetic field increases from zero in either the positive or negative direction. Having established an association between a bit
25 pattern and the 16 magnetisation states of the MRAM cell, each bit pattern also has a

unique associated response characteristic. These are shown in Figure 5 for MRAM cell 300 and in Figure 6 for MRAM cell 400.

The different orientations of the four magnetisation vectors in the four layers of MRAM cells 300 and 400 provide the basis of 16 distinct magnetisation states, each of which can be associated with a unique 4-bit pattern.

The process for writing a bit pattern to an MRAM cell is now described. Once a given bit pattern is associated with a given magnetisation state, a magnetic field or a sequence of magnetic fields can be applied to the MRAM cell to “write” a particular magnetisation state and thus bit pattern to the MRAM cell.

Figure 7 indicates the procedure used to store 16 binary states (4 bits) into the series connected MRAM cell 300. The process can be achieved for any initial magnetisation pattern as indicated in the first column by the inclusion of all enumerated bit patterns as initial states. However, when a particular initial state is known, it is possible in some cases to use a more expedient process for writing a given bit pattern to the cell 300, thus saving time.

The states to be stored are listed from 1111 through to 0000. A maximum of 4 distinct magnetic fields is necessary to achieve the 16 unique magnetisation states from an indeterminate initial state. A sequence of one or more magnetic fields is listed for each state to be stored and the corresponding resultant magnetisation state represented in a subsequent column by a stack of magnetisation vectors representing the direction of magnetisation of each layer. An arrow ($\rightarrow$) pointing to the right is in positive orientation, the magnetisation fields are classified in magnitude and direction. The H^{+++} field is sufficient to orient all the layers in the positive direction as indicated in the remark column and from the resultant orientation by contrast the H^{++} field is of a strength sufficient to change only the three layers with the least magnetic switching threshold to the positive direction. It is not sufficient to change the layer with the highest magnetic switching threshold to the positive direction. Similarly, a field of strength H^{+} is only

capable of orienting the layers with the two least magnetic switching thresholds to the positive direction, while a magnetic field of strength H^+ can only orient the layer with the least magnetic switching threshold to the positive direction.

For the fields used to write bit patterns, the following relations apply:

$$\begin{aligned}
 5 \quad & H_2 < H^+ < H_3 \\
 & H_4 < H^{++} < H_5 \\
 & H_6 < H^{+++} < H_7 \\
 & H_8 < H^{++++} \\
 & -H_3 < H^- < -H_2 \\
 10 \quad & -H_5 < H^- < -H_4 \\
 & -H_7 < H^- < -H_6 \\
 & H^- < -H_8
 \end{aligned}$$

With these factors in mind the process for writing the designated bit patterns to the GMR cell 300 becomes clear in view of Figure 7. When 1111 or 0000 are to be stored in MRAM cell 300, only one magnetic field (ie H^{++++} or H^- respectively) needs to be applied. When bit patterns 1110, 1101, 1100, 0011, 0010, 0001 are to be stored a first magnetic field followed by a second magnetic field is necessary. The application of three magnetic fields is necessary to achieve bit patterns 1011, 1010, 1001, 0110, 0101, 0100. Bit patterns 1000 and 0111 require the application of four magnetic fields. The particular sequence of magnetic fields required are all indicated in Figure 7.

The association of different bit patterns with orientations of magnetic vectors is arbitrary and the particular sequence of magnetisation steps described in Figure 7 is chosen for convenience, being applicable to any initial magnetisation state. Thus it follows that various different methods are possible. For example, if the initial state is

known, this information can be used to reduce or eliminate the number of magnetisation steps to write the binary state.

We now turn to the complementary method of reading a bit pattern stored in an MRAM cell 300 or 400.

5 The response characteristics shown in Figure 5 or 6 provide a basis for establishing a read procedure for determining the bit patterns stored by a particular magnetisation state of the MRAM cell.

Figure 8 is a flow chart of one particular method of detecting the 16 states contained in MRAM cell 300. Initially no word current is applied and a sense current is
10 applied to sense resistance followed by auto-zeroing of the circuit (block 800).

A magnetic field of magnitude H^+ is produced by the combination of a sense current in a sense line and a word current in a word line (block 801). The change of magnetoresistance due to applying the first magnetic field is sensed (block 802). The sensed resistance is either increased, decreased or the same as the resistance prior to
15 applying this first magnetic field, as indicated in Figure 5. Referring to all the graphs in Figure 5, there are four states in which resistance decreases and another four in which resistance increases, while the resistance does not change for the remaining eight states. For the association set out in Figure 7, the binary states in which resistance increases are 1000, 1100, 0000 or 0100. Resistance decreases for bit patterns 1110, 1101, 0101 and
20 0110. If the resistance does not change after the application of the first magnetic field, it is deduced that the MRAM cell 300 contains one of the bit patterns of the eight possibilities: 1111, 1011, 1001, 1010, 0011, 0111, 0010 or 0001. Thus this first step establishes that the bit pattern stored in the MRAM cell 300 is a member of one particular sub-set of three non-overlapping sub-sets of all possible bit patterns in the
25 MRAM cell 300.

A second field H^{++} is then applied and the resistance after application of this field is again measured. The possibilities for the stored bit pattern are narrowed further by this iteration. Further iterations may be necessary until the stored bit pattern is deduced by a sequence of applying a magnetic field and sensing the resultant change, if any, of the magnetoresistance. These subsequent steps are all shown in Figure 8.

Once the stored bit pattern has been read from MRAM cell 300, the magnetisation pattern is, of course, changed from its initial state. In most cases, the initial state needs to be restored to the MRAM cell 300. This is most conveniently done in accordance with the writing procedure outlined above and shown in Figure 7.

In restoring a bit pattern rather than writing a bit pattern from scratch, however, the previous magnetisation steps can be taken into account to reduce the number of further magnetisation steps with which a bit pattern is restored. For example, to read bit pattern 1110 (shown in Figure 7 as Case 2) a sequence of magnetisation steps is denoted by blocks 801, 803, 8036, 80391 (namely H^+ , H^{++} , H^{+++} and H^{++++}). It is not necessary in accordance with Figure 7 to again apply H^{++++} before applying H^- . By extension, this technique can be used in any instance of writing a binary state to the MRAM cell 300 when the previous state is known to provide the least number of magnetic fields to restore the initial bit pattern.

Other embodiments are possible in which the number of bits stored in the MRAM cell 300 or 400 is not the maximum possible. For example, the direction of the magnetisation vectors of layer 307 or 407 can be fixed. This can be done by pinning either of these layers 307 or 407 with antiferromagnetic materials such as FeMn NiO NiMn, etc, or by just letting the MRAM cell 300 or 400 operate at magnetic fields below H_7 . In both cases, a layer is essentially disregarded either by using an antiferromagnetic material or by using relatively low magnetic fields below the highest magnetic switching threshold. Thus the possible magnetisation states are reduced to 8, and consequently only three bits can be stored.

Figure 9 illustrates the response characteristics of the MRAM cell 300 for bit patterns from 000 to 111, in which the magnetisation vectors of the bottom ferromagnetic layer 307 of the GMR cell 2 is pinned along the positive magnetic field direction. It is assumed that the bit pattern 111 corresponds with a magnetisation in which the magnetisation vectors all along the positive magnetic field direction.

Figure 10 illustrates the response characteristics of the MRAM cell 300 for bit patterns from 000 to 111, in which the magnetisation vectors of the bottom ferromagnetic layer 307 of the GRM cell 2 is pinned instead along the negative magnetic field direction. Similarly it is assumed that the bit pattern 111 corresponds with a magnetisation in which the magnetisation vectors all along the positive magnetic field direction.

The method for writing bit patterns of three bits to a MRAM cell 300 in which a layer is pinned is similar to that used for the MRAM cell 300 if none of the layers are pinned. The method for reading bit patterns of three bits is also similar. Figures 13 and 14 respectively indicate the write and read procedures for a MRAM cell 300 in which the layer 307 is pinned in the positive magnetic field direction, as in Figure 9. Figure 15 shows the read procedure for the MRAM cell 300 if layer 307 is pinned to the negative field direction, as in Figure 10.

Figures 11 and 12 shows response characteristics of the MRAM cell 400 for bit patterns from 000 to 111, in which the magnetisation vectors of layer 407 are pinned respectively in a positive or negative magnetic field direction.

Of course, the magnetisation vectors of two ferromagnetic layers can be pinned to provide a MRAM cell in which two bits can be stored and detected in a manner analogous to that used for MRAM cells storing three or four bits.

The foregoing describes embodiments of the present invention and modifications, obvious to those skilled in the art can be made thereto, without departing from the scope of the present invention.

Claims

1. A magnetic random access memory (MRAM) storage cell characterised by a plurality of electrically connected magnetoresistive memory sub-units each having a plurality of sub-unit magnetisation states which in different combinations provide said cell with a plurality of cell states.
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2. A MRAM storage cell according to claim 1 further characterised in that said magnetoresistive memory sub-units are giant magnetoresistive (GMR) memory sub-units.
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3. A MRAM storage cell according to claim 1 or 2 further characterised in that each magnetoresistive sub-unit comprises a sandwich structure having a first ferromagnetic layer and a second ferromagnetic layer separated by a non-magnetic layer.
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4. A MRAM storage cell according to claim 3 further characterised in that the ferromagnetic layers have at least two different magnetic switching thresholds.
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5. A MRAM storage cell according to claim 4 further characterised in that all of the ferromagnetic layers have different magnetic switching thresholds.
6. A MRAM storage cell according to claim 5 wherein the respective memory sub-units have substantially equal magnetoresistive ratios.
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7 A MRAM storage cell according to claim 4 or 5 whereby said different
magnetic switching thresholds arise from different layer thicknesses, from
different coercivities, or a combination thereof.

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8. A MRAM storage cell according to any one of claims 5 to 7 further
characterised in that there are two of said sub-units and a total of 16 distinct
readable cell magnetisation states adapted to correspond to respective 4 - bit logic
states.

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9. A MRAM storage cell according to any one of claims 3 to 8 further
characterised in that said memory sub-units are electrically connected in series.

10. A MRAM storage cell according to claim 9 further characterised in that
15 said memory sub-units are electrically connected in series by an electrically
conductive non-magnetic spacer layer of sufficient thickness to prevent magnetic
coupling between said sub-units.

11. A MRAM storage cell according to any one of claims 3 to 8 further
20 characterised in the said memory sub-units are electrically connected in parallel.

12. A MRAM storage cell according to claim 11 further characterised in that
said sub-units are joined but spaced by an electrically insulating non-magnetic
layer.

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13. A MRAM storage cell according to claim 1 or 2 further characterised in that one or more of said memory sub-units is of spin valve structure, or pseudo-spin valve structure, or a magnetic tunnel junction.
- 5 14. A MRAM storage cell according to any one of claims 1 to 3 further characterised in that one or more of the layers or sub-structures thereof has the orientation of its magnetisation vectors pinned, whereby to reduce the number of said distinct magnetisation states and the bit number of corresponding logic states.
- 10 15. A method of storing a logic state in a MRAM storage cell according to any one of claims 1 to 14 comprising applying in sequence one or more magnetic fields to the MRAM storage cell,
- 15 characterised in that the magnitudes of the sequence of one or more magnetic fields are determined to successively modify, if necessary, the magnetisation state of the cell to one of a non-increasing subset of possible magnetisation states of the MRAM storage cell and hence an associated logic state.
- 20 16. A method according to claim 15 wherein the one or more magnetic fields are determined by the logic state to be stored and the logic state previously stored in the MRAM storage cell.
- 25 17. A method of reading a logic state stored in a MRAM storage cell according to any one of claims 1 to 14, comprising applying in sequence one or more magnetic fields to the MRAM storage cell,



characterised in that the magnitudes of the sequence of one or more magnetic fields are determined to successively discriminate between non-increasing subsets of possible magnetisation states of the cell to eventually deduce the magnetisation state of the MRAM storage cell and hence an associated logic state.

18. A method according to claim 17 wherein the stored logic state is deduced on the basis of an increase, decrease or no change of magnetoresistance of the MRAM storage cell.

19. A method according to any one of claims 17 or 18 further including restoring the MRAM storage cell to its initial magnetisation state.

