

Abstract

**DIFFERENTIAL SENSE AMPLIFIER WITHOUT DEDICATED PASS-GATE
TRANSISTORS**

A differential sense amplifier for sensing data stored in a plurality of memory cells (C) of a memory cell array, including:

- a first CMOS inverter having an output connected to a first bit line (BL) and an input connected to a second bit line (/BL) complementary to the first bit line,
 - a second CMOS inverter having an output connected to the second bit line (/BL) and an input connected to the first bit line (BL),
- each CMOS inverter comprising a pull-up transistor (M21, M22) and a pull-down transistor (M31, M32), said sense amplifier having a pair of pass-gate transistors arranged to connect said first and second bit lines (BL, /BL) to a first and a second global bit lines (IO, /IO), wherein the pass-gate transistors are constituted by the pull-up transistors (M21, M22) or the pull-up transistors (M31, M32).

FIGURE 3