In another embodiment, the present invention is a semiconductor device comprising a semiconductor wafer. A conductive interconnect structure is formed over the semiconductor wafer having a height extending above the semiconductor wafer. An insulating layer is formed over the semiconductor wafer that exposes an upper surface of the conductive interconnect structure while maintaining coverage over a sidewall of the conductive interconnect structure.

Brief Description of the Drawings

FIG. 1 illustrates a printed circuit board with different types of packages mounted to its surface;

FIGs. 2a-2c illustrate further detail of the representative semiconductor packages mounted to the printed circuit board;

FIGs. 3a-3m illustrate a process of forming conductive bumps on a semiconductor device with a supporting and protective structure;

FIG. 4 illustrates a semiconductor device with conductive bumps having a supporting and protective structure;

FIGs. 5a-5~~n~~o illustrate a process of forming conductive vias through a semiconductor device with a supporting and protective structure and electrically connected contact pads; and

FIG. 6 illustrates conductive vias through a semiconductor device with a supporting and protective structure and electrically connected contact pads.

or positive-acting photo resist. Second, the photoresist layer is transferred into the wafer surface. The transfer occurs when etching removes the portion of the top layers of semiconductor wafer not covered by the photoresist. The chemistry of photoresists is such that the photoresist dissolves slowly and resists removal by chemical etching solutions while the portion of the top layers of the semiconductor wafer not covered by the photoresist is removed more rapidly. The process of forming, exposing, and removing the photoresist, as well as the process of removing a portion of the semiconductor wafer can be modified according to the particular resist used and the desired results.

In negative-acting photo resists, photoresist is exposed to light and is changed from a soluble condition to an insoluble condition in a process known as polymerization. In polymerization, unpolymerized material is exposed to a light or energy source and polymers form a cross-linked material that is etch-resistant. In most negative resists, the polymers are polyisopremnes. Removing the soluble portions (i.e., the portions not exposed to light) with chemical solvents or developers leaves a hole in the resist layer that corresponds to the opaque pattern on the reticle. A mask whose pattern exists in the opaque regions is called a clear-field mask.

In positive-acting photo resists, photoresist is exposed to light and is changed from relatively nonsoluble condition to a much more soluble condition in a process known as photosolubilization. In photosolubilization, the relatively insoluble resist is exposed to the proper light energy and is converted to a more soluble state. The photosolubilized part of the resist can be removed by a solvent in the development process. The basic positive photoresist polymer is the phenol-formaldehyde polymer, also called the phenol-formaldehyde

Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor wafer having a plurality of contact pads;

forming a first insulating layer over the semiconductor wafer and contact pads;

removing a portion of the first insulating layer to expose a first portion of the contact pads, while leaving a second portion of the contact pads covered by the first insulating layer;

forming an under bump metallization layer over the contact pads and the first insulating layer;

forming a plurality of bumps over the under bump metallization layer;

forming a second insulating layer over the semiconductor wafer to cover the first insulating layer, a sidewall of the under bump metallization layer, sidewall of the bumps, and upper surface of the bumps; and

removing a portion of the second insulating layer over a first portion of the sidewall of the bumps down to the first insulating layer ~~covering the upper surface of the bumps~~, while maintaining coverage of the second insulating layer over a second portion of the sidewall of the bumps and over the sidewall of the under bump metallization layer to provide structural support for the bumps and prevent growth of inter-metallic compounds.

2. The method of claim 1, wherein removing the portion of the second insulating layer further includes maintaining a thickness

of the second insulating layer at the sidewall of the bumps greater than one fourth of a height of the bumps.

~~3. The method of claim 1, wherein removing the portion of the second insulating layer further includes maintaining coverage of the second insulating layer over the first insulating layer outside a footprint of the bumps.~~

3. The method of claim 1, wherein forming the bumps includes forming cylindrical bumps.

4. The method of claim 1, wherein forming the bumps includes forming bumps with a rectangular cross-section.

~~4~~5. The method of claim 1, wherein forming the under bump metallization layer further includes:

forming an adhesion layer over the plurality of contact pads;

forming a barrier layer over the adhesion layer; and

forming a wetting layer over the barrier layer.

~~5~~6. A method of making a semiconductor device, comprising:

providing a semiconductor wafer;

forming a plurality of vias into the semiconductor wafer;

forming a liner layer in the vias;

depositing conductive material over the liner layer in the vias to form ~~forming~~ a plurality of conductive vias~~ through the semiconductor wafer having a portion that extends above a surface of the semiconductor wafer~~;

removing a portion of the semiconductor wafer so the conductive vias extend above a surface of the semiconductor wafer;

removing a portion of the liner layer to expose the conductive material;

forming a conductive liner over the conductive material after removing the portion of the liner layer;

forming an insulating layer over the semiconductor wafer and the conductive vias; and

removing a portion of the insulating layer ~~covering an upper surface of the conductive vias,~~ leaving the conductive liner extending above the insulating layer, while maintaining coverage of the insulating layer over a sidewall of the conductive vias to provide structural support for the conductive vias.

~~6. The method of claim 5, wherein forming the conductive vias further includes:~~

~~forming a temporary substrate over the semiconductor wafer;~~

~~forming a plurality of vias through the temporary substrate and the semiconductor wafer;~~

~~depositing a conductive material in the plurality of vias; and~~

~~removing the temporary substrate.~~

~~7. The method of claim 6, further including:~~

~~depositing a liner layer in the plurality of vias; and~~

~~removing a portion of the liner layer to expose the conductive material.~~

~~8. The method of claim 6, further including:~~

~~depositing a liner layer including an insulating thin film and a conductive liner material; and~~

~~removing a portion of the insulating thin film over the conductive vias to form a conductive liner layer.~~

~~9~~7. The method of claim ~~5~~6, wherein removing the portion of the insulating layer includes maintaining a thickness of the insulating layer greater than one fourth a height of the portion of the conductive vias that extends above the surface of the semiconductor wafer.

8. The method of claim 6, further including:

forming a plurality of semiconductor die in the semiconductor wafer; and

singulating the semiconductor die.

~~10~~9. The method of claim ~~5~~6, further including:

forming a conductive layer over and electrically connected to the conductive vias;

forming an insulating layer over the semiconductor wafer and the conductive layer; and

removing a portion of the insulating layer over the conductive layer to expose a surface area of the conductive

layer greater than a surface area of ~~the~~an upper surface of the conductive vias.

10. The method of claim 6, further including removing the portion of the insulating layer down to the semiconductor wafer.

11. A method of making a semiconductor device, comprising:

providing a semiconductor wafer;

forming a conductive interconnect structure ~~having~~ through the semiconductor wafer and including a height extending above a surface of the semiconductor wafer;

forming an insulating layer over the semiconductor wafer and the conductive interconnect structure with the insulating layer including a height greater than the height of the conductive interconnect structure; and

removing a portion of the insulating layer to leave a sloped contour ~~covering an upper surface of the conductive interconnect structure while maintaining coverage~~ of the insulating layer over a sidewall of the conductive interconnect structure.

12. The method of claim 11, wherein providing the semiconductor wafer further includes forming a plurality of semiconductor die in the semiconductor wafer.

~~12. The method of claim 11, wherein forming the conductive interconnect structure further includes forming a plurality of conductive bumps over the semiconductor wafer.~~

13. The method of claim 11, wherein forming the conductive interconnect structure further includes forming a plurality of conductive vias through the semiconductor wafer.

14. The method of claim 11, further including forming one or more redistribution layers over and electrically connected to the conductive interconnect structure.

145. The method of claim 11, wherein removing the portion of the insulating layer further includes maintaining a thickness of the insulating layer greater than one fourth the height of the conductive interconnect structure extending above the surface of the semiconductor wafer.

~~15. The method of claim 11, wherein removing the portion of the insulating layer further includes maintaining the insulating~~

~~layer outside a periphery of the conductive interconnect structure.~~

~~16. A semiconductor device, comprising:~~

~~a semiconductor wafer;~~

~~a conductive interconnect structure formed over the semiconductor wafer having a height extending above the semiconductor wafer; and~~

~~an insulating layer formed over the semiconductor wafer that exposes an upper surface of the conductive interconnect structure while maintaining coverage over a sidewall of the conductive interconnect structure.~~

~~17. The semiconductor device of claim 16, further comprising a conductive layer formed over the upper surface of the conductive interconnect structure.~~

~~18. The semiconductor device of claim 16, wherein the conductive interconnect structure comprises a plurality of conductive bumps formed over the semiconductor wafer.~~

~~19. The semiconductor device of claim 16, wherein the conductive interconnect structure comprises a plurality of conductive vias formed through the semiconductor wafer.~~

~~20. The semiconductor device of claim 16, wherein a thickness of the insulating layer adjacent to the conductive interconnect structure is greater than one fourth the height of the interconnect structure extending above the surface of the semiconductor wafer.~~

16. The method of claim 11, further including removing the portion of the insulating layer down to the semiconductor wafer.

17. A method of making a semiconductor device, comprising:

providing a substrate;

forming an interconnect structure through the substrate and including a height extending above a surface of the substrate;

forming an insulating layer over the substrate and interconnect structure; and

removing a portion of the insulating layer to leave a sloped contour of the insulating layer over a portion of a sidewall of the interconnect structure.

18. The method of claim 17, wherein removing the portion of the insulating layer further includes maintaining a thickness of the insulating layer greater than one fourth a height of the interconnect structure extending above a surface of the substrate.

19. The method of claim 17, wherein forming the interconnect structure further includes forming a plurality of conductive vias through the substrate.

20. The method of claim 17, further including forming one or more redistribution layers over and electrically connected to the interconnect structure.

21. The method of claim 17, further including removing the portion of the insulating layer down to the substrate.