CLAIMS

1. A semiconductor variable capacitor comprising: a semiconductor region; an insulative layer disposed above the semiconductor region; a first non-insulative region disposed above the insulative layer; a second non-insulative region disposed adjacent to the semiconductor region; and a control region disposed adjacent to the semiconductor region such that a capacitance between the first non-insulative region and the second non-insulative region is configured to be adjusted by varying a control voltage applied to the control region, wherein: the first non-insulative region is disposed above a first portion of the semiconductor region and a second portion of the semiconductor region; the control region or the second non-insulative region comprises a first side and a second side; the first portion and the second portion of the semiconductor region are disposed adjacent to the first side and the second side, respectively; and the first side is perpendicular to the second side with respect to a top view, and the first portion being adjacent to the first side with respect to the top view, and the second portion being adjacent to the second side with respect to the top view.

2. The semiconductor variable capacitor of claim 1, wherein: the first portion and the second portion of the semiconductor region are disposed adjacent to the first side and the second side of the control region, respectively; the first non-insulative region is disposed above a third portion of the semiconductor region and a fourth portion of the semiconductor region; and the third portion and the fourth portion of the semiconductor region are disposed adjacent to the first side and the second side of the second non-insulative region, respectively.

3. The semiconductor variable capacitor of claim 1, wherein: the first portion and the second portion of the semiconductor region are disposed adjacent to the first side and the second side of the control region, respectively; the first non-insulative region is disposed above a third portion of the semiconductor region and a fourth portion of the semiconductor region; and the third portion and the fourth portion of the semiconductor region are disposed adjacent to a third side and a fourth side of the control region, respectively.

4. The semiconductor variable capacitor of claim 3, further comprising: another control region disposed adjacent to the semiconductor region such that a capacitance between the first non-insulative region and the second non-insulative region is configured to be adjusted by varying another control voltage applied to the other control region, wherein: the first non-insulative region is disposed above a fifth portion of the semiconductor region and a sixth portion of the semiconductor region; and the fifth portion and the sixth portion of the semiconductor region are disposed adjacent to a first side and a second side of the other control region, respectively.

5. The semiconductor variable capacitor of claim 3, further comprising: another insulative layer disposed above the semiconductor region; a third non-insulative region disposed above the other insulative layer; and another control region disposed adjacent to the semiconductor region such that a capacitance between the second non-insulative region and the third non-insulative region is configured to be adjusted by varying another control voltage applied to the other control region, wherein: the third non-insulative region is disposed above a fifth portion of the semiconductor region and a sixth portion of the semiconductor region; and the fifth portion and the sixth portion of the semiconductor region are disposed adjacent to a first side and a second side of the other control region, respectively.

6. The semiconductor variable capacitor of claim 5, wherein the second non-insulative region is disposed between the control region and the other control region.

7. The semiconductor variable capacitor of claim 1, further comprising: another insulative layer disposed above the semiconductor region; a third non-insulative region disposed above the other insulative layer; and another control region disposed adjacent to the semiconductor region such that a capacitance between the second non-insulative region and the third non-insulative region is configured to be adjusted by varying another control voltage applied to the other control region, wherein: the third non-insulative region is disposed above a third portion of the semiconductor region; the first portion of the semiconductor region is disposed adjacent to a portion of the first side of the control region or the second non-insulative region; and the third portion of the semiconductor region is disposed adjacent to another portion of the first side of the control region or the second non-insulative region.

8. The semiconductor variable capacitor of claim 7, further comprising a fourth non-insulative region disposed adjacent to the semiconductor region, wherein: the first non-insulative region is disposed above a fourth portion of the semiconductor region; the third non-insulative region is disposed above a fifth portion of the semiconductor region; the fourth portion of the semiconductor region is disposed adjacent to a portion of the first side of the fourth non-insulative region; and the fifth portion of the semiconductor region is disposed adjacent to another portion of the first side of the fourth non-insulative region.

9. The semiconductor variable capacitor of claim 1, further comprising: another insulative layer disposed above the semiconductor region; a third non-insulative region disposed above the other insulative layer; and another control region disposed adjacent to the semiconductor region such that a capacitance between the second non-insulative region and the third non-insulative region is configured to be adjusted by varying another control voltage applied to the other control region, wherein: the third non-insulative region is disposed above a third portion of the semiconductor region; the first portion and the second portion of the semiconductor region are disposed adjacent

to the first side and the second side of the control region; and the third portion of the semiconductor region is disposed adjacent to a corner portion of the second non-insulative region.

10. The semiconductor variable capacitor of claim 1, wherein the control voltage is applied to the control region with respect to the second non-insulative region.